SM802181

Flexible Ultra-Low Jitter Clock Synthesizer

ClockWorks® FLEX

General Description

The SM802181 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply.

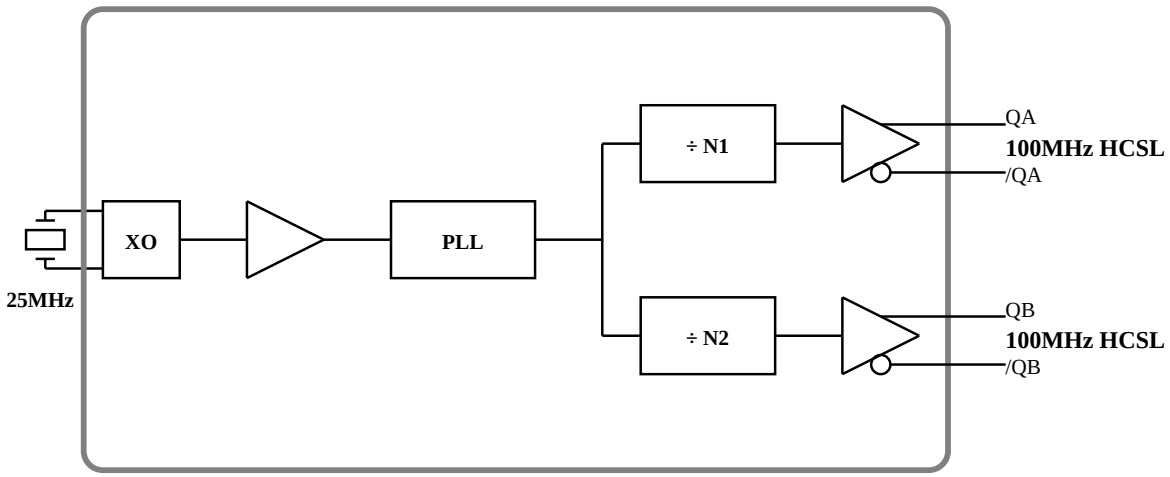
Applications

- PCI-Express
- Storage

Features

- Generates 2 output clocks
- Frequency and output logic:
  - 100MHz HCSL x 2
- 25MHz Crystal Input
- Typical phase noise:
  - 222fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Industrial temperature range
- 16-Pin 3mm x 3.5mm QFN package

Block Diagram

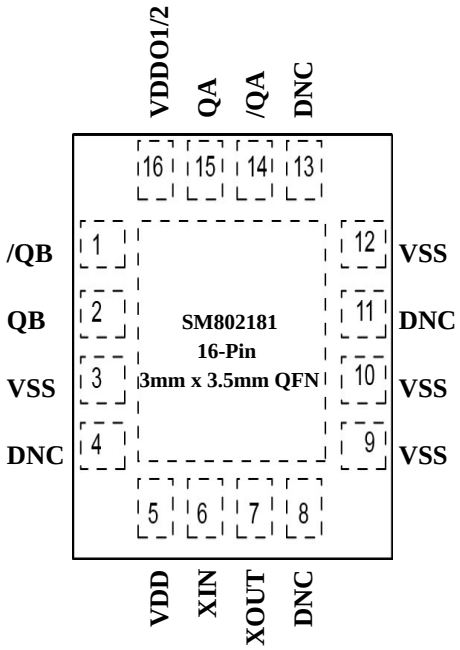


Ordering Information

Ordering Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM802181UMG	802181	Tube	-40°C to +85°C	16-Pin QFN (3x3.5 mm)
SM802181UMG TR	802181	Tape and Reel	-40°C to +85°C	16-Pin QFN (3x3.5 mm)

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 2	/QB, QB	O, Diff	HCSL	Bank 2 Clock Output Frequency = 100MHz
3, 9, 10, 12	VSS	PWR		Core Power Supply Ground
4, 8, 11, 13	DNC			Do not connect anything to these pins
5	VDD	PWR		Core Power Supply
6, 7	XIN, XOUT	I/O, SE		Crystal Reference Input/Output = 25MHz
14, 15	/QA, QA	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100MHz
16	VDDO1/2	PWR		Power Supply for the Outputs on Bank 1/2
-	EXPOSED PAD	-		The exposed pad must be connected to the VSS ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (VDD, VDDO1, VDDO2).....+4.6V
Input Voltage (VIN).....-0.50V to VDD + 0.5V
Lead Temperature (soldering, 20s).....260°C
Case Temperature.....115°C
Storage Temperature (T_S).....-65°C to +150°C
ESD Machine Model.....200V
ESD Human Body Model.....2000V

Operating Ratings[2]

Supply Voltage (VDD, VDDO1, VDDO2)
.....2.375V to +3.465V
Ambient Temperature (TA).....-40°C to +85°C
Junction Thermal Resistance[3]
QFN (T_{JA}) Still Air.....60°C/W

DC Electrical Characteristics[4]

VDD = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDD, VDDO1, VDDO2	3.3V Operating Voltage 2.5V Operating Voltage	VDDO1 = VDDO2 VDDO1 = VDDO2	3.135 2.375	3.3 2.5	3.465 2.625	V
IDD	Total supply current, VDD + VDDO	Outputs unterminated			136	mA

Crystal Characteristics

VDD = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF load capacitance	Fundamental, Parallel Resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				40	Ohms
Shunt Capacitor, CO			2	5	pF
Correlation Drive Level			10	100	µW

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

HCSL DC Electrical Characteristics[4]

VDD = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C, RL = 50 Ohms to VSS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage		660	700	850	mV
VOL	Output Low Voltage		-150	0	27	mV
Vcross	Crossing Point Voltage		250	350	550	mV

AC Electrical Characteristics[4]

VDDA = VDD = 3.3V ±5% or 2.5V ±5%
VDDO = 2.5V or 3.3V ±5%
TA = -40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FIN	Input Frequency	Crystal Input		25		MHz
FOUT	Output Frequency	Bank 1 and bank 2		100		MHz
TR/TF	Output Rise/Fall time	20% - 80% HCSL ouput	150	300	450	ps
ODC	Output Duty Cycle	<350MHz output frequencies	48	50	52	%
Tskew	Output-to-Output Skew	Note 5			50	ps
Tlock	PLL Lock Time				20	ms
Tjit(Ø)	RMS Phase Noise	Note 6 100MHz HCSL: Integration range (1.875MHz-20MHz) Integration range (12kHz-20MHz)		 89 222		fs

Notes:
5. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system using crystal input.

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Quartz Crystals and Microchip ICs* application note ANTC207 for further details.

If you need help selecting a suitable crystal for your application, contact Microchip's TCG applications group at: tcghelp@microchip.com.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF below) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the SM802xxx.

The impedance value of the Ferrite Bead (FB) needs to be between 80 Ohms and 240 Ohms with a saturation current >=250mA.

The VDDO1 and VDDO2 pins connect directly to the VDD Plane. All VDD pins on SM802xxx connect to VDD after the power supply filter.

Power Supply Filtering Recommendations

Preferred filter, using Microchip MIC94325 Ripple Blocker:

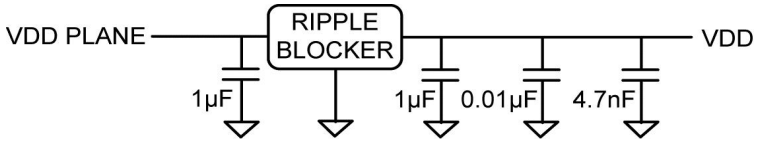


Figure 1. Vdd filter using Microchip MIC94325 Ripple Blocker

Alternative, traditional filter, using a ferrite bead:

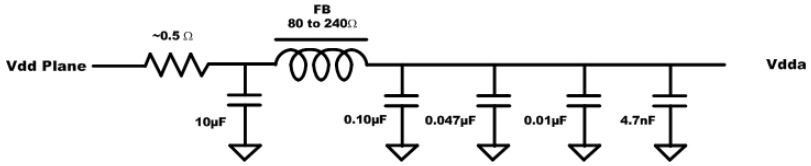


Figure 2. VDDA (Analog) traditional Pi filter

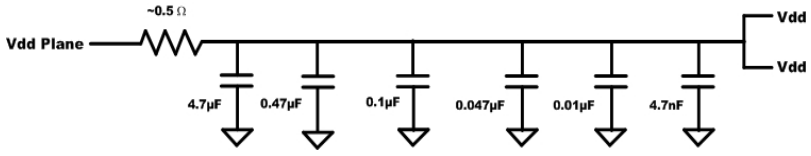


Figure 3. Recommended Power Supply Filtering

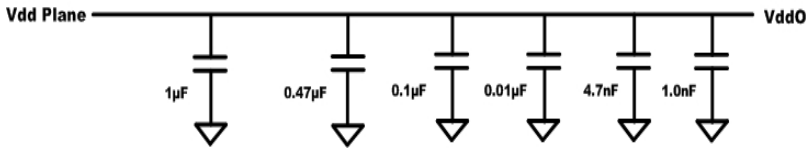


Figure 4. Recommended decoupling for each VDDO

Timing Diagrams

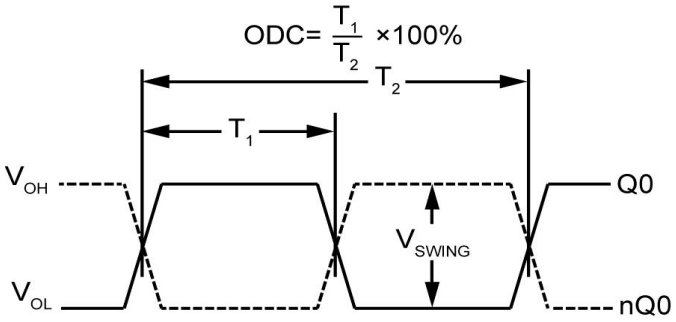


Figure 5. Duty Cycle Timing

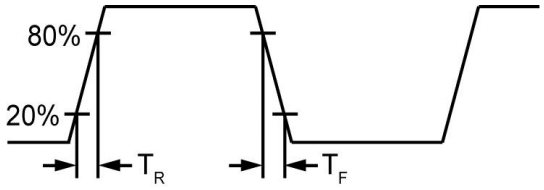


Figure 6. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

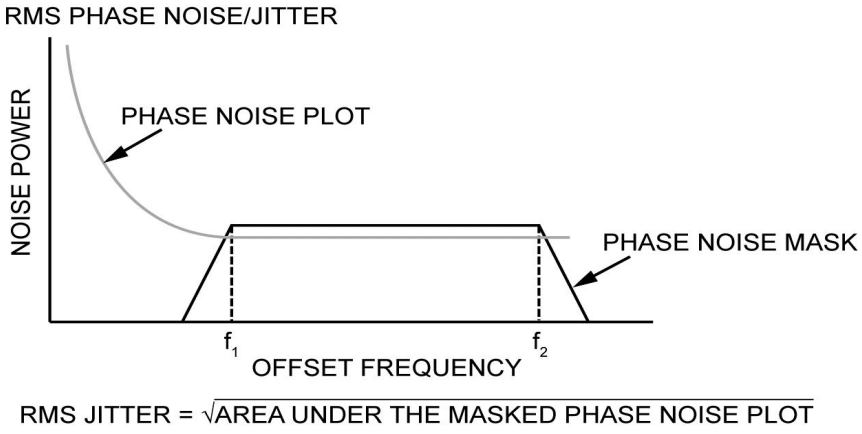


Figure 7. RMS Phase/Noise/Jitter

Crystal Input Interface

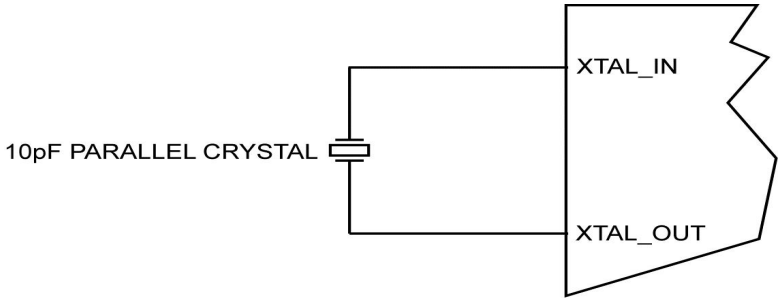


Figure 8. Crystal Input Interface

Output Termination

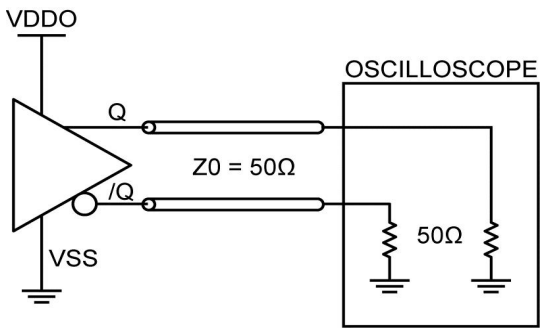


Figure 9. HCSL Output Load and Test Circuit

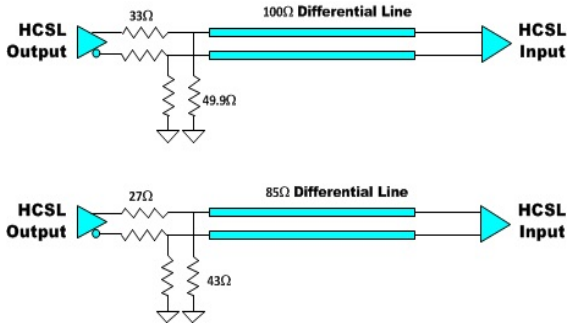


Figure 10. Standard HCSL Termination

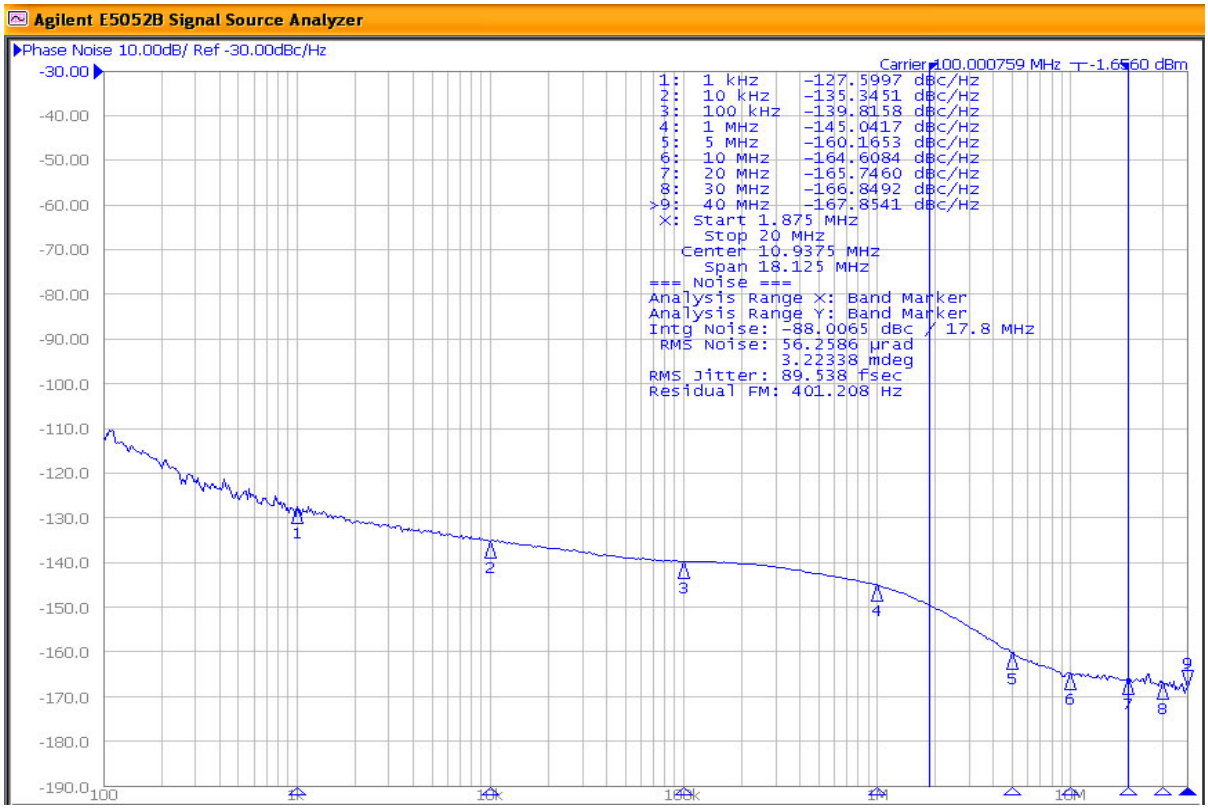


Figure 11. 100MHz HCSL Output 1.875MHz-20MHz 89fs

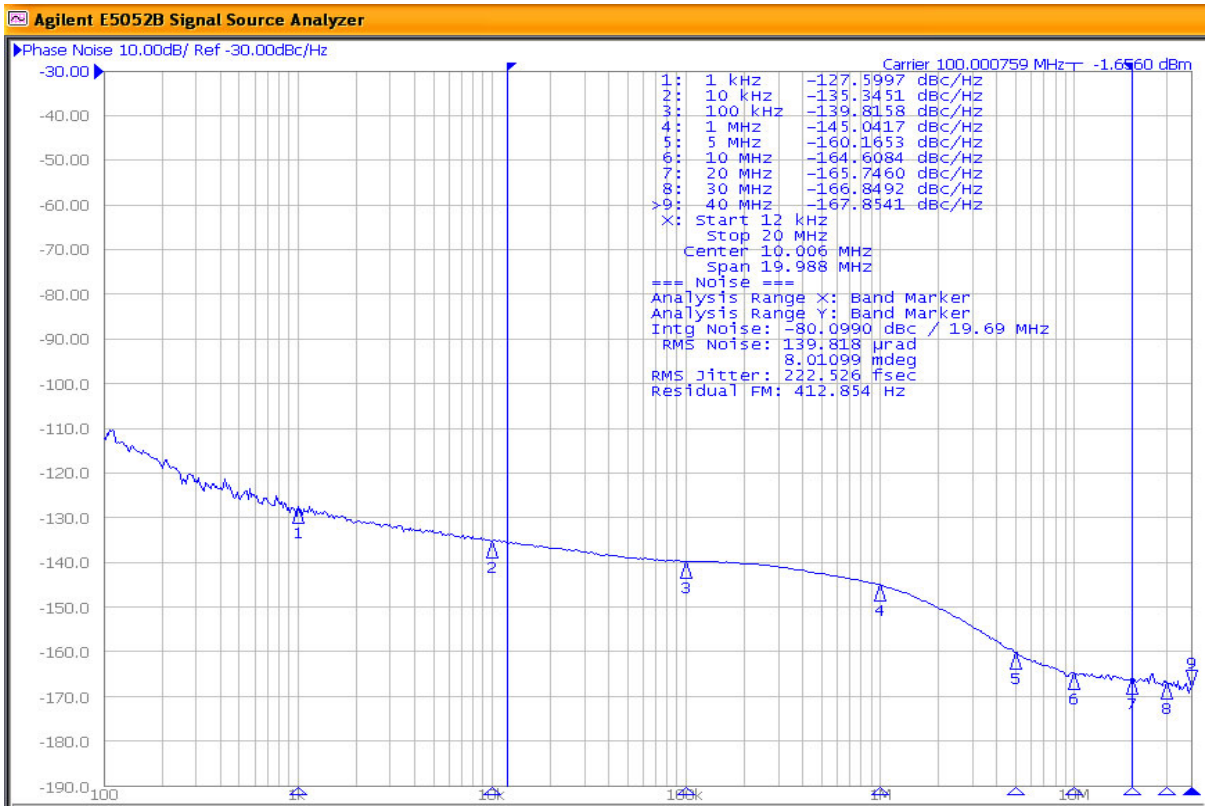
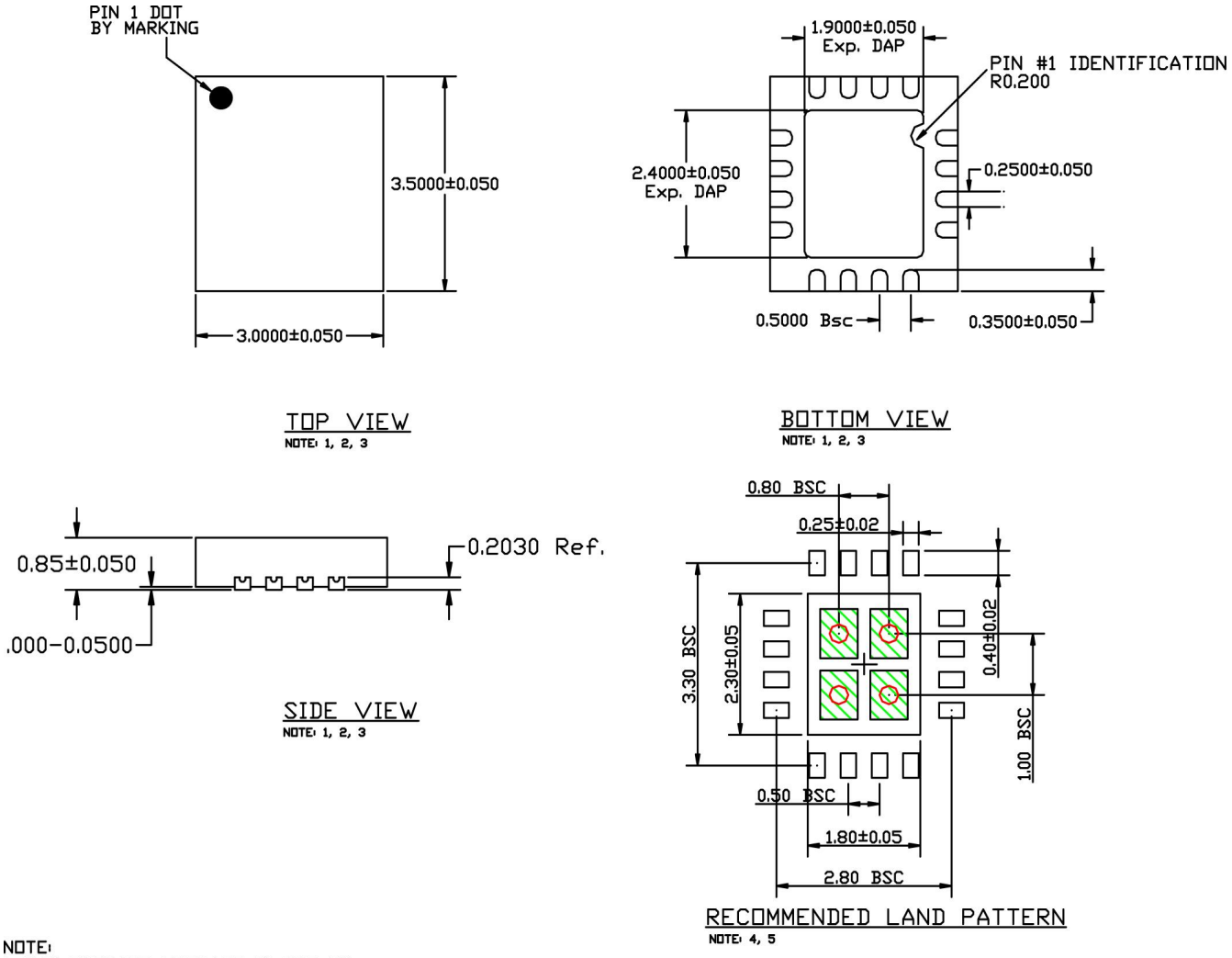


Figure 12. 100MHz HCSL Output 12kHz-20MHz 222fs

Package Information and Recommended Land Pattern for 16-Pin QFN[7]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENT THERMAL VIA. RECOMMENDED DIAMETER IS 0.30 - 0.35 MM AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.80x0.60 MM, 0.20 MM SPACING.

16-Pin QFN (3x3.5 mm)

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.