REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	Add device type 06. Add vendor CAGE 0HGZ7 as source of supply for device types 01 through 04. Editorial changes throughout.	93-09-17	M. A. Frye
C	Changes in accordance with NOR 5962-R143-94.	94-05-10	M. A. Frye
D	Changes in accordance with NOR 5962-R028-95.	94-11-04	M. A. Frye
E	Updated boilerplate to reflect current requirements and made corrections to waveforms. - glg	01-01-17	Raymond Monnin
F	Boilerplate update, part of 5 year review. Corrected generic number on page 2. ksr	06-06-06	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	F	F	F	F															
SHEET	15	16	17	18															

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
27 March 1990

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 1K X 9 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89536**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89536	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	7202	1K X 9-bit parallel FIFO	120 ns
02	7202	1K X 9-bit parallel FIFO	80 ns
03	7202	1K X 9-bit parallel FIFO	65 ns
04	7202	1K X 9-bit parallel FIFO	40 ns
05	7202	1K X 9-bit parallel FIFO	30 ns
06	7202	1K X 9-bit parallel FIFO	20 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	dual-in-line package
Y	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Z	GDFP2-F28	28	flat package
U	CQCC1-N32	32	rectangular chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC output current (I_{OUT}) ..... 50 mA
Ambient storage temperature ..... -65°C to +150°C
Maximum power dissipation (P_D): ..... 1.0 W
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C 1/

1.4 Recommended operating conditions.
Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}) ..... 2.2 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc 2/
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.

2/ 1.5 V undershoots are allowed for 10 ns once per cycle.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-PRF-38535, appendix A) shall be subjected to and pass the Internal Water-Vapor Content test (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	$0.0 \text{ V} \le V_{IN} \le V_{CC}$	1, 2, 3	All	-10	10	µA
Output leakage current	I_{LO}	$0.0 \text{ V} \le V_{OUT} \le V_{CC}$, $\overline{R} \ge V_{IH}$	1, 2, 3	All	-10	10	µA
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 8.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All	2.4		V
Operating supply current	I_{CC1}	$\overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$ $V_{CC} = 5.5$ V f = maximum, outputs open	1, 2, 3	01-03		100	mA
		$V_{CC} = 5.5$ V, f = 20 MHz, outputs open		04-06		140	
Standby power supply current	I_{CC2}	$\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$, outputs open, f = 0 MHz	1, 2, 3	01-03		15	mA
				04-06		20	
Power down current	I_{CC3}	All inputs = $V_{CC} - 0.2$ V, outputs open, f = 0 MHz	1, 2, 3	All		900	µA
Input capacitance	C_{IN}	$V_I = 0$ V , f = 1.0 MHz $T_A = +25°C$, See 4.3.1c	4	All		8	pF
Output capacitance	C_{OUT}	$V_O = 0$ V , f = 1.0 MHz $T_A = +25°C$, See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d.	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C V_{SS} = 0 V 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{RC}	C_L = 30 pF See figures 3 and 4	9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	50		
				05	40		
				06	30		
Access time	t_A		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		40	
				05		30	
				06		20	
Read recovery time	t_{RR}		9, 10, 11	01,02	20		ns
				03	15		
				04-06	10		
Read pulse width	t_{RPW}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Read pulse low to data bus at low-Z	t_{RLZ} 1/		9, 10, 11	01-03	10		ns
				04-06	5.0		
Write pulse low to data bus at low-Z	t_{WLZ} 1/ 2/		9, 10, 11	01,02	20.0		ns
				03	15		
				04	10		
				05,06	5.0		
Data valid from read pulse high	t_{DV}		9, 10, 11	All	5.0		ns
Read pulse high to data bus high-Z	t_{RHZ} 1/		9, 10, 11	01		35	ns
				02,03		30	
				04		25	
				05		20	
				06		15	
Write cycle time	t_{WC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	40		
				06	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write pulse width	t_{WPW}	$C_L = 30$ pF See figures 3 and 4	9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Write recovery time	t_{WR}		9, 10, 11	01,02	20		ns
				03	15		
				04-06	10		
Data setup time	t_{DS}		9, 10, 11	01,02	40		ns
				03	30		
				04	20		
				05	18		
				06	12		
Data hold time	t_{DH}		9, 10, 11	01-03	10		ns
				04-06	0		
Reset cycle time	t_{RSC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	50		
				05	40		
				06	30		
Reset pulse width	t_{RS}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Reset recovery time	t_{RSR}		9, 10, 11	01,02	20		ns
				03	15		
				04-06	10		
Reset setup time	t_{RSS} 1/		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Retransmit cycle time	t_{RTC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	50		
				05	40		
				06	30		
Retransmit pulse width	t_{RT}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Retransmit recovery time	t_{RTR}	$C_L = 30$ pF, See figures 3 and 4.	9, 10, 11	01,02	20		ns
				03	15		
				04-06	10		
Reset to empty flag low	t_{EFL}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		50	
				05		40	
				06		30	
Read low to empty flag low	t_{REF}		9, 10, 11	01-03		60	ns
				04,05		30	
				06		20	
Read high to full flag high	t_{RFF}		9, 10, 11	01-03		60	ns
				04		35	
				05		30	
				06		20	
Write high to empty flag high	t_{WEF}		9, 10, 11	01-03		60	ns
				04		35	
				05		30	
				06		20	
Write low to full flag low	t_{WFF}		9, 10, 11	01-03		60	ns
				04		35	
				05		30	
				06		20	
Reset to half-full and full flag high	t_{HFH} t_{FFH}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		50	
				05		40	
				06		30	
Read/write to $\overline{XO}$ low	t_{XOL}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		40	
				05		30	
				06		20	
Read/write to $\overline{XO}$ high	t_{XOH}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		40	
				05		30	
				06		20	
$\overline{XI}$ pulse width	t_{XI}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
$\overline{XI}$ recovery time	t_{XIR}		9, 10, 11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{XI}$ set-up time	t_{XIS}	C_L = 30 pF, See figures 3 and 4.	9, 10, 11	01-03	15		ns
				04-06	10		
Retransmit setup time	t_{RTS} 1/		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Read pulse width after EF high	t_{RPE}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		
Write low to half-full flag low	t_{WHF}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		50	
				05		40	
				06		30	
Read high to half-full flag high	t_{RHF}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		50	
				05		40	
				06		30	
Write pulse width after FF high	t_{WPF}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	40		
				05	30		
				06	20		

1/ If not tested, shall be guaranteed to the limits specified in table I.

2/ Only applies to read data flow-through mode.

Device types	All	
Case outlines	X, Y, and Z	U
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XI}$	D_0
8	$\overline{FF}$	$\overline{XI}$
9	Q_0	$\overline{FF}$
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	$\overline{R}$	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	$\overline{R}$
19	Q_7	Q_4
20	$\overline{XO}$ / $\overline{HF}$	Q_5
21	$\overline{EF}$	Q_6
22	$\overline{RS}$	Q_7
23	$\overline{FL}$ / $\overline{RT}$	$\overline{XO}$ / $\overline{HF}$
24	D_7	$\overline{EF}$
25	D_6	$\overline{RS}$
26	D_5	$\overline{FL}$ / $\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	---	D_6
30	---	D_5
31	---	D_4
32	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load
Depth expansion/compound expansion mode

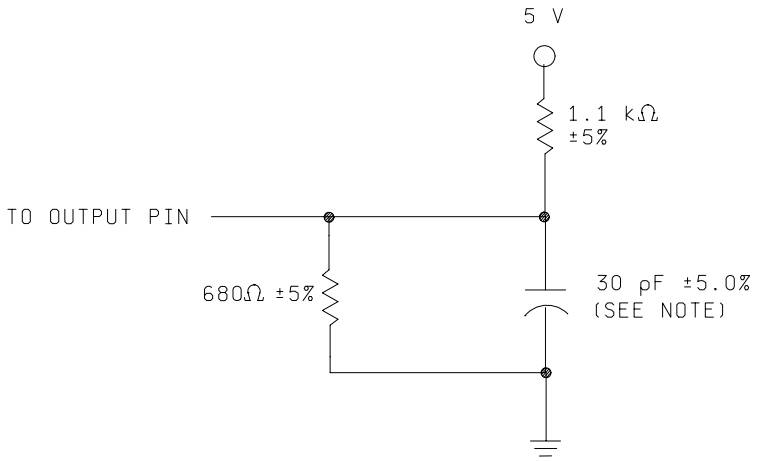
Mode	Inputs			Internal status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	1/	Location zero	Location zero	0	1
Read/write	1	X	1/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

NOTES: $\overline{RS}$ = Reset input, $\overline{FL}$ / $\overline{RT}$ = First load/retransmit, $\overline{EF}$ = Empty flag output,
$\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth tables.

OUTPUT LOAD CIRCUIT (OR EQUIVALENT)

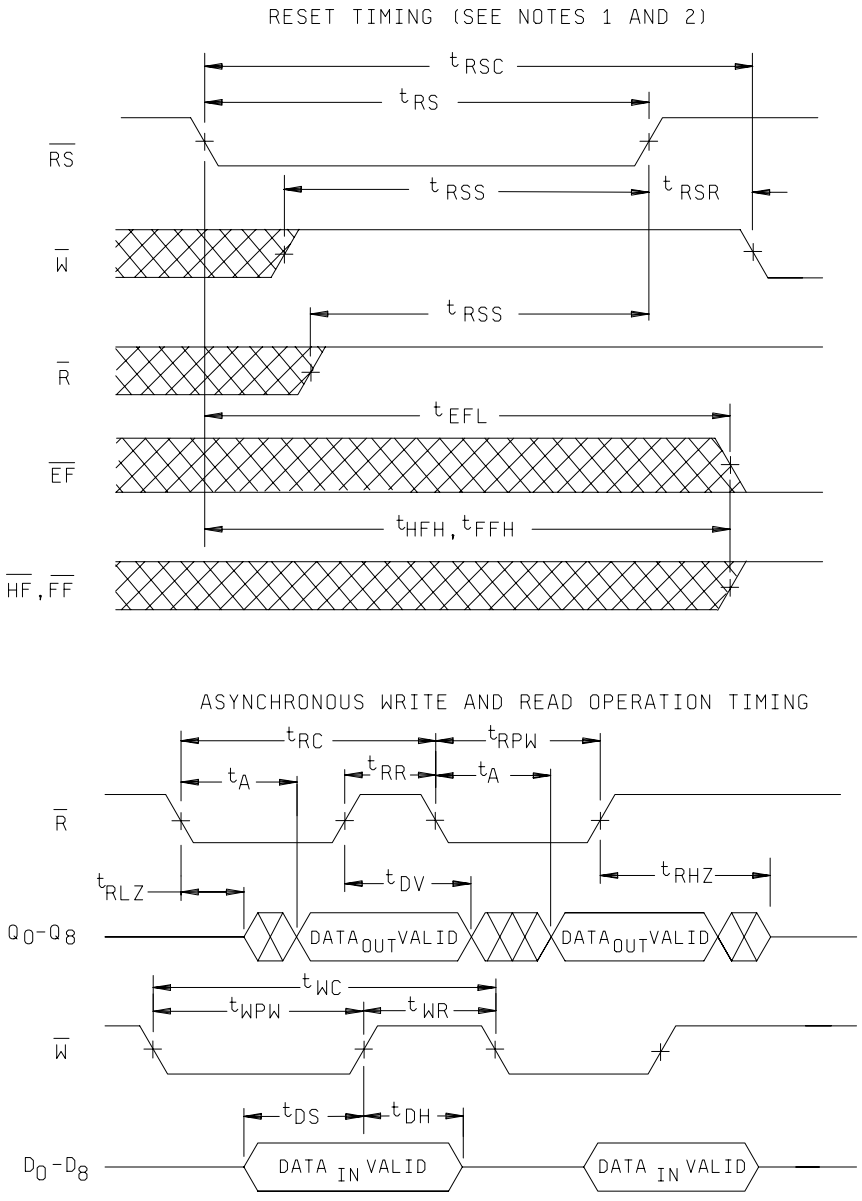


NOTE: C_L includes scope and jig capacitance.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and ac test conditions.

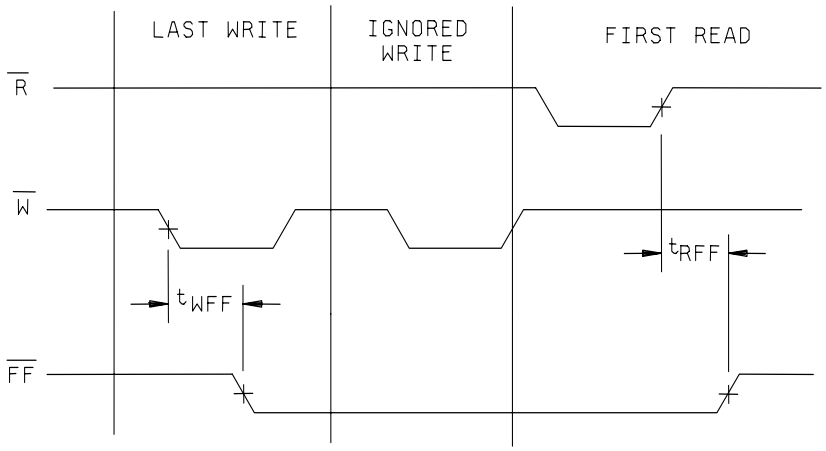


Notes:

1. $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$ may change status during RESET but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

FIGURE 4. Timing waveforms.

FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE TIMING

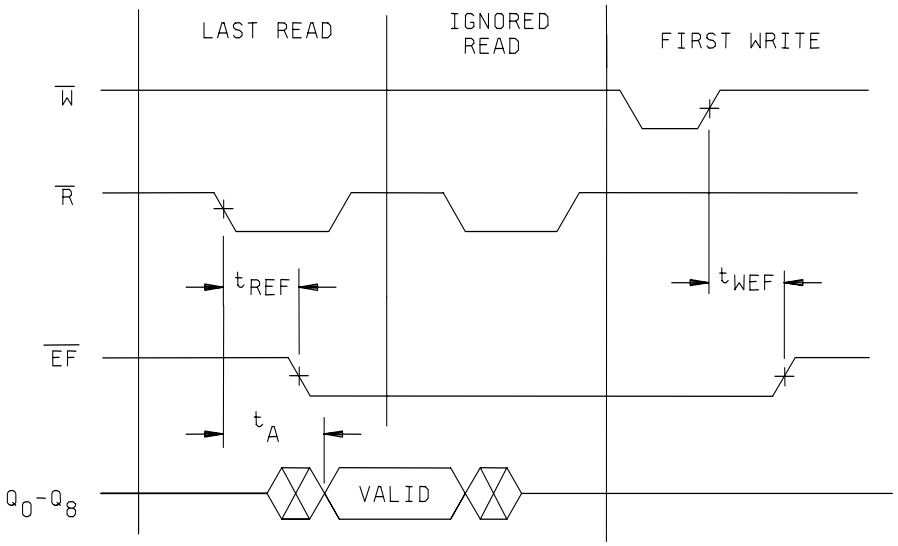
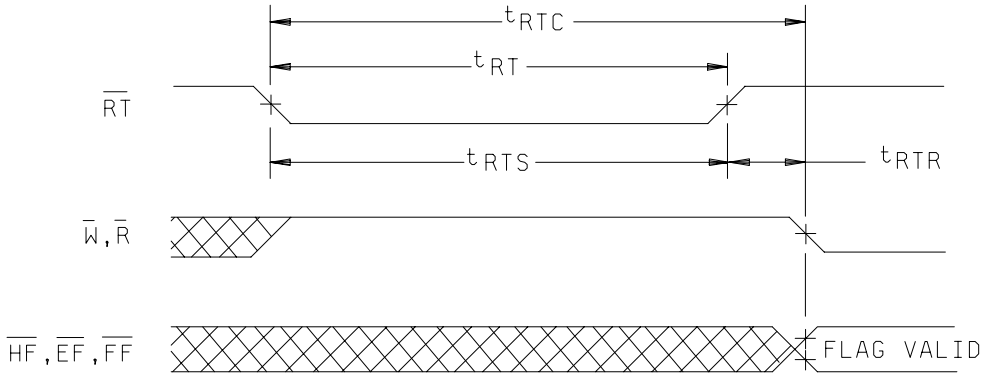
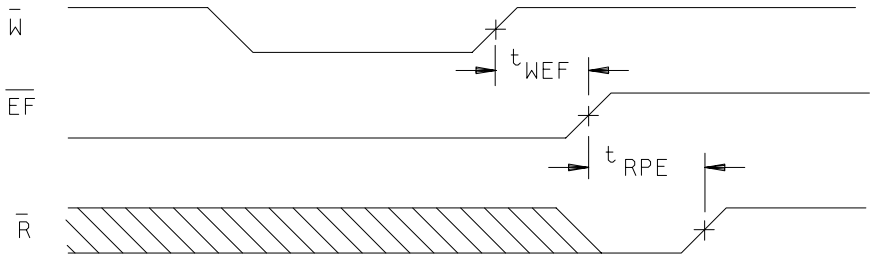


FIGURE 4. Timing waveforms - continued.

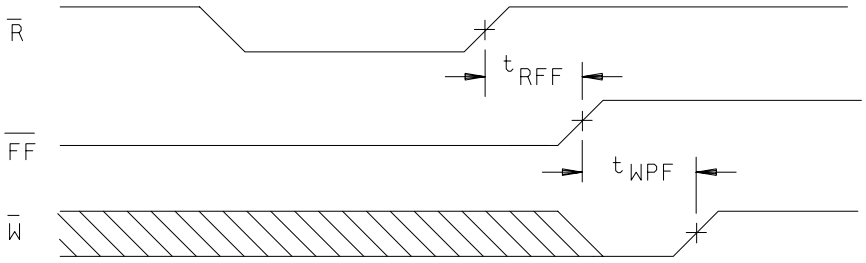
RETRANSMIT TIMING (SEE NOTE 3)



EMPTY FLAG TIMING



FULL FLAG TIMING



Note 3: $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$ may change status during RETRANSMIT but flags will be valid at t_{RTC}.

FIGURE 4. Timing waveforms - continued.

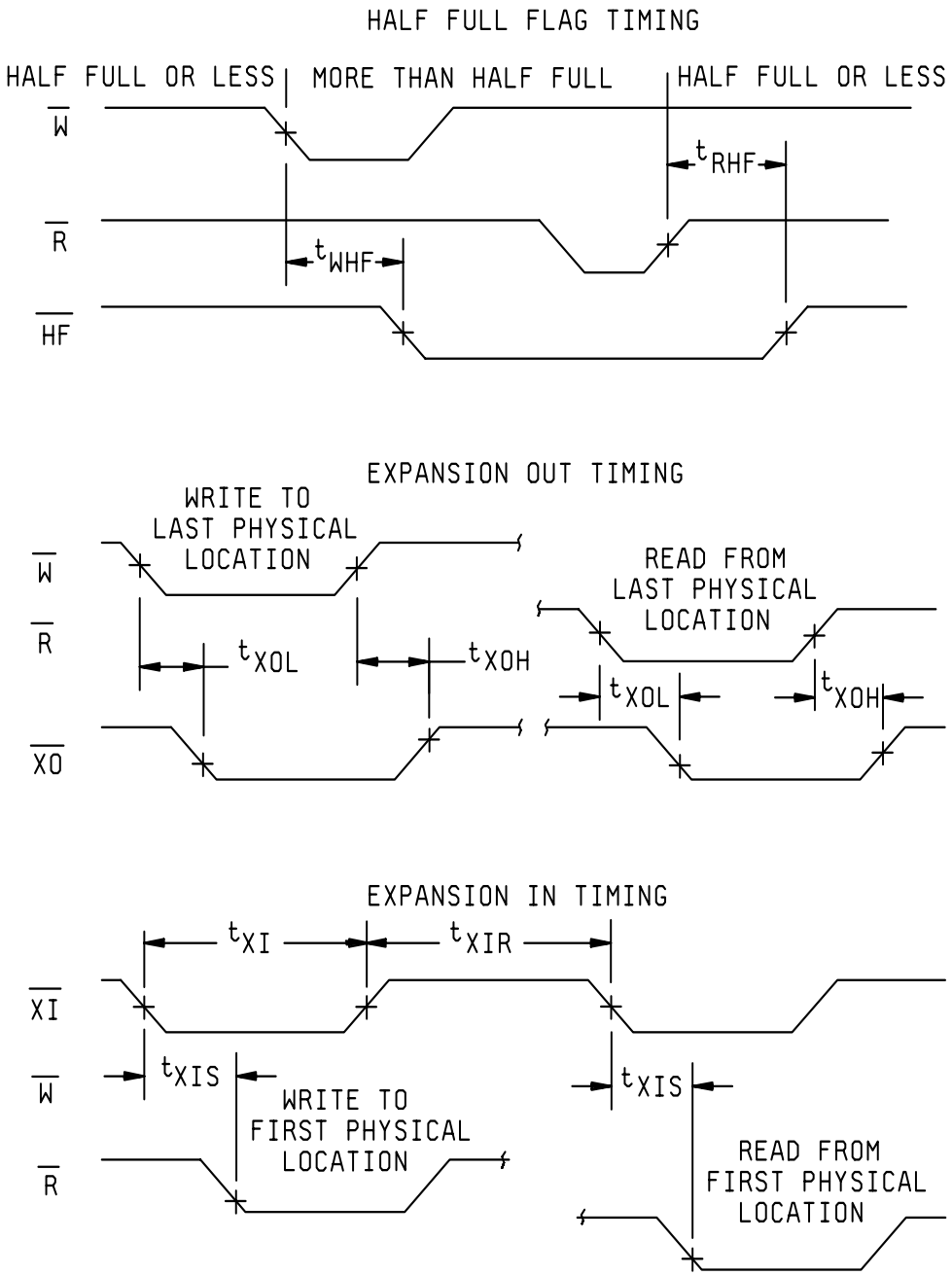


FIGURE 4. Timing waveforms - continued.

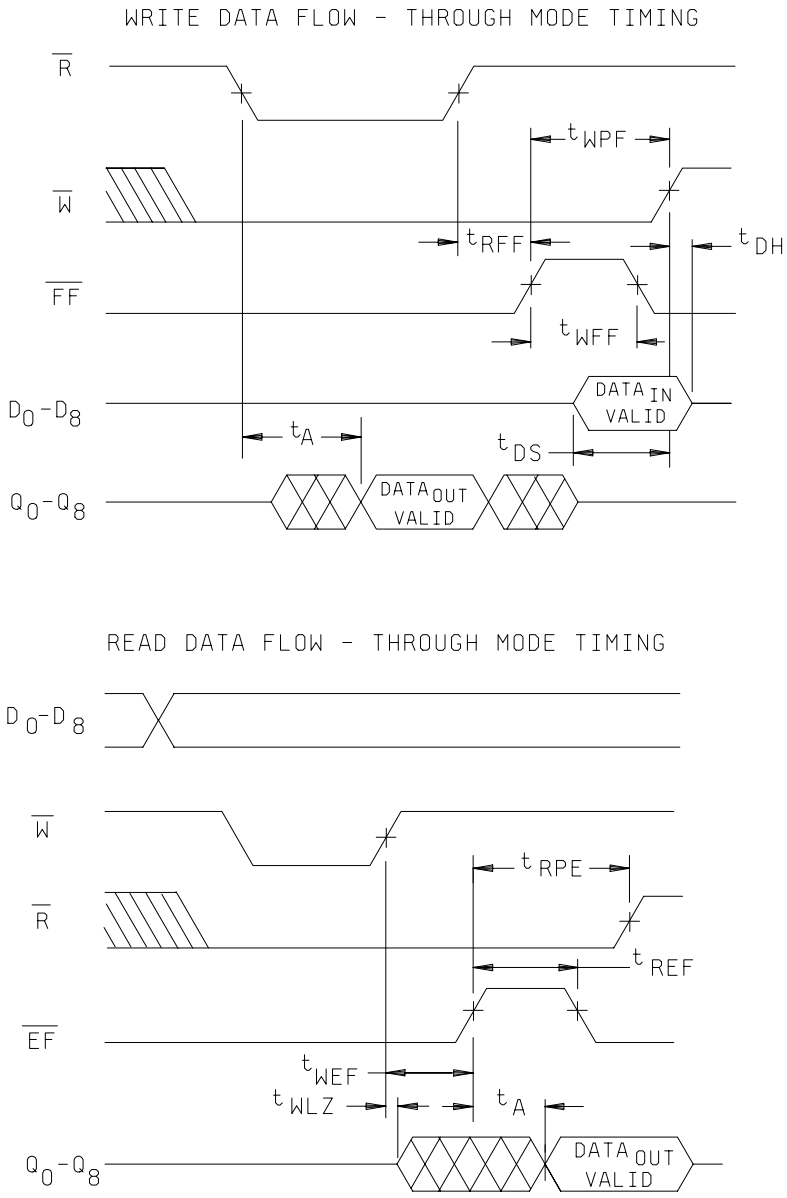


FIGURE 4. Timing waveforms - continued.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after any design or process changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements. *

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* Indicates PDA applies to subgroup 1.
** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-06

Approved sources of supply for SMD 5962-89536 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8953601XA	3/	IDT7202LA120TDB
	3/	MM1P-67202AL-50/883
5962-8953601YA	3/	IDT7202LA120DB
5962-8953601ZA	3/	IDT7202LA120XEB
5962-8953601UA	3/	IDT7202LA120LB
	3/	MM4J-6702AL-50/883
5962-8953602XA	3/	IDT7202LA80TDB
	3/	MM1P-67202AL-50/883
5962-8953602YA	3/	IDT7202LA80DB
5962-8953602ZA	3/	IDT7202LA80XEB
5962-8953602UA	3/	IDT7202LA80LB
	3/	MM4J-67202AL-50/883
5962-8953603XA	3/	IDT7202LA65TDB
	3/	MM1P-67202AL-50/883
5962-8953603YA	3/	IDT7202LA65DB
5962-8953603ZA	3/	IDT7202LA65XEB
5962-8953603UA	3/	IDT7202LA65LB
	3/	MM4J-67202AL-50/883
5962-8953604XA	3/	IDT7202LA40TDB
	3/	MM1P-67202AL-40/883
5962-8953604YA	3/	IDT7202LA40DB
5962-8953604ZA	3/	IDT7202LA40XEB
5962-8953604UA	3/	IDT7202LA40LB
	3/	MM4J-67202AL-40/883
5962-8953605XA	61772	IDT7202LA30TDB
	3/	MM1P-67202AL-30/883
5962-8953605YA	61772	IDT7202LA30DB
5962-8953605ZA	3/	IDT7202LA30XEB
5962-8953605UA	61772	IDT7202LA30LB
	3/	MM4J-67202AL-30/883
5962-8953606XA	61772	IDT7202LA20TDB
5962-8953606YA	61772	IDT7202LA20DB
5962-8953606ZA	3/	IDT7202LA20XEB
5962-8953606UA	61772	IDT7202LA20LB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.