200-MHz CMOS OPERATIONAL AMPLIFIER

Check for Samples: OPA2356-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Unity-Gain Bandwidth: 450 MHz
- Wide Bandwidth: 200 MHz GBW
- High Slew Rate: 360 V/s
- Low Noise: 5.8 nV/√Hz
- Excellent Video Performance
  - Differential Gain: 0.02%
  - Differential Phase: 0.05°
  - 0.1-dB Gain Flatness: 75 MHz
- Input Range Includes Ground
- Rail-To-Rail Output (Within 100 mV)
- Low Input Bias Current: 3 pA
- Thermal Shutdown
- Single-Supply Operating Range: 2.5 V to 5.5 V

APPLICATIONS

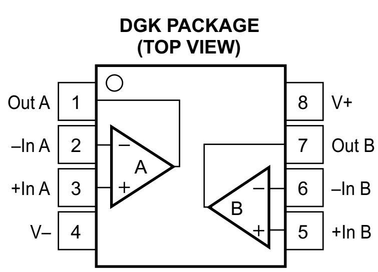
- Video Processing
- Ultrasound
- Optical Networking, Tunable Lasers
- Photodiode Transimpedance Amplifiers
- Active Filters
- High-Speed Integrators
- Analog-To-Digital (A/D) Converter Input Buffers
- Digital-To-Analog (D/A) Converter Output Amplifiers
- Barcode Scanners
- Communications

DESCRIPTION

The OPA2356-Q1 is a high-speed voltage-feedback CMOS operational amplifier designed for video and other applications requiring wide bandwidth. The OPA2356-Q1 is unity gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.05°. Quiescent current is only 8.3 mA.

OPA2356-Q1 is optimized for operation on single or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). Common-mode input range for the OPA2356-Q1 extends 100 mV below ground and up to 1.5 V from V+. The output swing is within 100 mV of the rails, supporting wide dynamic range.

The OPA2356-Q1 is available in the VSSOP-8 package and is specified over the –40°C to 125°C range.



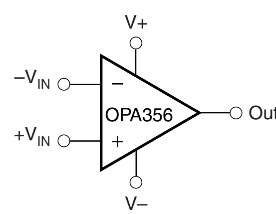


Table 1. ORDERING INFORMATION(1)(2)

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	OPA2356AQDGKRQ1	AYIZ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VALUE		UNIT
		MIN	MAX	
V_S	Supply voltage, V+ to V–		7.5	V
V_{IN}	Signal input terminals voltage range(2)	–0.5	(V+ + 0.5)	V
	V– current(2)		10	mA
	Output short-circuit duration(3)	Continuous		
θ_{JA}	Thermal impedance, junction to free air(4)		150	°C/W
T_A	Operating free-air temperature range	–40	125	°C
T_{STG}	Storage temperature range	–65	150	°C
T_J	Junction temperature		160	°C
T_{LEAD}	Lead temperature (soldering, 10 s)		300	°C
ESD Ratings	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B		750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground one amplifier per package.
(4) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.7	5.5	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

V_S = 2.7 V to 5.5 V, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage		V_S = 5 V, V_{CM} = V– + 0.8 V	25°C		±2	±9	mV
				Full range			±15	
$\Delta V_{OS}/\Delta T$	Offset voltage drift over temperature			Full range		±7		µV/°C
PSRR	Offset voltage drift vs power supply		V_S = 2.7 V to 5.5 V, V_{CM} = V_S / 2 – 0.15 V	25°C		±80	±350	µV/V
I_B	Input bias current			25°C		3	±50	pA
I_{OS}	Input offset current			25°C		±1	±50	pA
V_n	Input voltage noise density		f = 1 MHz	25°C		5.8		nV/√Hz
I_n	Input current noise density		f = 1 MHz	25°C		50		fA/√Hz
V_{CM}	Input common-mode voltage range			25°C	V– – 0.1		V+ – 1.5	V
CMRR	Input common-mode rejection ratio		V_S = 5.5 V, –0.1 V < V_{CM} < 4 V	25°C	66	80		dB
				Full range	66			
Z_{ID}	Differential input impedance			25°C		10^{13} || 1.5		Ω || pF
Z_{ICM}	Common-mode input impedance			25°C		10^{13} || 1.5		Ω || pF
A_{OL}	Open-loop gain		OPA356: V_S = 5 V, 0.3 V < V_O < 4.7 V	25°C	84	92		dB
				Full range	80			
			OPA2356: V_S = 5 V, 0.4 V < V_O< 4.6 V	Full range	80			
f_{-3dB}	Small-signal bandwidth		G = 1, V_O = 100 mVp-p, R_F = 0 Ω	25°C		450		MHz
			G = 2, V_O = 100 mVp-p, R_L = 50 Ω			100		
			G = 2, V_O = 100 mVp-p, R_L = 150 Ω			170		
			G = 2, V_O = 100 mVp-p, R_L = 1 kΩ			200		
GBW	Gain-bandwidth product		G = 10, R_L = 1 kΩ	25°C		200		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness		G = 2, V_O = 100 mVp-p, R_F = 560 Ω	25°C		75		MHz
SR	Slew rate		V_S = 5 V, G = 2, 4-V output step	25°C		300 –360		V/µs
t_{rf}	Rise-and-fall time		G = 2, V_O = 200 mVp-p, 10% to 90%	25°C		2.4		ns
			G = 2, V_O = 2 Vp-p, 10% to 90%			8		
t_{settle}	Settling time	0.1%	V_S = 5 V, G = 2, 2-V output step	25°C		30		ns
		0.01%		25°C		120		
	Overload recovery time		V_{IN} × Gain = V_S	25°C		8		ns
	Harmonic distortion	Second harmonic	G = 2, f = 1 MHz, VO = 2 Vp-p, R_L = 200 Ω	25°C		–81		dBc
		Third harmonic		25°C		–93		
	Differential gain error		NTSC, R_L = 150 Ω	25°C		0.02		%
	Differential phase error		NTSC, R_L = 150 Ω	25°C		0.05		°
	Voltage output swing from rail		V_S = 5 V, R_L = 150 Ω, A_{OL} > 84 dB	25°C		0.2	0.3	V
			V_S = 5 V, R_L = 1 kΩ			0.1		
			V_S = 5 V, R_L = 50 Ω			0.4	0.6	

(1) Full range T_A = –40°C to 125°C

ELECTRICAL CHARACTERISTICS (continued)

V_S = 2.7 V to 5.5 V, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

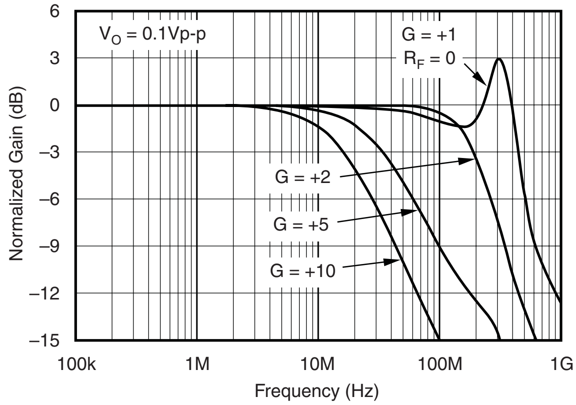
PARAMETER			TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
I_O	Output current (2)	Continuous		25°C	±60			mA
		Peak	V_S = 5 V		±100			
			V_S = 3 V			±80		
	Short-circuit current			25°C		250 –200		mA
	Closed-loop output impedance			25°C		0.02		Ω
I_Q	Quiescent current		V_S = 5 V, I_O = 0	25°C		8.3	11	mA
				Full range			14	
	Thermal shutdown junction temperature		Shutdown	25°C		160		°C
			Reset from shutdown			140		

(2) See typical characteristic graph *Output Voltage Swing vs Output Current*.

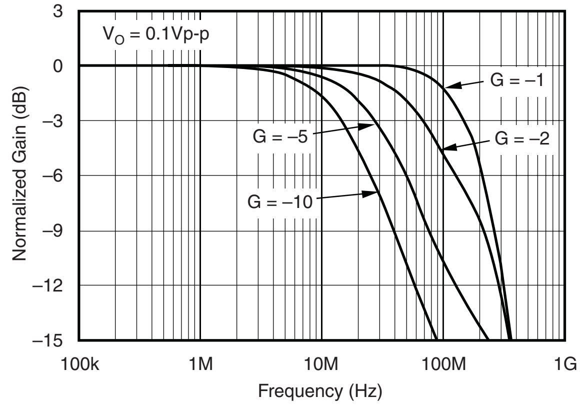
TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

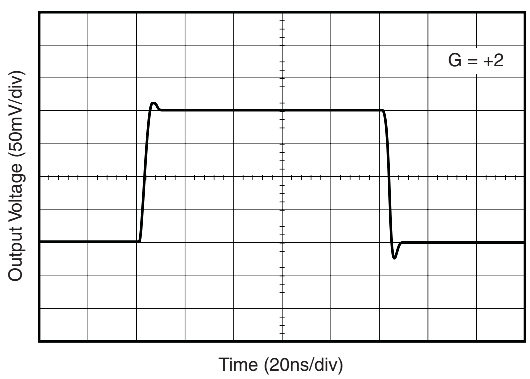
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



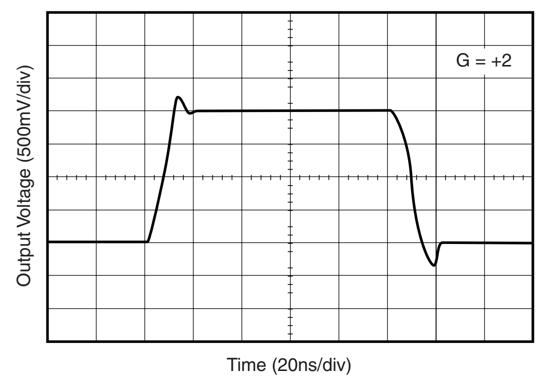
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



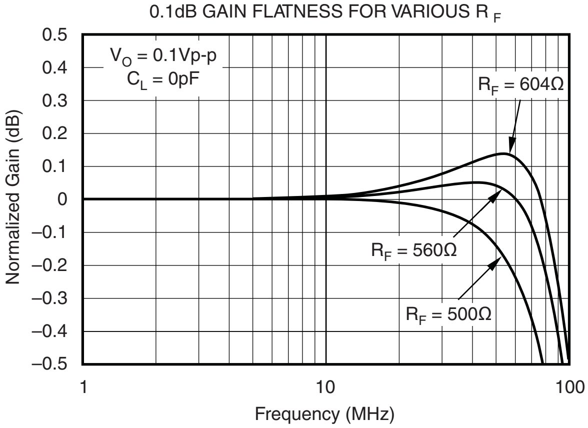
NON-INVERTING SMALL-SIGNAL STEP RESPONSE



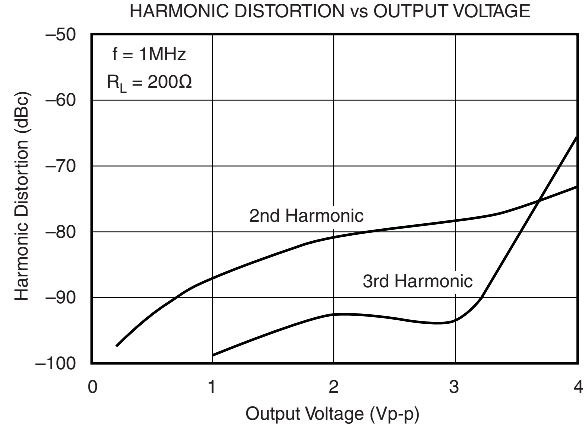
NON-INVERTING LARGE-SIGNAL STEP RESPONSE



0.1dB GAIN FLATNESS FOR VARIOUS R F



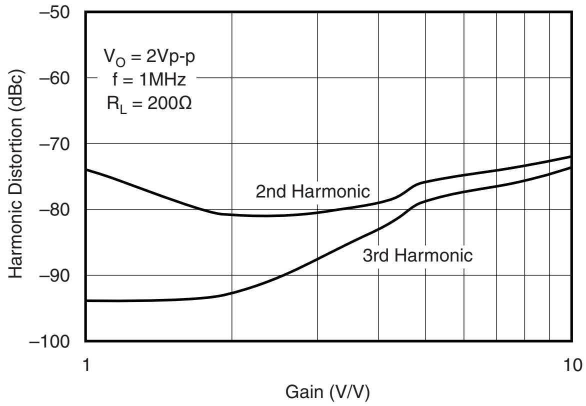
HARMONIC DISTORTION vs OUTPUT VOLTAGE



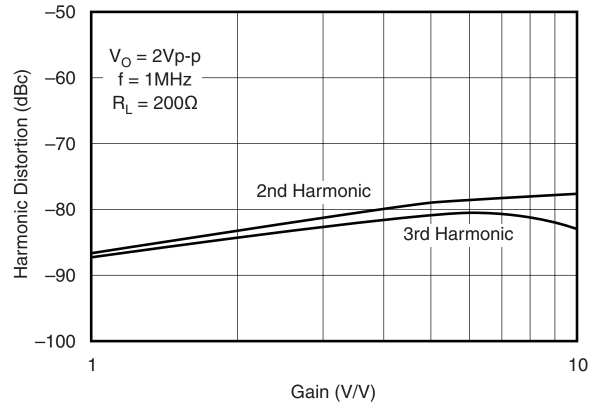
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

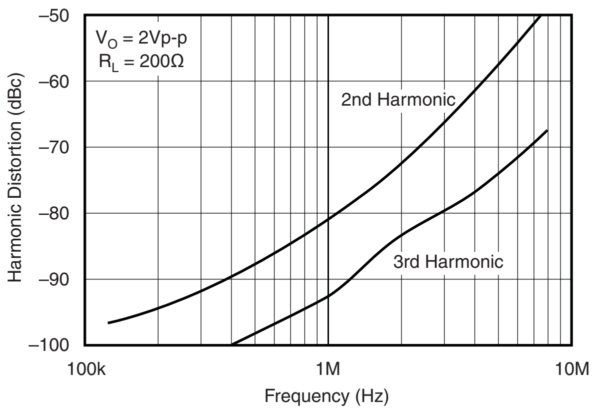
HARMONIC DISTORTION vs NON-INVERTING GAIN



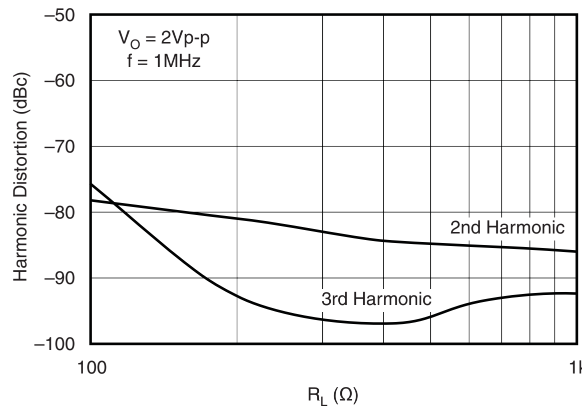
HARMONIC DISTORTION vs INVERTING GAIN



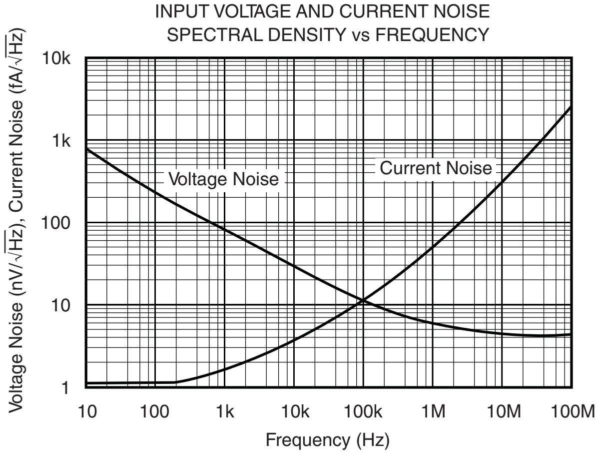
HARMONIC DISTORTION vs FREQUENCY



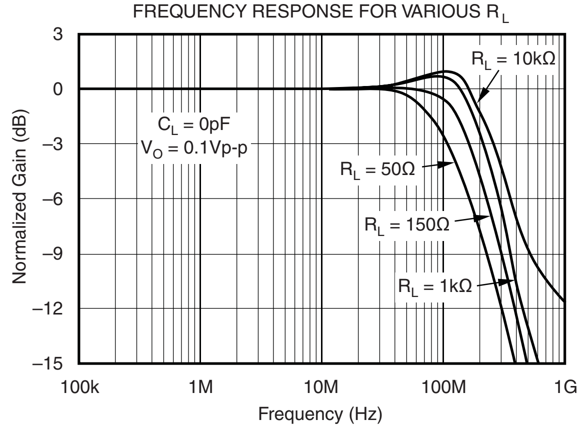
HARMONIC DISTORTION vs LOAD RESISTANCE



INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



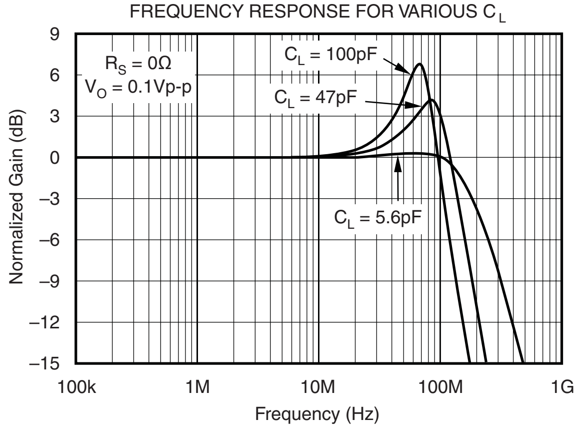
FREQUENCY RESPONSE FOR VARIOUS R_L



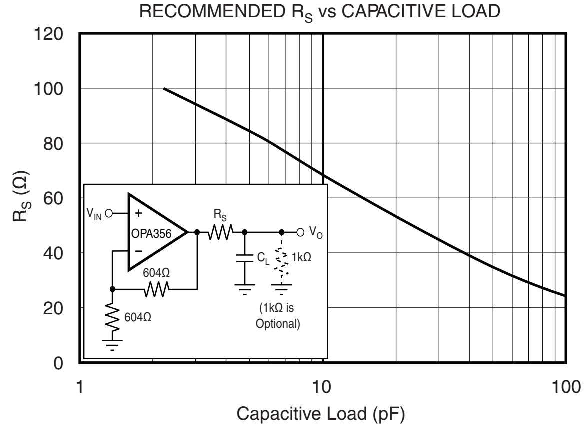
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

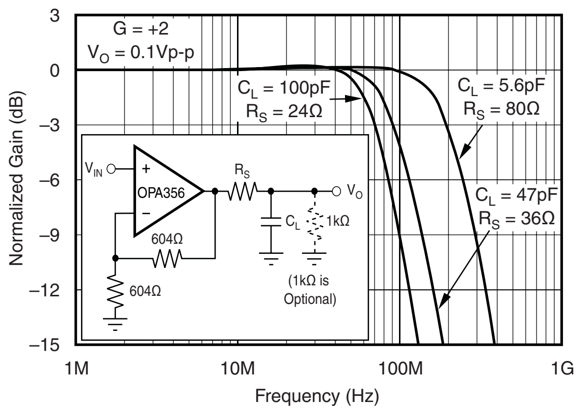
FREQUENCY RESPONSE FOR VARIOUS C_L



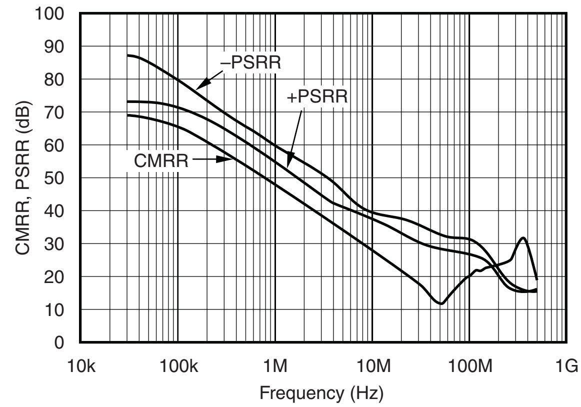
RECOMMENDED R_S vs CAPACITIVE LOAD



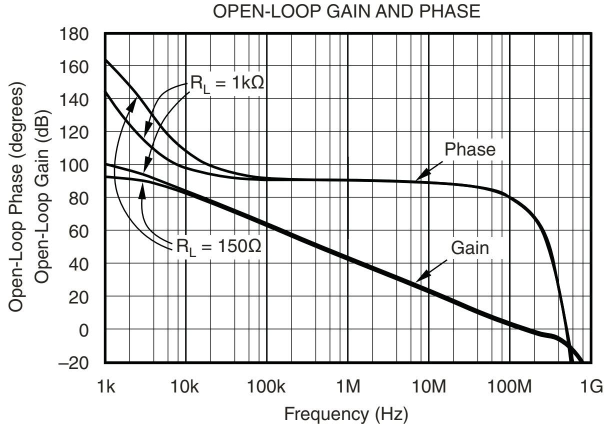
FREQUENCY RESPONSE vs CAPACITIVE LOAD



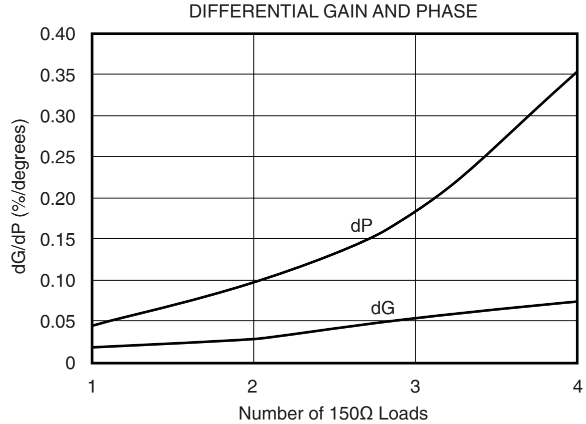
COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OPEN-LOOP GAIN AND PHASE



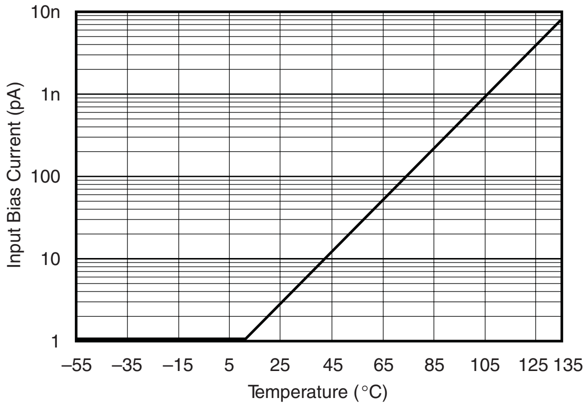
COMPOSITE VIDEO DIFFERENTIAL GAIN AND PHASE



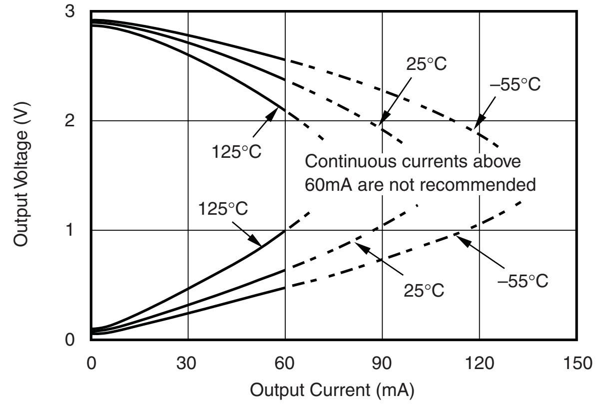
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

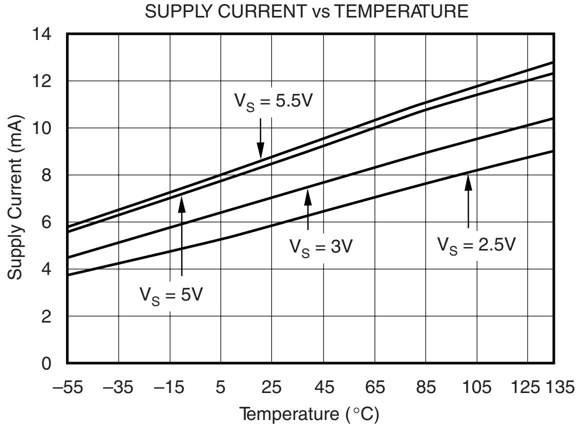
INPUT BIAS CURRENT vs TEMPERATURE



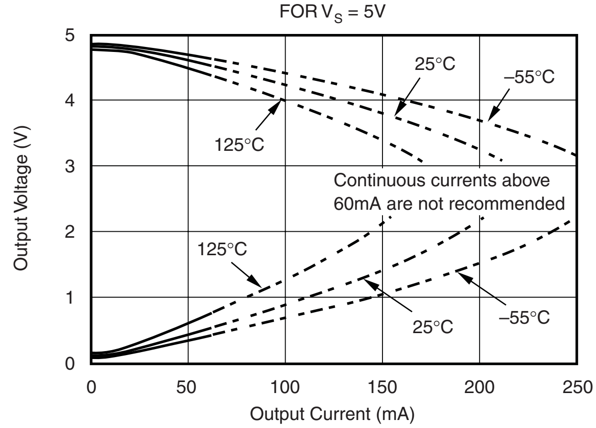
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT FOR V_S = 3V



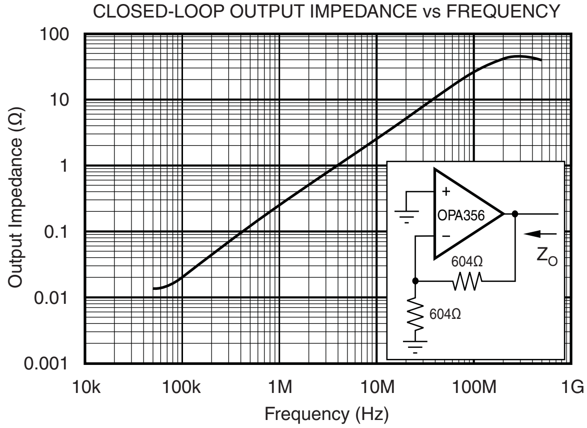
SUPPLY CURRENT vs TEMPERATURE



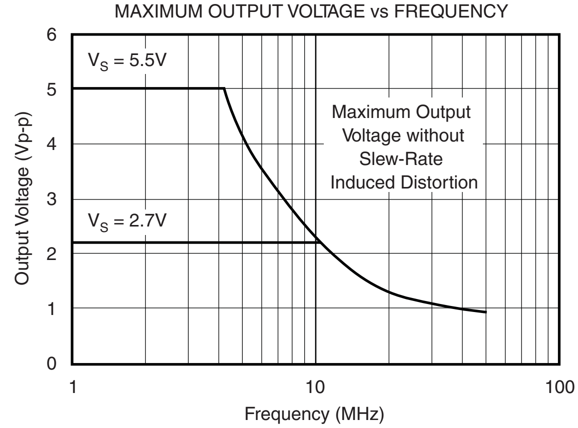
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT FOR V_S = 5V



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



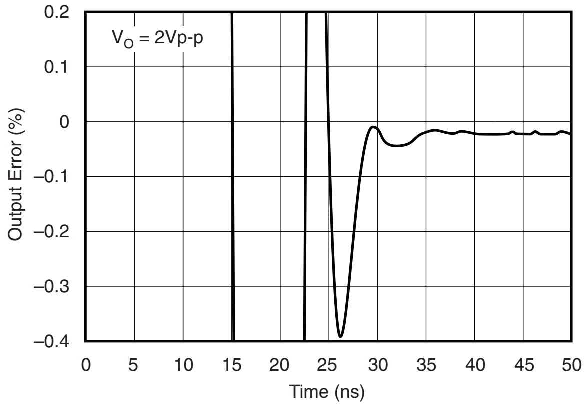
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



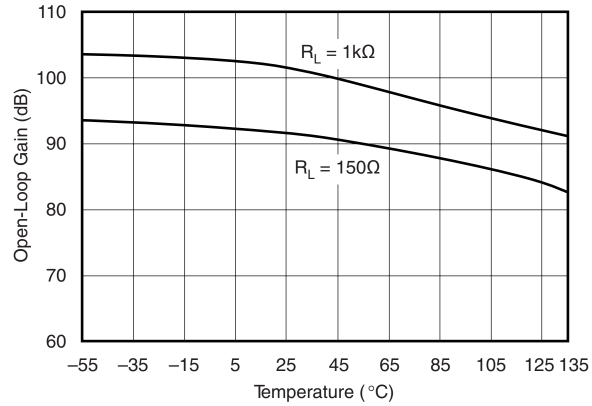
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

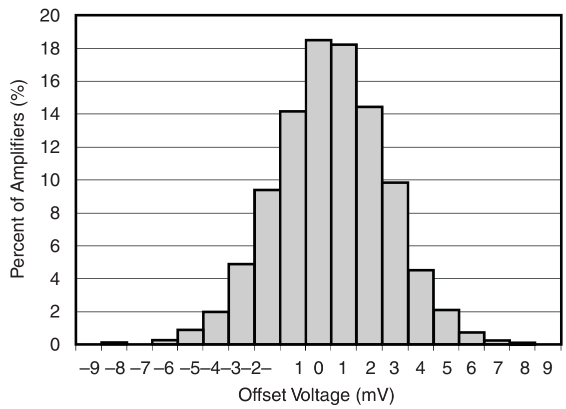
OUTPUT SETTLING TIME TO 0.1%



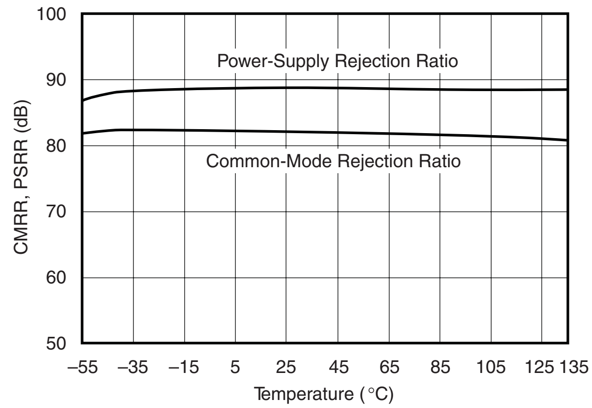
OPEN-LOOP GAIN vs TEMPERATURE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE



APPLICATION INFORMATION

The OPA2356-Q1 is a CMOS high-speed voltage-feedback operational amplifier designed for video and other general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 360-V/μs slew rate, but it is unity-gain stable and can be operated as a 1-V/V voltage follower.

Its input common-mode voltage range includes ground, allowing the OPA2356-Q1 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

PCB Layout

Good high-frequency PC board layout techniques should be employed for the OPA2356-Q1. Generous use of ground planes, short direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean, stable operation. Large areas of copper also provide a means of dissipating heat that is generated within the amplifier in normal operation.

Sockets are definitely not recommended for use with any high-speed amplifier.

A 10-μF ceramic bypass capacitor is the minimum recommended value; adding a 1-μF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

Operating Voltage

The OPA2356-Q1 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Output Drive

The OPA2356-Q1 output stage is capable of driving a standard back-terminated 75-Ω video cable. By back-terminating a transmission line, it does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; it presents only a 150-Ω resistive load to the OPA2356-Q1 output.

The output stage can supply high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA2356-Q1 from dangerously high junction temperatures. At 160°C, the protection circuit will shut down the amplifier. Normal operation will resume when the junction temperature cools to below 140°C.

NOTE

It is not recommended to run a continuous dc current in excess of ±60 mA. See the Output Voltage Swing vs Output Current graph in the Typical Characteristics section of this data sheet.

Input and ESD Protection

All OPA2356-Q1 pins are static protected with internal ESD protection diodes tied to the supplies, as shown in Figure 1. These diodes provide overdrive protection if the current is externally limited to 10 mA by the source or by a resistor.

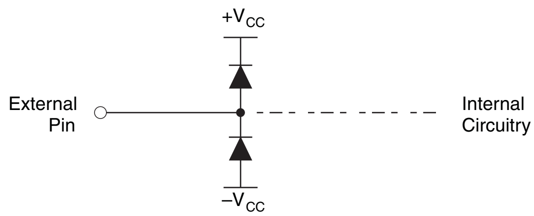


Figure 1. Internal ESD Protection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2356AQDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

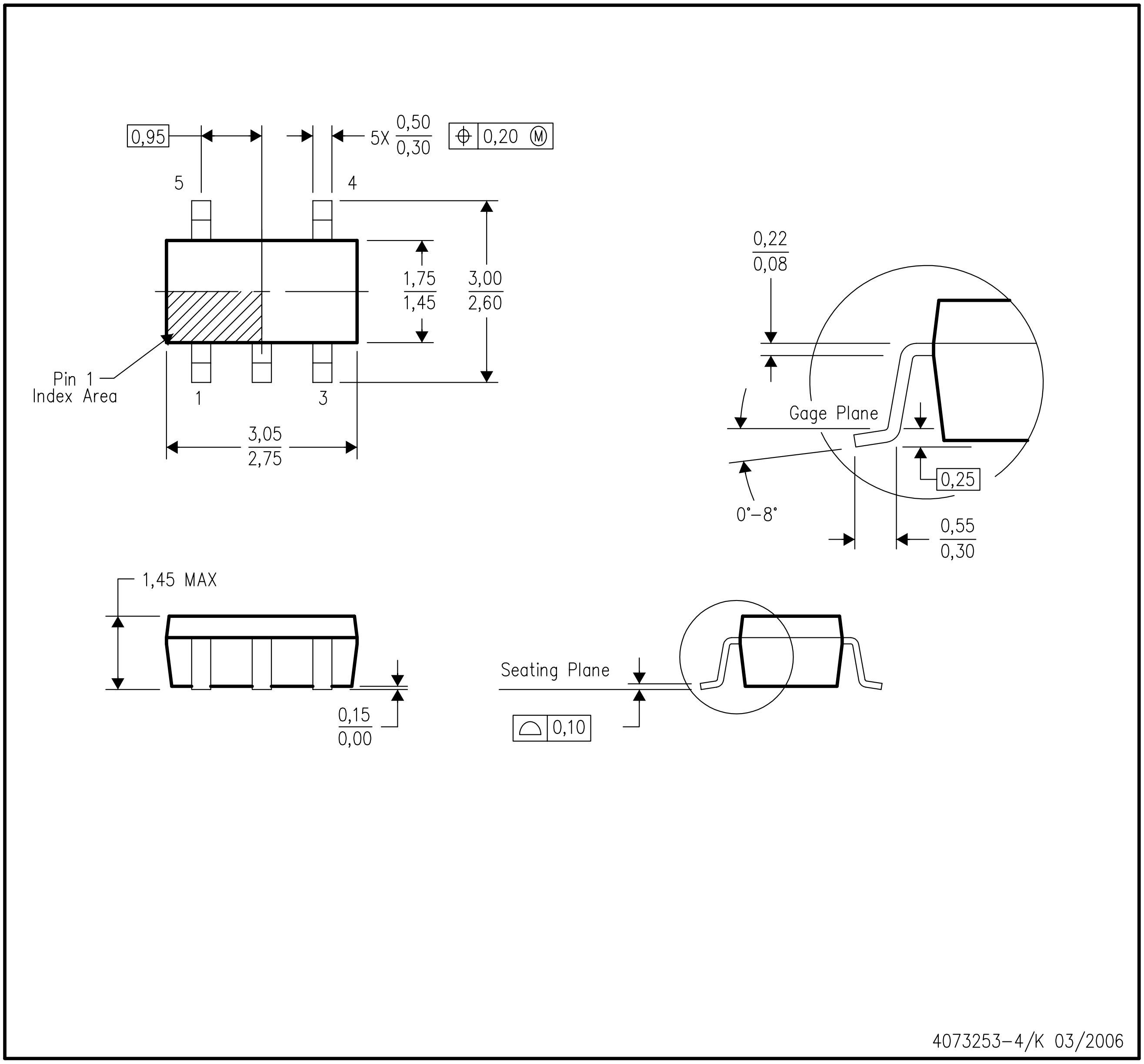
OTHER QUALIFIED VERSIONS OF OPA2356-Q1 :

- Catalog: OPA2356

NOTE: Qualified Version Definitions:

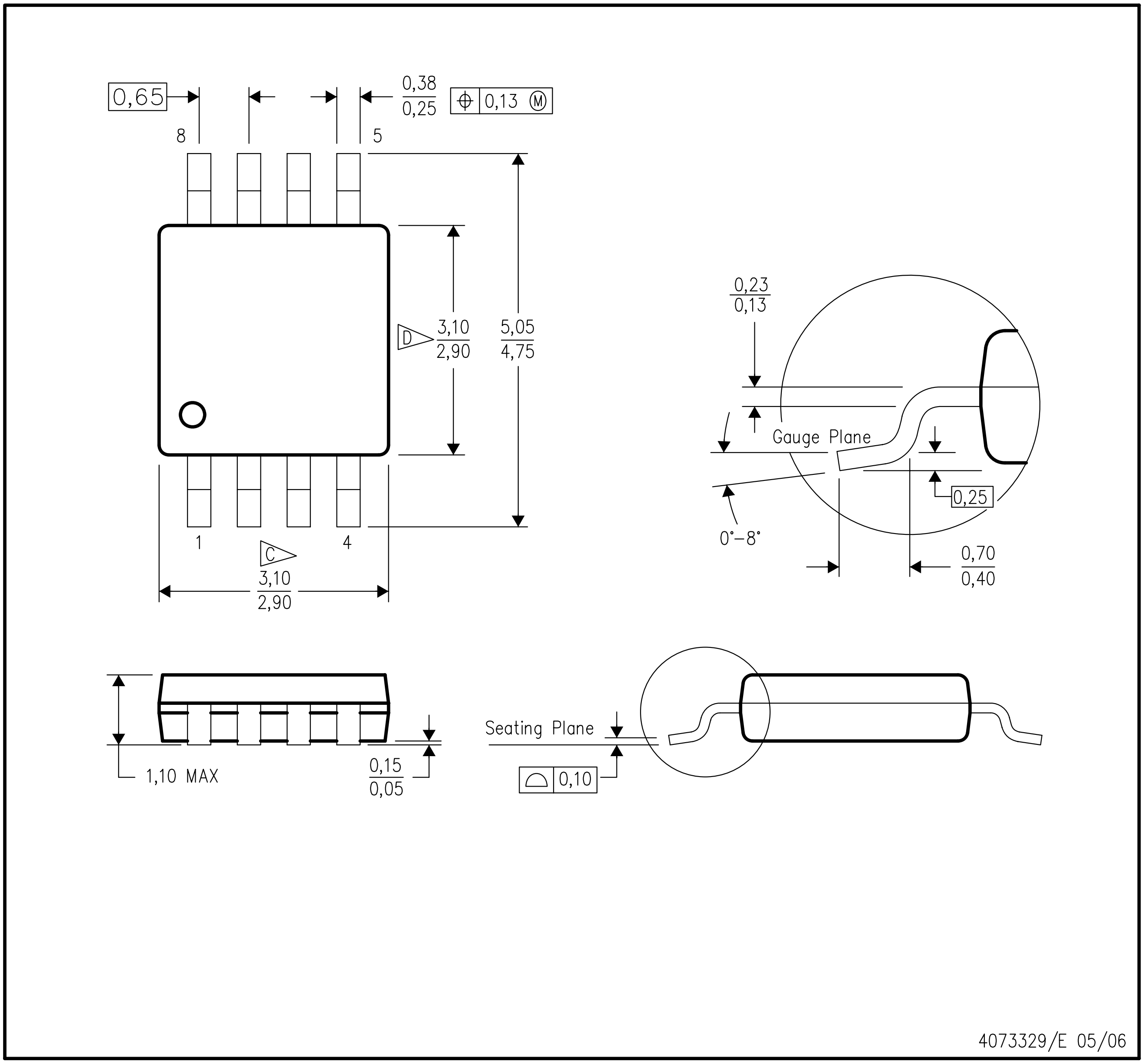
- Catalog - TI's standard catalog product

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.