



54F/74F543 Octal Registered Transceiver

General Description

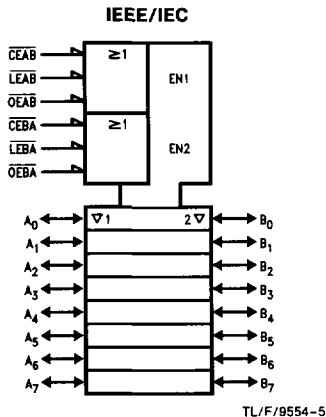
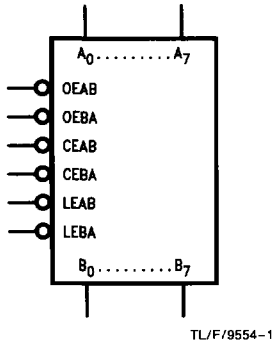
The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil).

Features

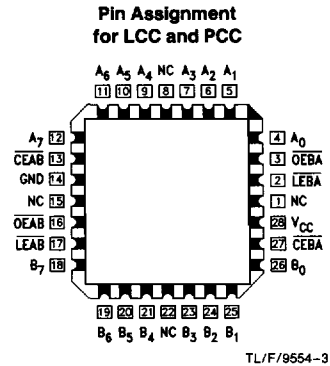
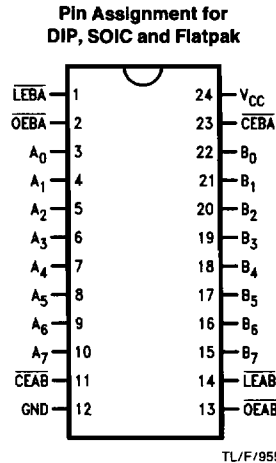
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil)
- B outputs sink 64 mA (48 mA Mil)
- 300 mil slim package

Ordering Code: See Section 5

Logic Symbols



Connection Diagrams



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{CEAB}	A-to-B Enable Input (Active LOW)	1.0/2.0	20 μ A/ -1.2 mA
\overline{CEBA}	B-to-A Enable Input (Active LOW)	1.0/2.0	20 μ A/ -1.2 mA
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
A_0-A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs	3.5/1.083	70 μ A/ -650 μ A
B_0-B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs	150/40 (33.8) 3.5/1.083	-3 mA/24 mA (20 mA) 70 μ A/ -650 μ A
		600/106.6 (80)	-12 mA/64 mA (48 mA)

Functional Description

The 'F543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{OEAB}) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7 , as indicated in the Data I/O Control Table. With \overline{CEAB} LOW, a LOW signal on the A-to-B Latch Enable (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

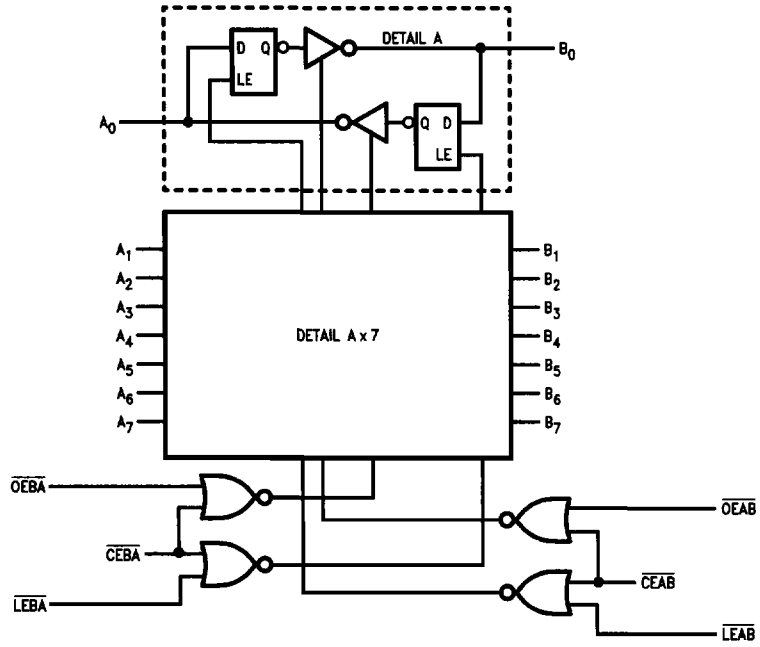
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} and \overline{OEBA}

Logic Diagram



TL/F/9554-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2			V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA (A _n)
		54F 10% V _{CC}	2.4				I _{OH} = -3 mA (A _n , B _n)
		54F 10% V _{CC}	2.0				I _{OH} = -12 mA (B _n)
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA (A _n)
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA (A _n , B _n)
		74F 10% V _{CC}	2.0				I _{OH} = -12 mA (B _n)
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA (A _n)
		74F 5% V _{CC}	2.7				I _{OH} = -3 mA (A _n , B _n)
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA (A _n)
		54F 10% V _{CC}		0.55			I _{OL} = 48 mA (B _n)
		74F 10% V _{CC}		0.5			I _{OL} = 24 mA (A _n)
		74F 10% V _{CC}		0.55			I _{OL} = 64 mA (B _n)
I _{IH}	Input HIGH Current	20			μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	100			μA	Max	V _{IN} = 7.0V (OEAB, OEBA, LEAB, LEBA, CEAB, CEBA)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	1.0			mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current				mA	Max	V _{IN} = 0.5V (OEAB, OEBA)
							V _{IN} = 0.5V (CEAB, CEBA)
I _{IH} + I _{OZH}	Output Leakage Current	70			μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current	-650			μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-60	-150		mA	Max	V _{OUT} = 0V (A _n)
		-100	-225				V _{OUT} = 0V (B _n)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = V _{CC} (A _n , B _n)
I _{CCH}	Power Supply Current		67	100	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		83	125	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		83	125	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	3.0 3.0	5.5 5.0	7.5 6.5			3.0 3.0	8.5 7.5	ns	2-3
t _{PLH} t _{PHL}	Propagation Delay LEB _A to A _n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	2-3
t _{PLH} t _{PHL}	Propagation Delay LEA _B to B _n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	2-3
t _{PZH} t _{PZL}	Output Enable Time OE _B \bar{A} or OE _A \bar{B} to A _n or B _n CE _B \bar{A} or CE _A \bar{B} to A _n or B _n	3.0 4.0	7.0 7.5	9.0 10.5			3.0 4.0	10.0 12.0	ns	2-5
t _{PHZ} t _{PLZ}	Output Disable Time OE _B \bar{A} or OE _A \bar{B} to A _n or B _n CE _B \bar{A} or CE _A \bar{B} to A _n or B _n	2.5 2.5	6.0 5.5	8.0 7.5			2.5 2.5	9.0 8.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com			
		Min	Max	Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time, HIGH or LOW A _n or B _n to LE _B \bar{A} or LE _A \bar{B}	3.0 3.0				3.5 3.5		ns	2-6
t _h (H) t _h (L)	Hold Time, HIGH or LOW A _n or B _n to LE _B \bar{A} or LE _A \bar{B}	3.0 3.0				3.5 3.5			
t _w (L)	Latch Enable, B to A Pulse Width, LOW	8.0				9.0			