MOTOROLA

MC74AC574
MC74ACT574

Product Preview

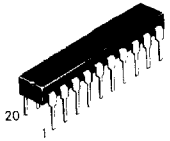
Octal D-Type Flip-Flop with 3-State Outputs

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC74AC574/74ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The MC74AC574/74ACT574 is functionally identical to the MC74AC374/74ACT374 except for the pinouts.

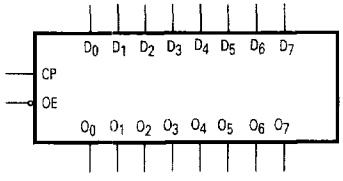
- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC374/74ACT374
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT574 Has TTL Compatible Inputs

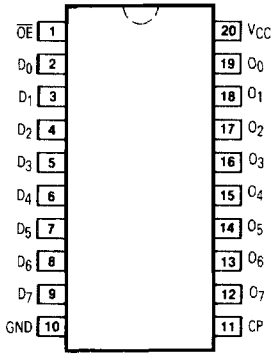


N SUFFIX
CASE 738-03
PLASTIC

DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0–O_7	3-State Outputs

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

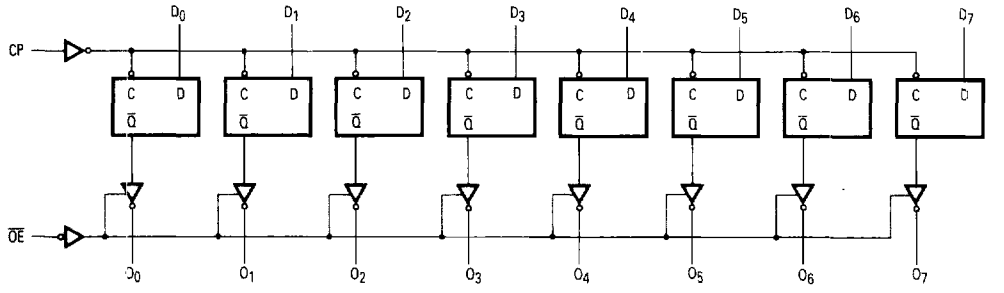
The MC74AC574/74ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT574)	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 160				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		10 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		10 6.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	110		85		ns	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	7.0	11	1.0	12	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	6.5	10	1.0	11	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.4	9.5	1.0	10	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	10	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.5	8.5	1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	4.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V