Advance Information

16M CMOS Wide DRAM Family

Fast Page Mode, x16 and x18

1M x 16

MCM516160A
Fast Page Mode
4096 Cycle Refresh

MCM518160A
Fast Page Mode
1024 Cycle Refresh

1M x 18

MCM516180A
Fast Page Mode
4096 Cycle Refresh

MCM518180A
Fast Page Mode
1024 Cycle Refresh

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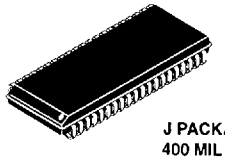
The family of 16M Dynamic RAMs is fabricated using 0.55μ CMOS high-speed silicon-gate process technology. It includes devices organized as 1,048,576 sixteen- and eighteen-bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

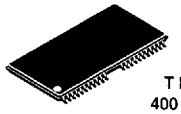
The x16 and x18 devices with 4096 cycle refresh (MCM516160A and MCM516180A) require 12 address lines (12 rows, 8 columns), while the x16 and x18 devices with 1024 cycle refresh (MCM518160A and MCM518180A) require only 10 address lines (10 rows, 10 columns).

These devices are packaged in a standard 400 mil J-lead small outline package (SOJ) and a standard 400 mil thin-small-outline package (TSOP).

- Single 5 V ± 10% Power Supply
- Three-State Data Outputs, x16 and x18 Configurations
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 4096 Cycle Refresh:
  MCM516160A and MCM516180A = 64 ms
- 1024 Cycle Refresh:
  MCM518160A and MCM518180A = 16 ms
- Fast Access Time (t_{RAC}):
  MCM51xxxxA-60 = 60 ns (Max)
  MCM51xxxxA-70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM516160A-60 = 550 mW (Max)
  MCM516160A-70 = 468 mW (Max)
  MCM518160A-60 = 1018 mW (Max)
  MCM518160A-70 = 853 mW (Max)
  MCM516180A-60 = 605 mW (Max)
  MCM516180A-70 = 523 mW (Max)
  MCM518180A-60 = 1100 mW (Max)
  MCM518180A-70 = 935 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 11 mW (Max, TTL Levels)
  All Devices = 5.5 mW (Max, CMOS Levels)



J PACKAGE
400 MIL SOJ
CASE 986-01

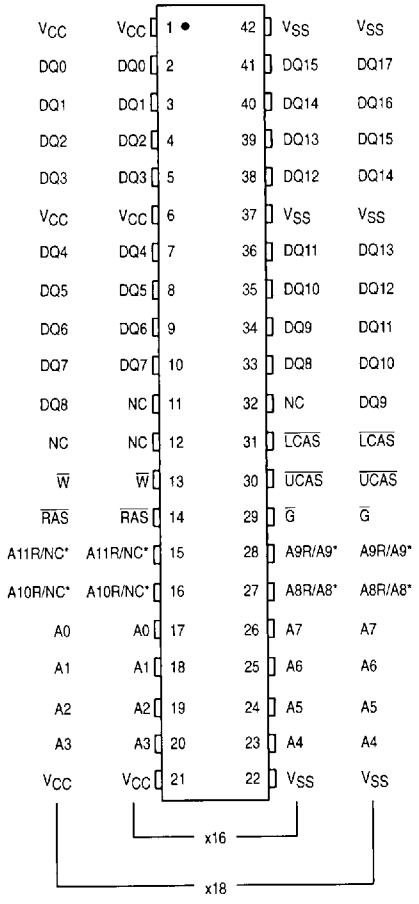


T PACKAGE
400 MIL TSOP II
CASE 985-01

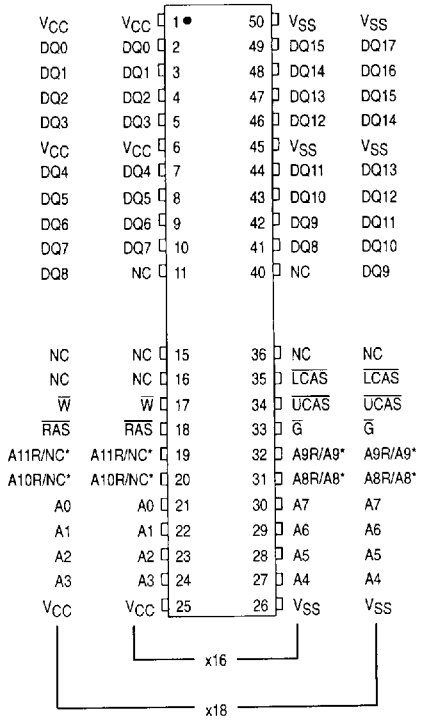
This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS

400 MIL SOJ



400 MIL TSOP

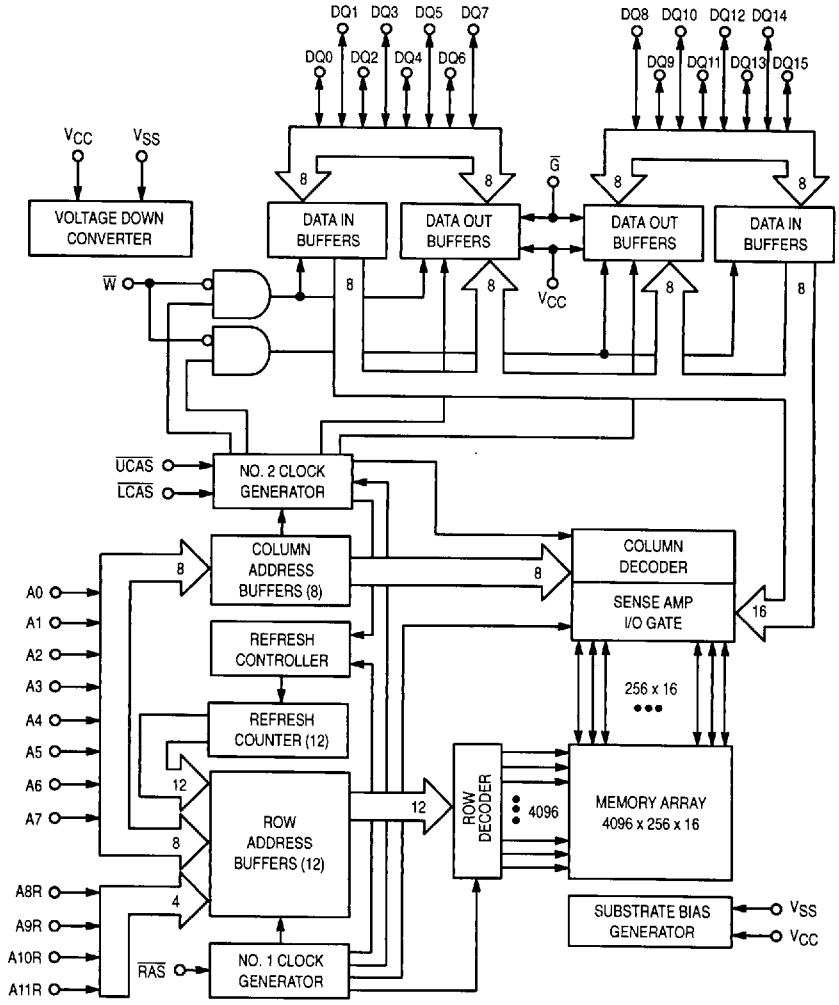


*4096 Cycle Refresh or 1024 Cycle Refresh (R Suffix = Row Address)

PIN NAMES	
A0 – A11 ..... Address Input	LCAS ..... Column Address Strobe
DQ0 – DQ17 ..... Data Input/Output	UCAS ..... Column Address Strobe
G ..... Output Enable	VCC ..... Power Supply (+ 5 V)
W ..... Read/Write Enable	VSS ..... Ground
RAS ..... Row Address Strobe	NC ..... No Connection

BLOCK DIAGRAMS

MCM516160A BLOCK DIAGRAM
1M x 16, 4096 CYCLE REFRESH



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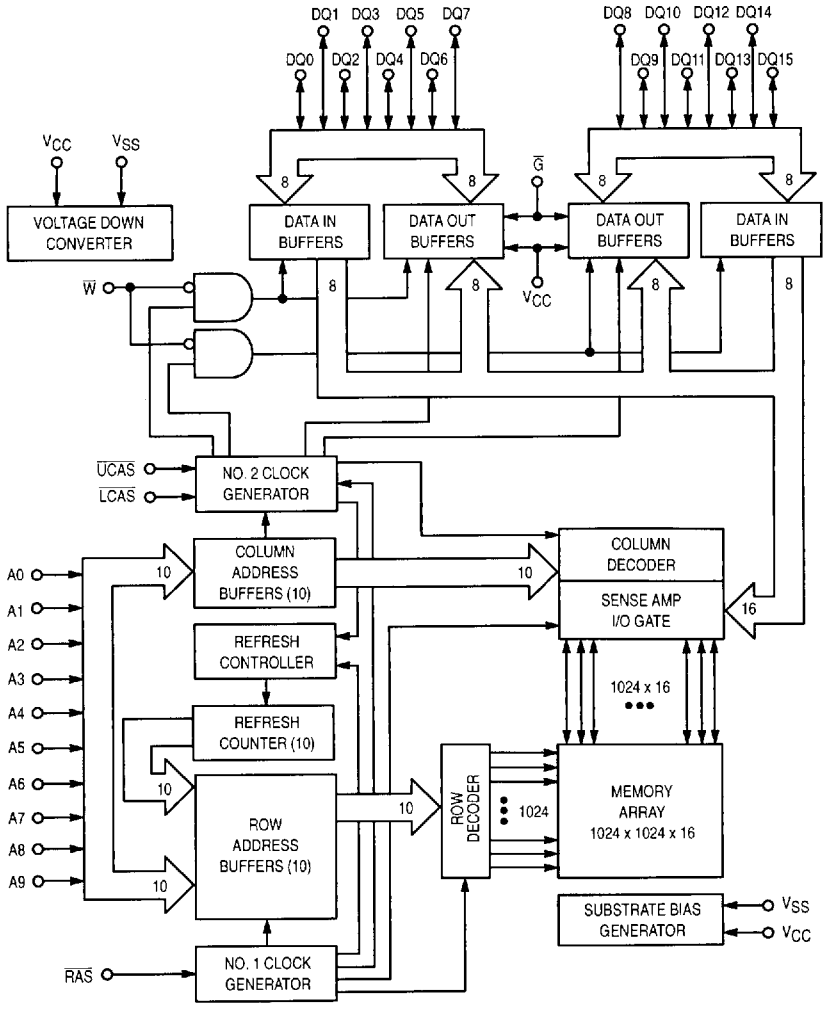
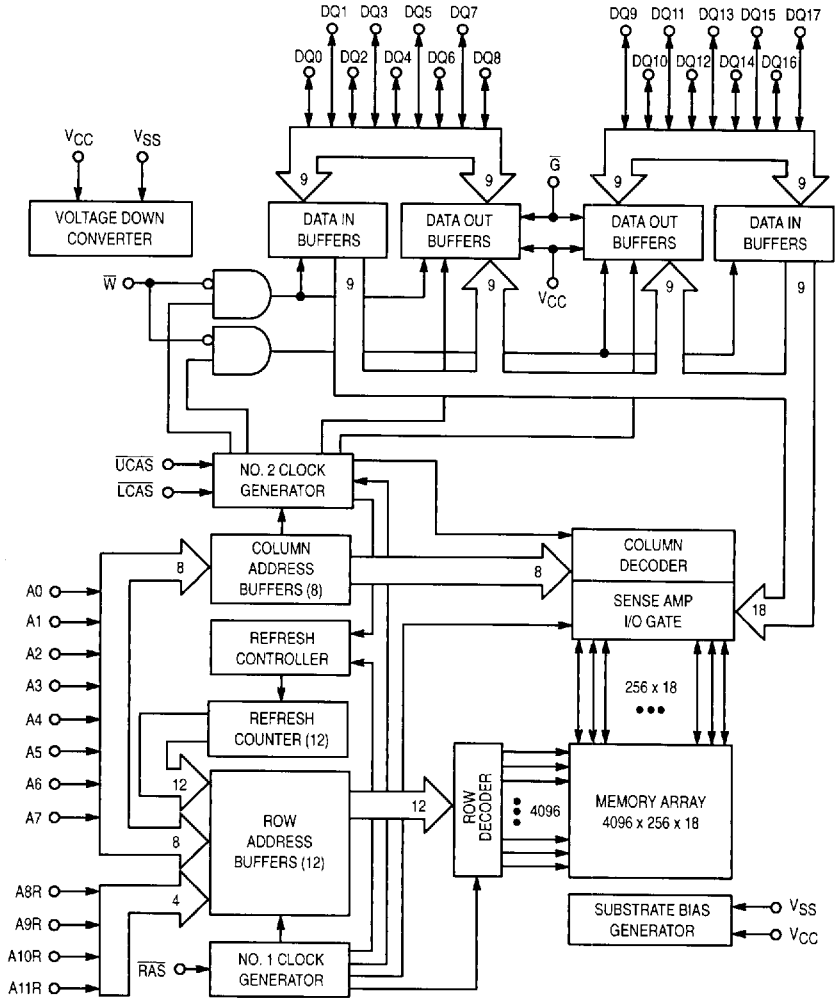
MCM518160A BLOCK DIAGRAM
1M x 16, 1024 CYCLE REFRESH



MCM516180A BLOCK DIAGRAM
1M x 18, 4096 CYCLE REFRESH



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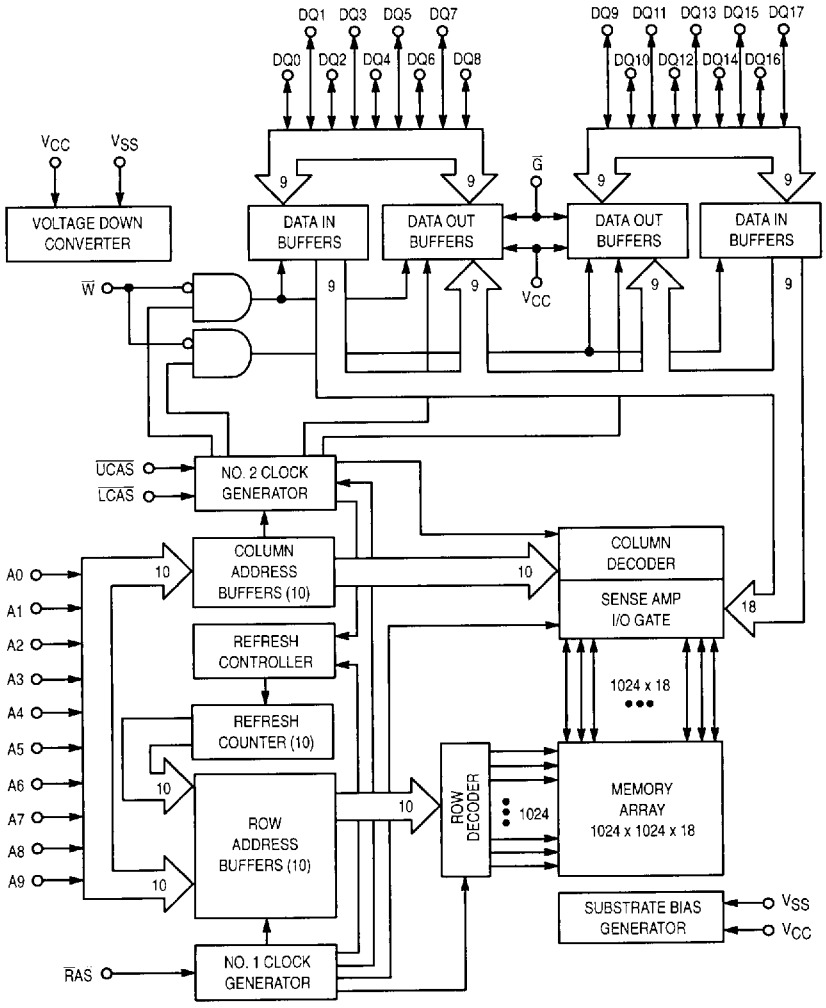
MCM518180A BLOCK DIAGRAM
1M x 18, 1024 CYCLE REFRESH



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	− 0.5 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Data Out Current		I_{out}	50	mA
Soldering Temperature x Time		T_{solder}	260 x 10	°C x s
Power Dissipation	MCM516160A	P_D	950	mW
	MCM518160A		1100	
	MCM516180A		950	
	MCM518180A		1100	
Operating Temperature Range		T_A	0 to + 70	°C
Storage Temperature Range		T_{stg}	− 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5*	V
Logic Low Voltage, All Inputs	V_{IL}	− 0.5**	—	0.8	V

* V_{CC} + 2.0 V at pulse width ≤ 20 ns.
** −2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	MCM51xxxxA-60		MCM51xxxxA-70		Unit	Notes
		Min	Max	Min	Max		
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min) MCM516160A-xx	I_{CC1}	—	100	—	85	mA	1, 2
MCM518160A-xx		—	185	—	155		
MCM516180A-xx		—	110	—	95		
MCM518180A-xx		—	200	—	170		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})	I_{CC2}	—	2	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, t_{RC} = t_{RC} Min)	I_{CC3}					mA	1, 2
MCM516160A-xx		—	100	—	85		
MCM518160A-xx		—	185	—	155		
MCM516180A-xx		—	110	—	95		
MCM518180A-xx		—	200	—	170		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}					mA	1, 2
MCM516160A-xx		—	90	—	80		
MCM518160A-xx		—	90	—	80		
MCM516180A-xx		—	95	—	85		
MCM518180A-xx		—	95	—	85		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1	—	1	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = t_{RC} Min)	I_{CC6}					mA	1
MCM516160A-xx		—	100	—	85		
MCM518160A-xx		—	185	—	155		
MCM516180A-xx		—	110	—	95		
MCM518180A-xx		—	200	—	170		
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	–10	10	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	–10	10	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{PC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance A0 – A11	C_{in}	5	pF
Input Capacitance $\overline{G}$, $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$		7	
Input/Output Capacitance ($\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} to Disable Output) DQ0 – DQ17	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM5161x0A-60 MCM5181x0A-60		MCM5161x0A-70 MCM5181x0A-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	180	—	ns	5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (Continued)

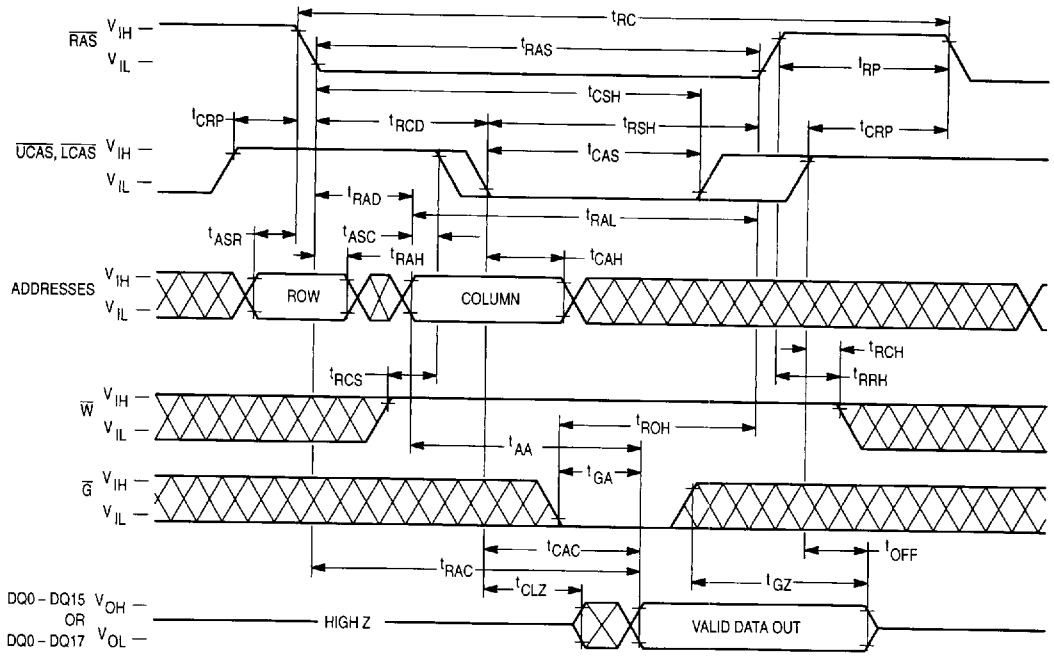
Parameter	Symbol		MCM5161x0A-60 MCM5181x0A-60		MCM5161x0A-70 MCM5181x0A-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	14
Refresh Period MCM516xxxA MCM518xxxA	t_{RVRV}	t_{RFSH}	— —	64 16	— —	64 16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	40	—	45	—	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	—	95	—	ns	15
Column Address to Write Delay	t_{AVWL}	t_{AWD}	55	—	60	—	ns	15
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	60	—	65	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{CELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	15	—	20	ns	6
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	15	—	15	—	ns	
Output Buffer Turn-Off Delay from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	15	0	15	ns	10
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	15	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GDS}	0	—	0	—	ns	
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	85	—	90	—	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode) MCM516xxxA MCM518xxxA	t_{RELREH}	t_{RASP}	60 60	100 k 100 k	70 70	100 k 200 k	ns	

NOTES:

14. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

READ CYCLE



NOTE: D_{in} = Open

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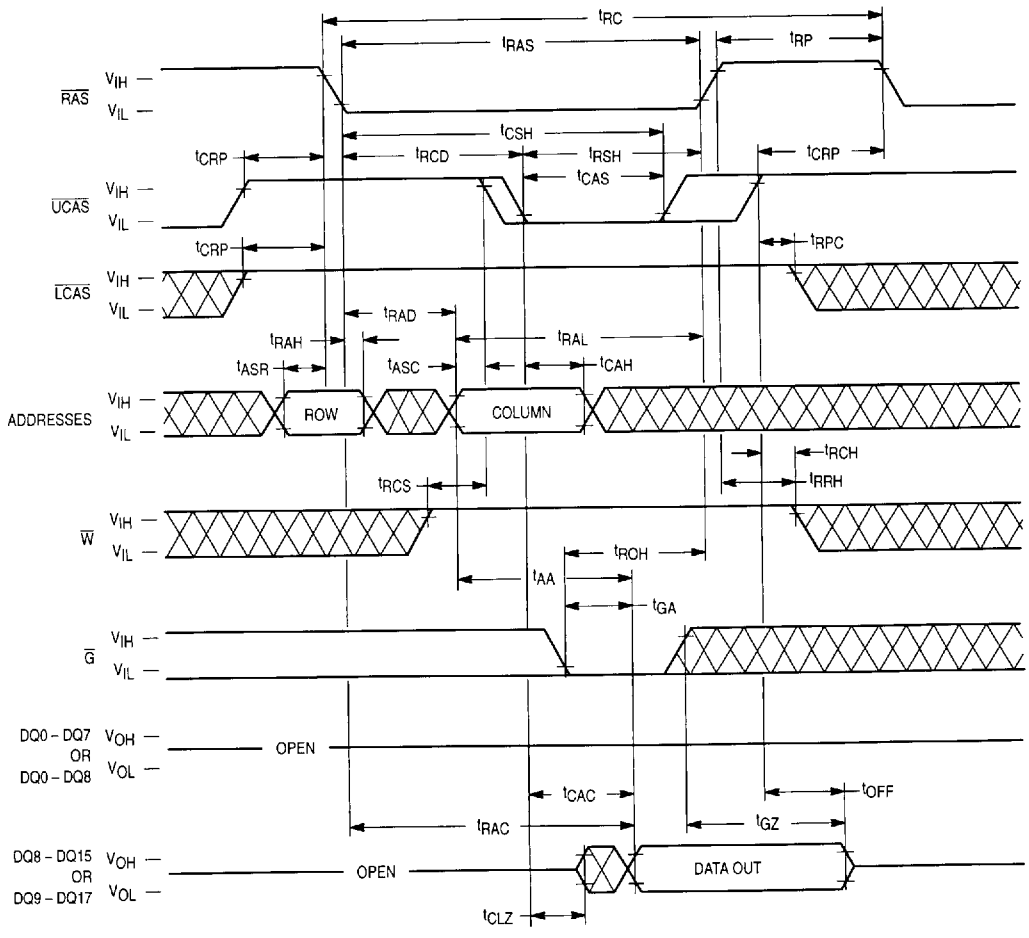
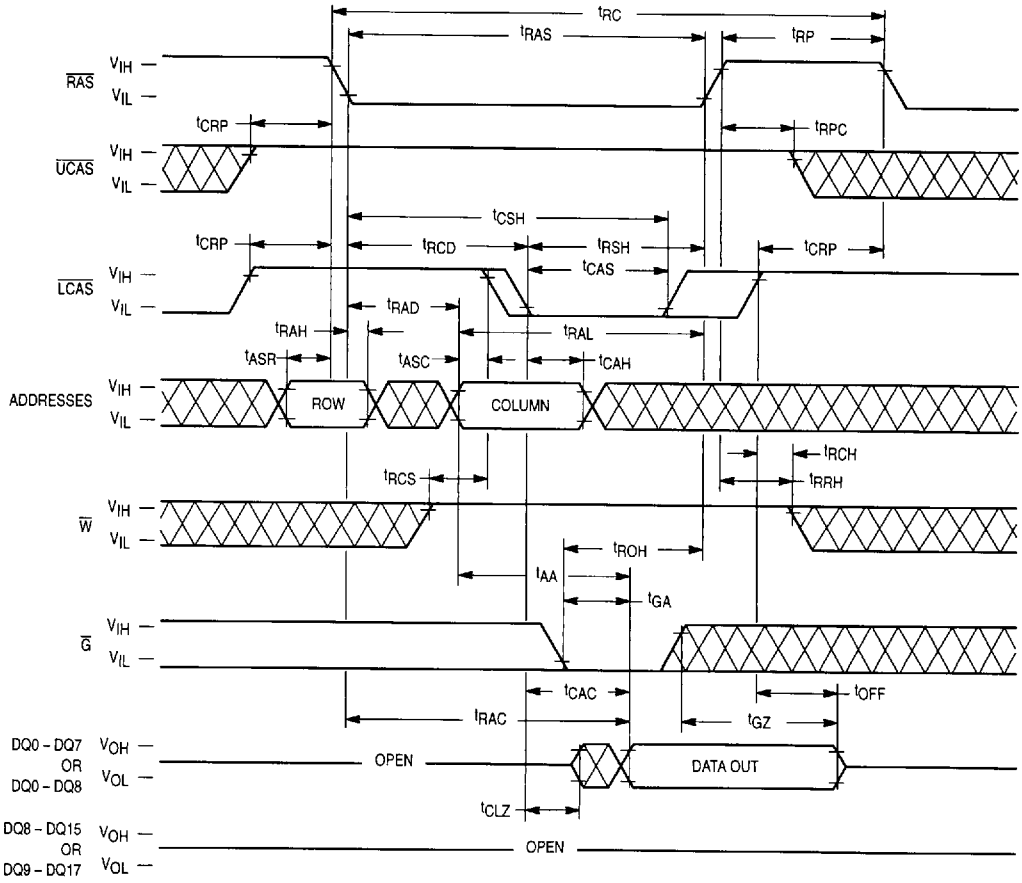
UPPER BYTE READ CYCLE



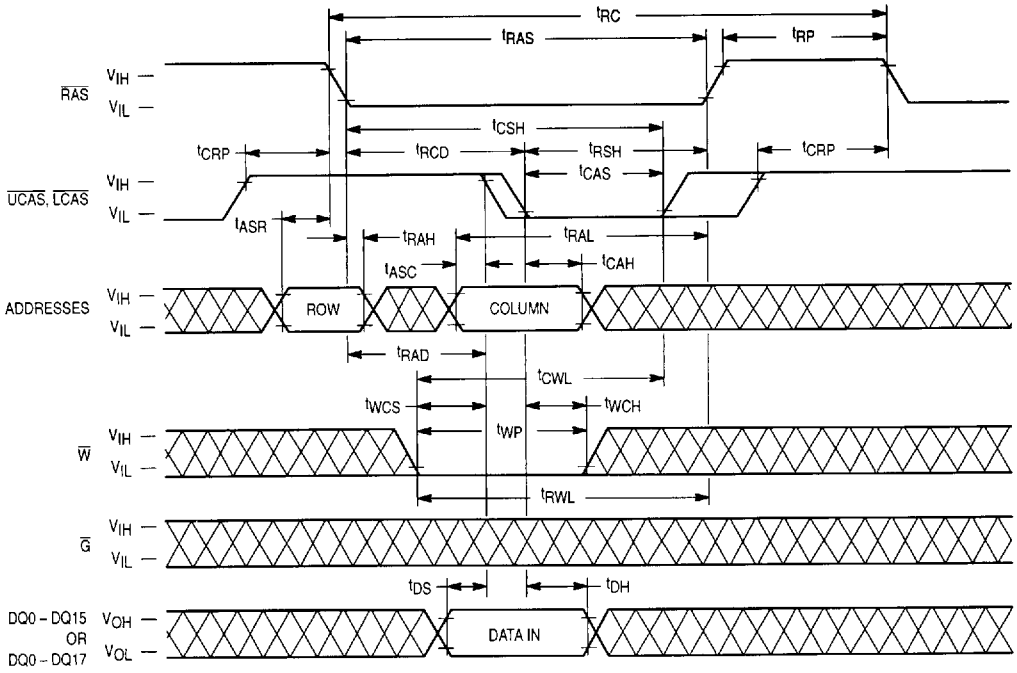
NOTE: D_{in} (DQ0 – DQ7 or DQ0 – DQ8) = Don't Care
D_{in} (DQ8 – DQ15 or DQ9 – DQ17) = Open

LOWER BYTE READ CYCLE



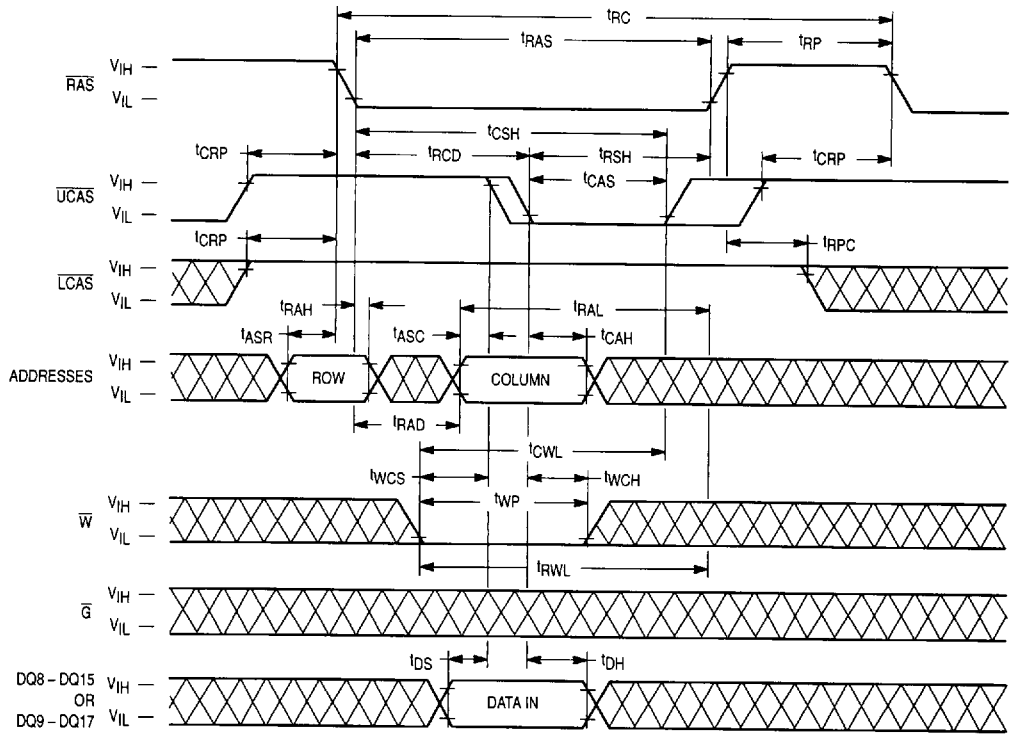
NOTE: D_{in} (DQ0 – DQ7 or DQ0 – DQ8) = Open
D_{in} (DQ8 – DQ15 or DQ9 – DQ17) = Don't Care

WRITE CYCLE (EARLY WRITE)



NOTE: D_{out} = Open

UPPER BYTE WRITE CYCLE (EARLY WRITE)



NOTE: D_{in} (DQ0 – DQ7 or DQ0 – DQ8) = Don't Care
D_{out} = Open

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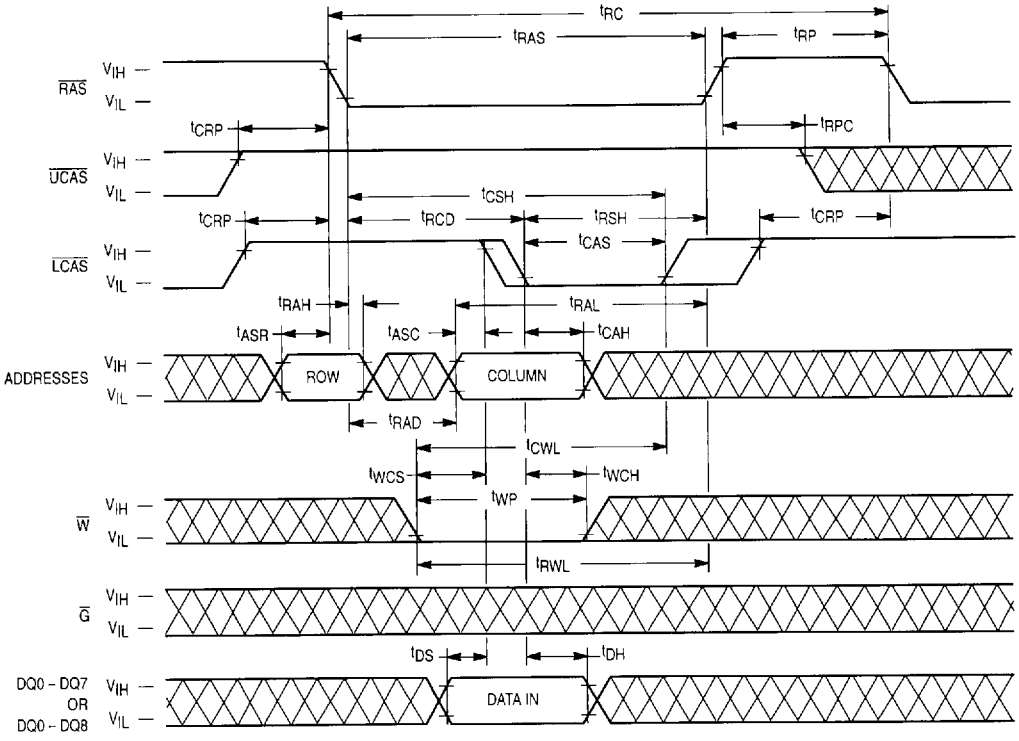
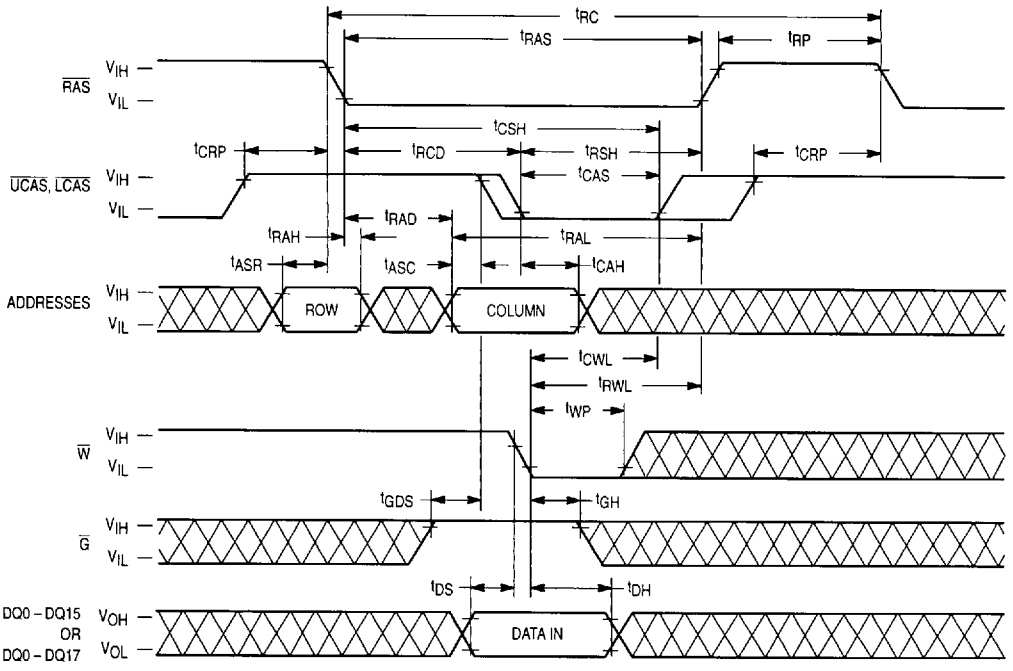
LOWER BYTE WRITE CYCLE (EARLY WRITE)



NOTE: D_{in} (DQ8 – DQ15 or DQ9 – DQ17) = Don't Care
D_{out} = Open

WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



NOTE: D_{out} = Open

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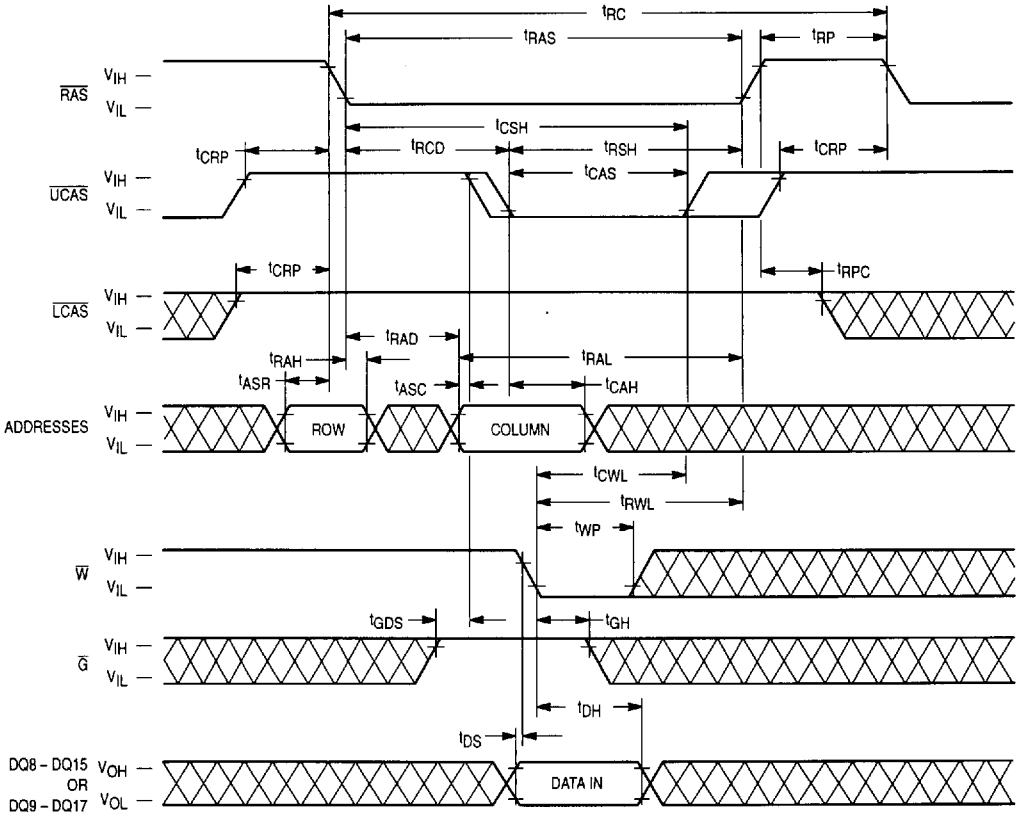
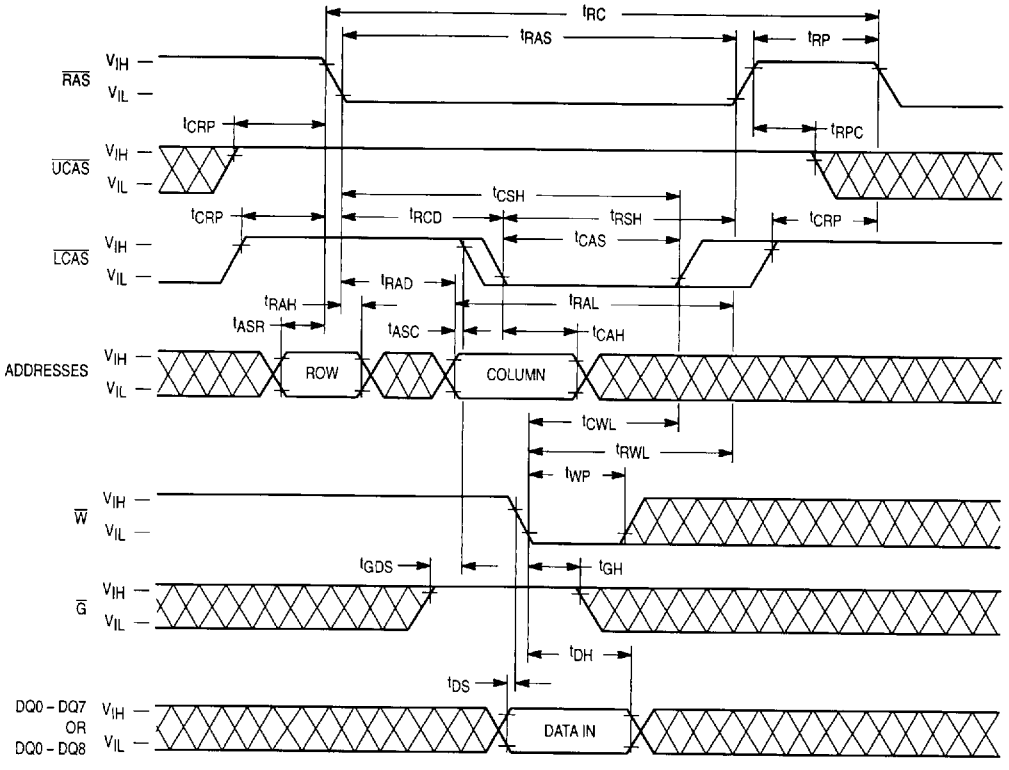
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



NOTE: D_{in} (DQ0 – DQ7 or DQ0 – DQ8) = Don't Care
D_{out} = Open

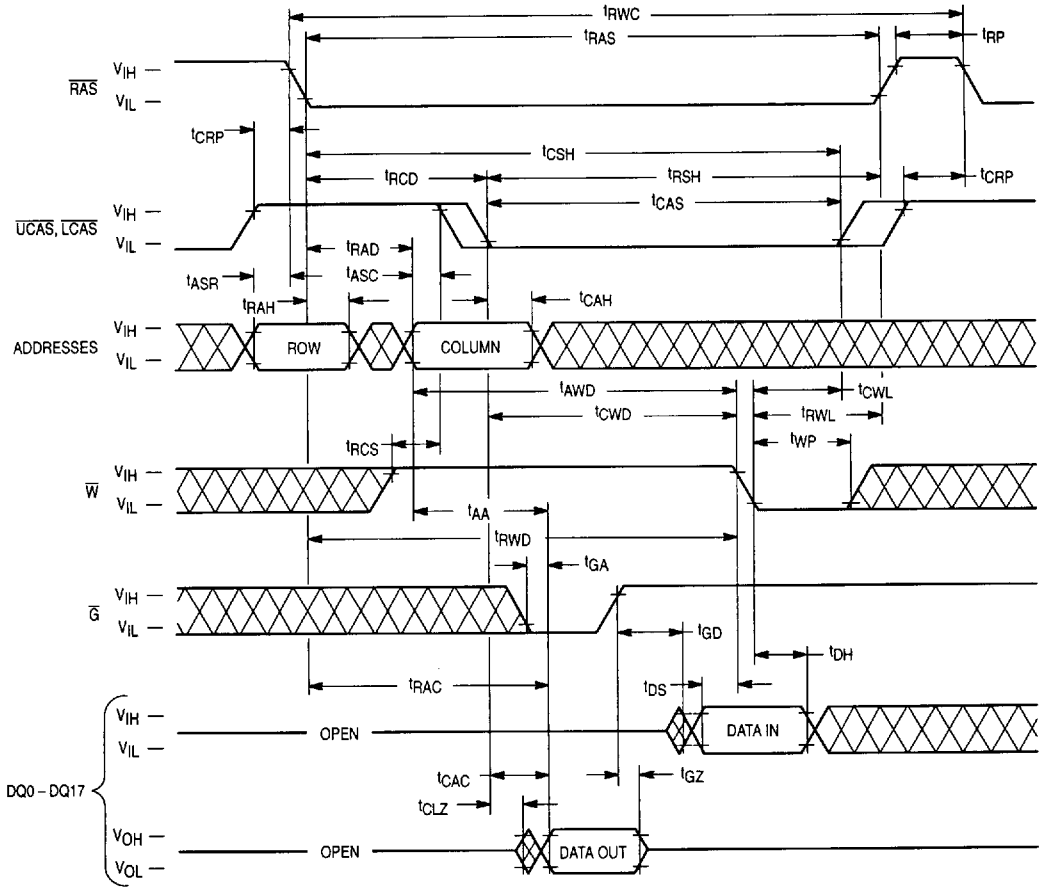
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



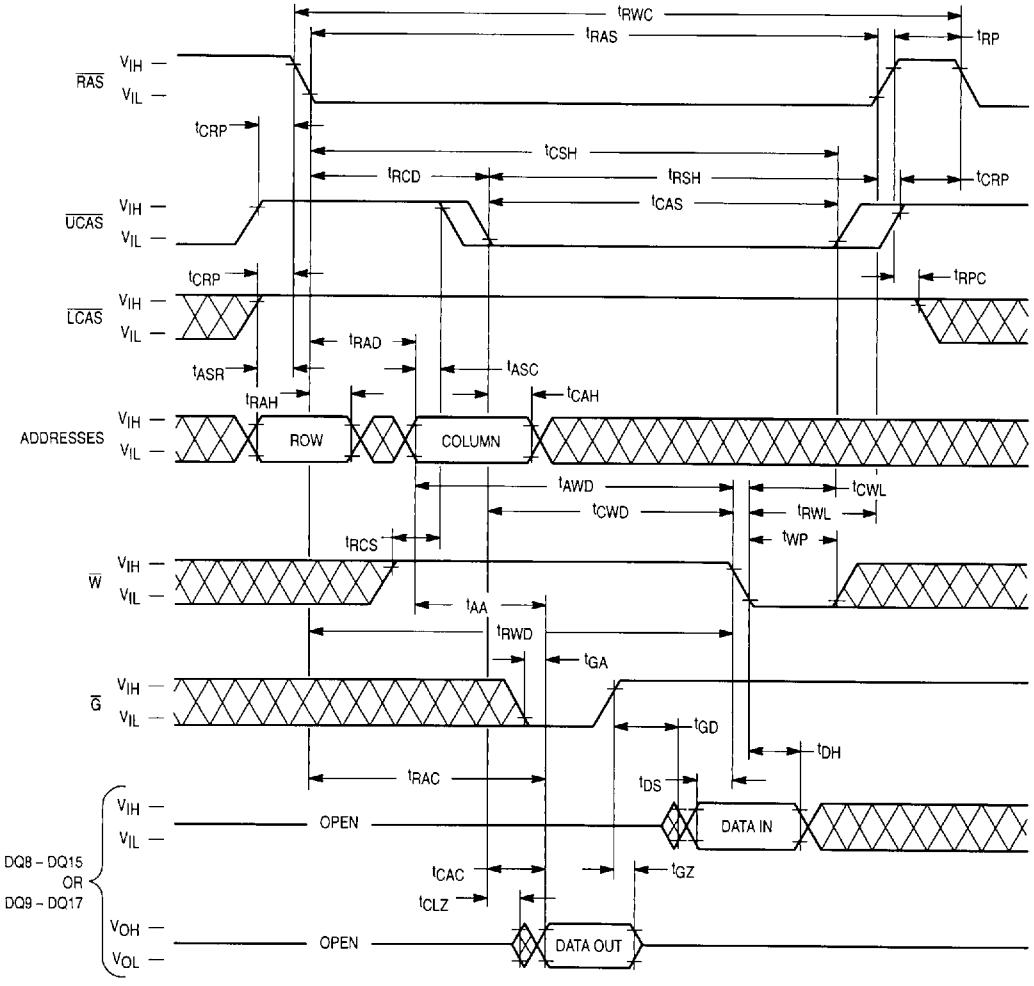
NOTE: D_{in} (DQ8 – DQ15 or DQ9 – DQ17) = Don't Care
D_{out} = Open

4

READ-WRITE CYCLE

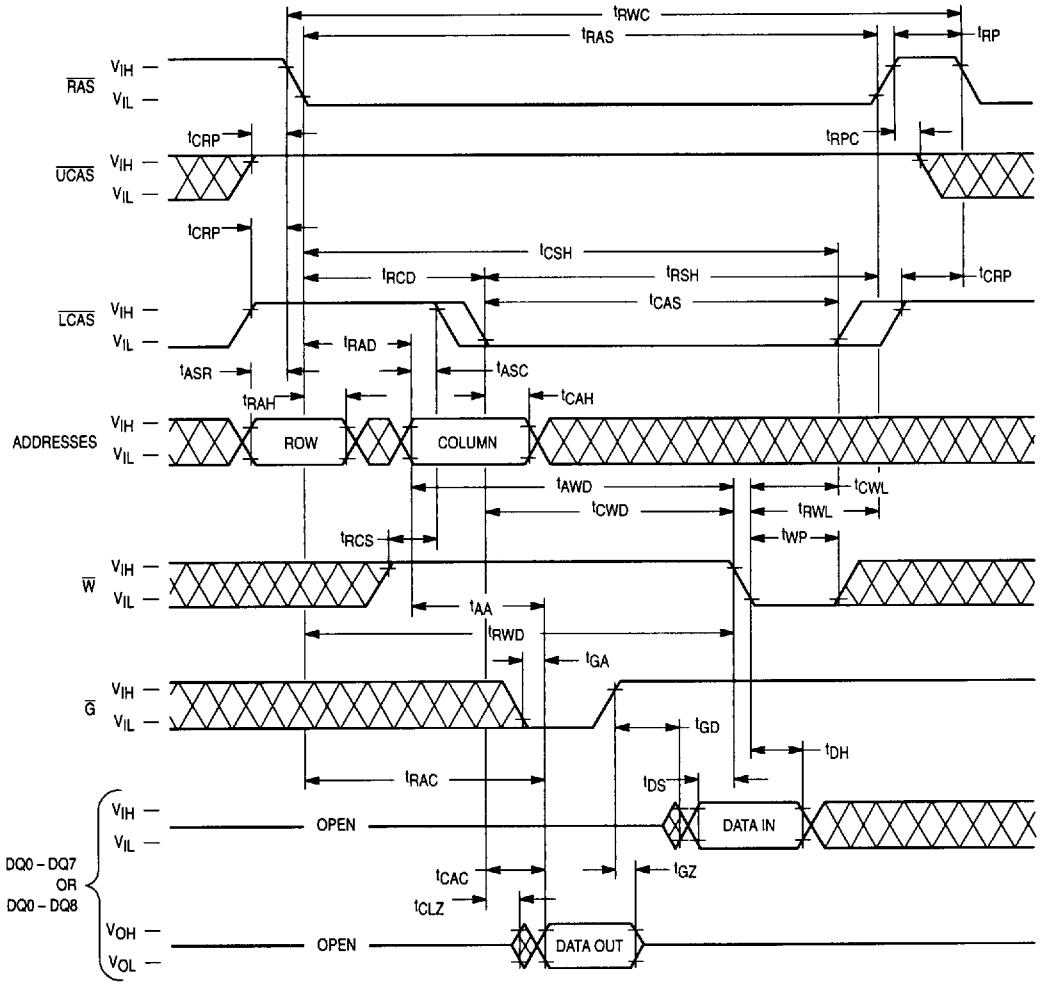


UPPER BYTE READ-WRITE CYCLE



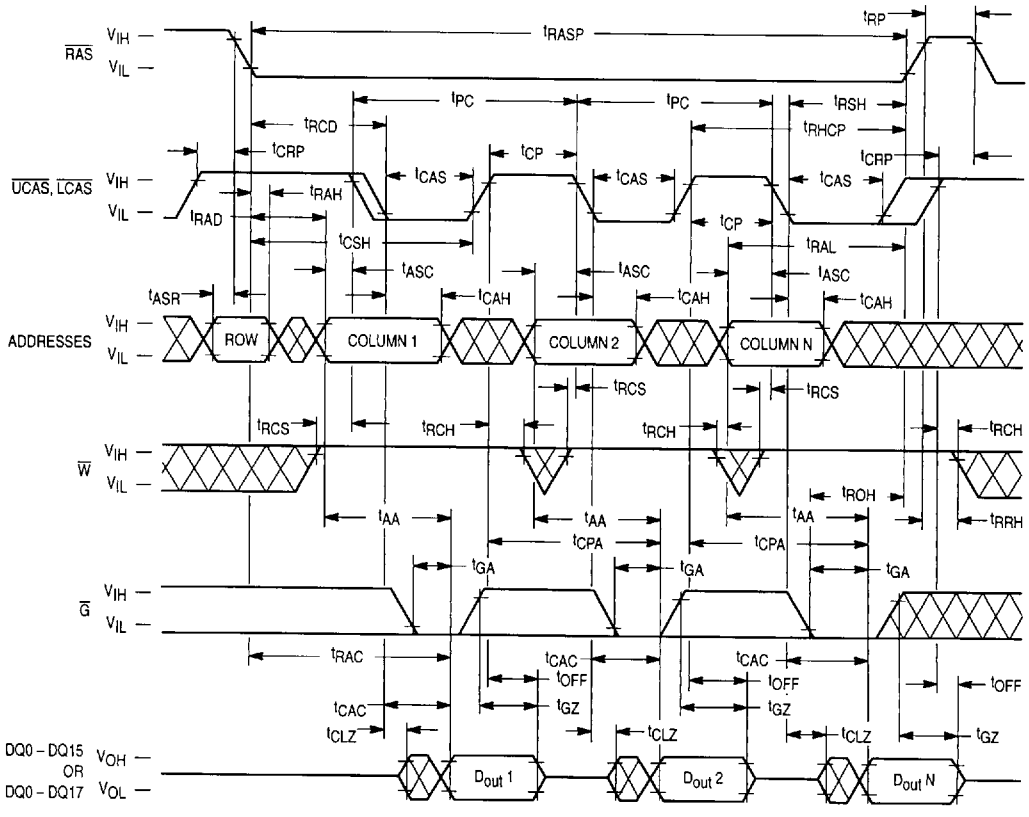
NOTE: D_{in} (DQ0 – DQ7 or DQ0 – DQ8) = Don't Care
D_{out} (DQ0 – DQ7 or DQ0 – DQ8) = Open

LOWER BYTE READ-WRITE CYCLE



NOTE: D_{in} (DQ8 – DQ15 or DQ9 – DQ17) = Don't Care
D_{out} (DQ8 – DQ15 or DQ9 – DQ17) = Open

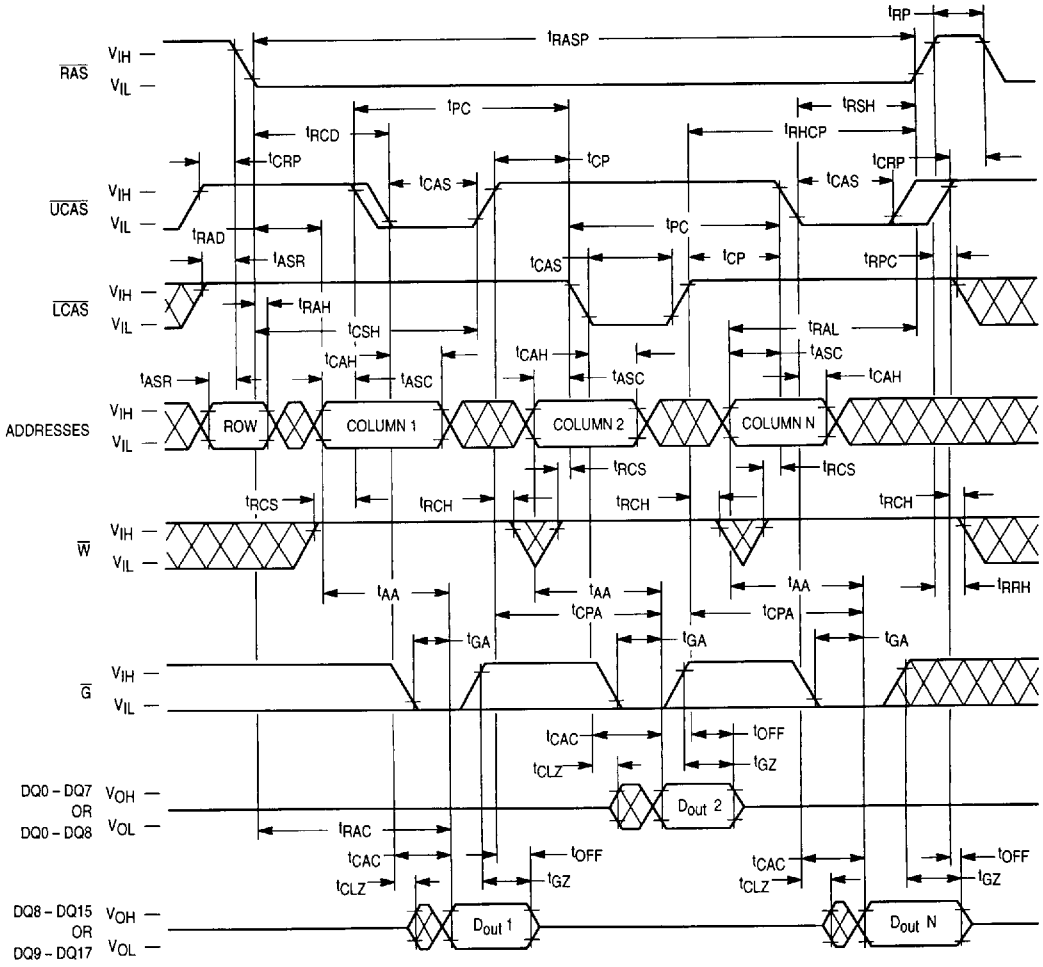
FAST PAGE MODE READ CYCLE



NOTE: D_{in} = Open

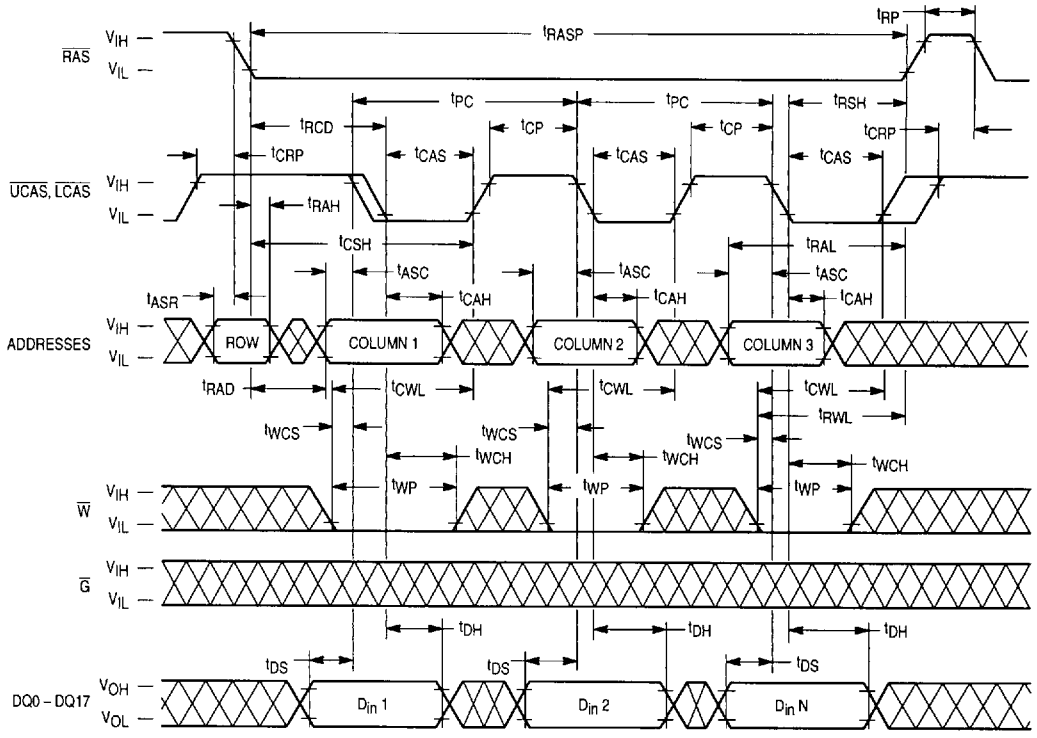
4

FAST PAGE MODE BYTE READ CYCLE



NOTE: D_{in} Open

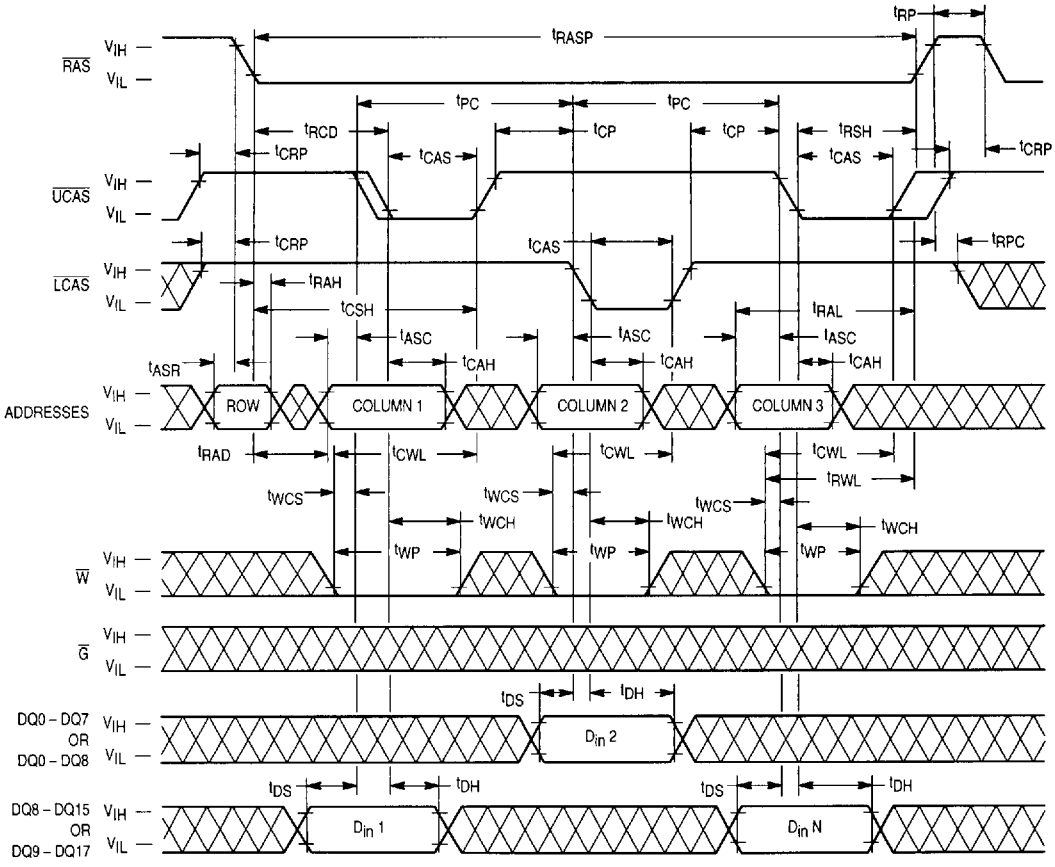
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



NOTE: D_{out} = Open

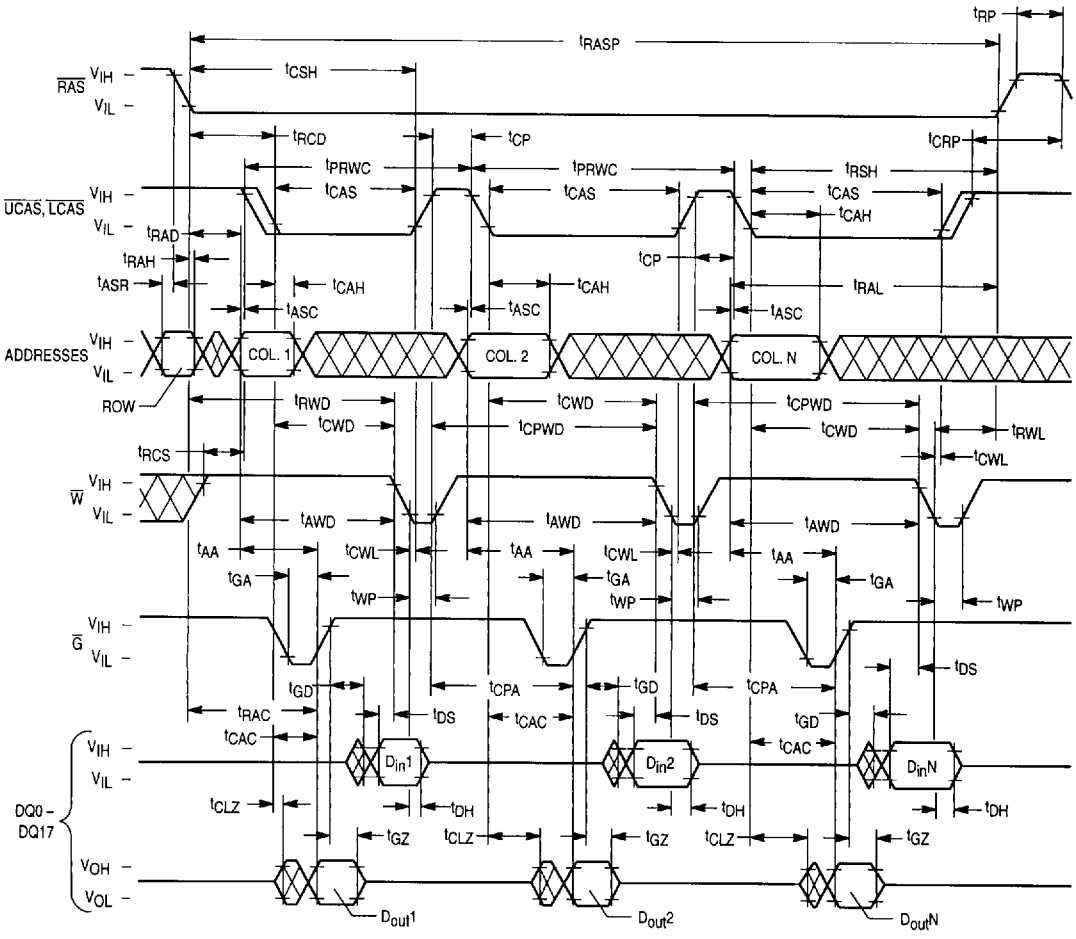
4

FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



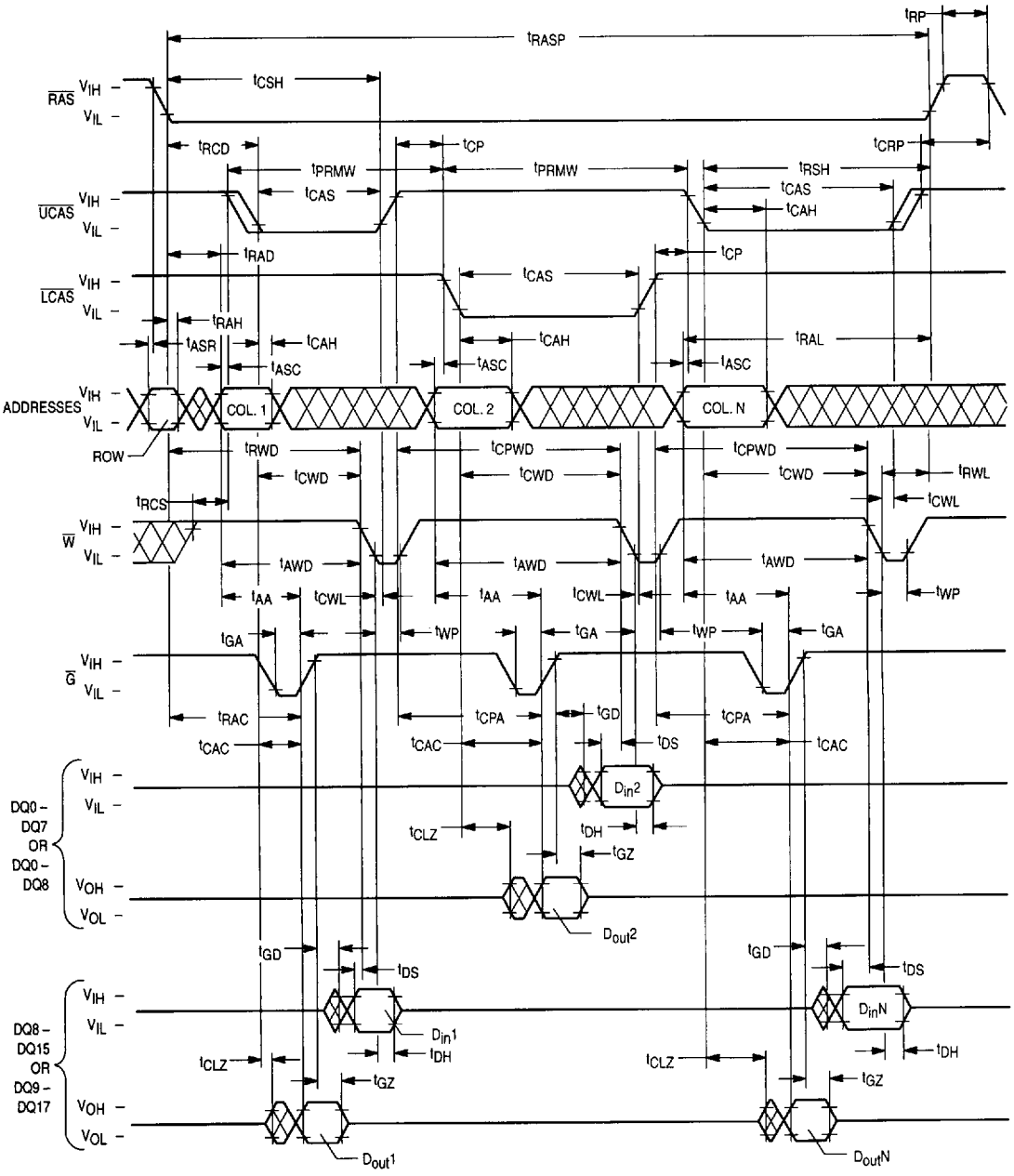
NOTE: D_{out} = Open

FAST PAGE MODE READ-WRITE CYCLE

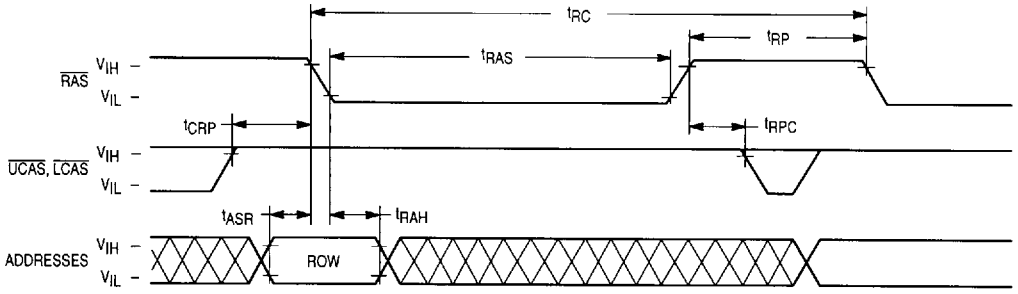


4

FAST PAGE MODE BYTE READ-WRITE CYCLE



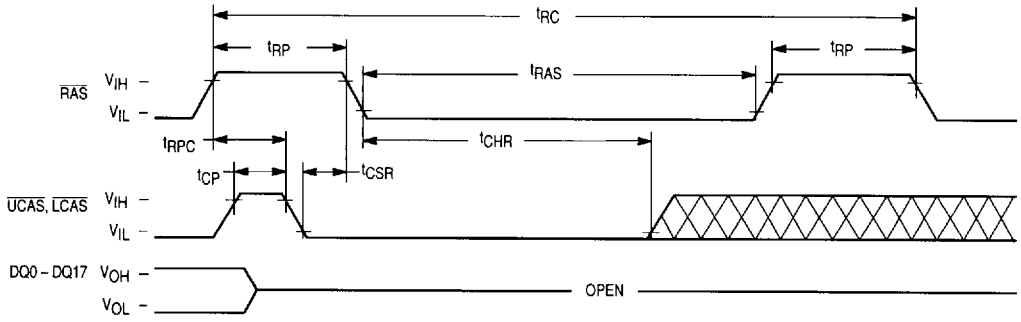
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



NOTE: $\overline{W}$, $\overline{G}$ = "H" or "L"
D_{in} = Don't Care
D_{out} = Open
Addresses: MCM516xxxA — A0 to A11; MCM518xxxA — A0 to A9.

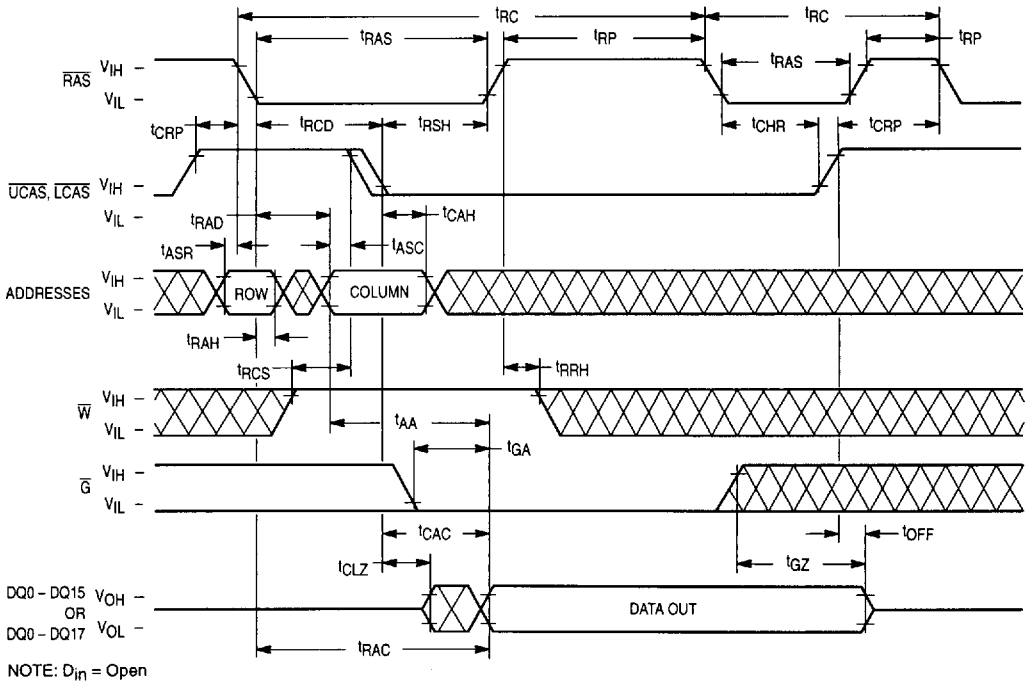
4

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



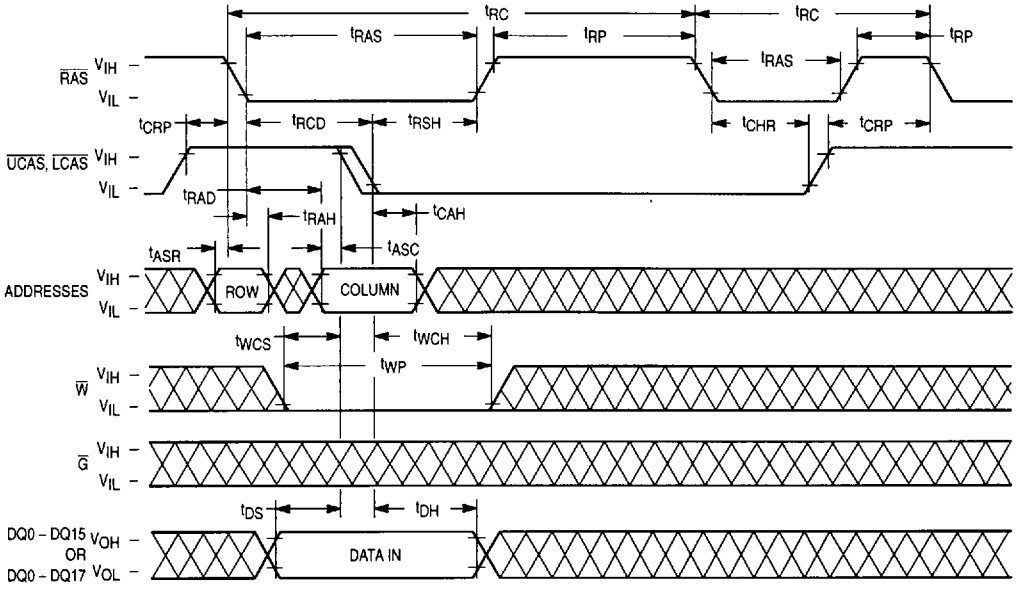
NOTE: $\overline{W}$, $\overline{G}$, Addresses= "H" or "L"
D_{in} = Don't Care
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is performed when either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ meets this timing.

HIDDEN REFRESH CYCLE (READ)



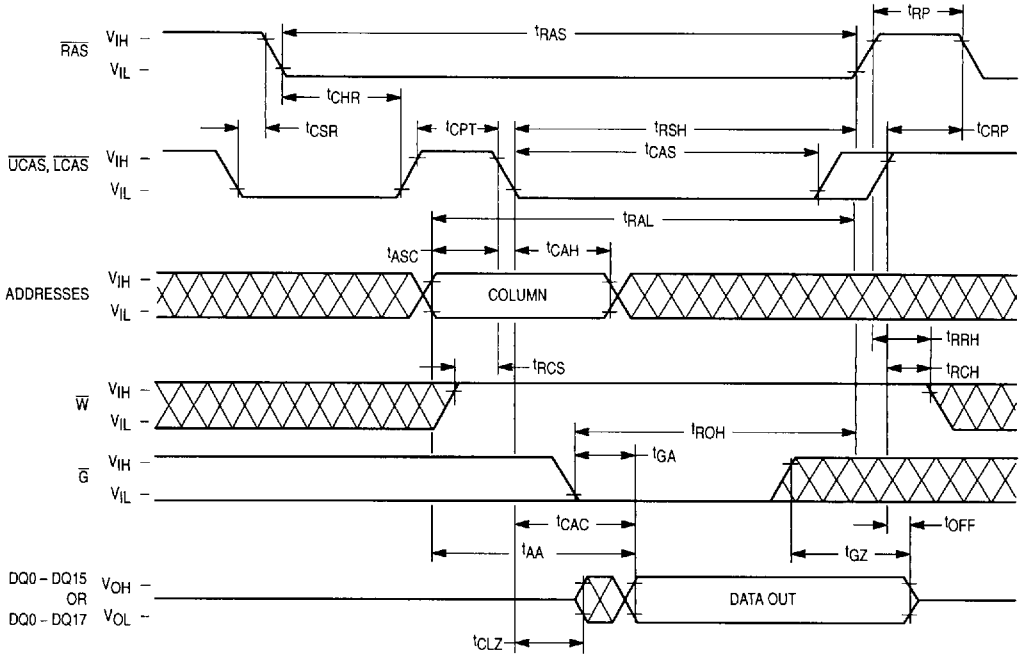
NOTE: D_{in} = Open

HIDDEN REFRESH CYCLE (WRITE)



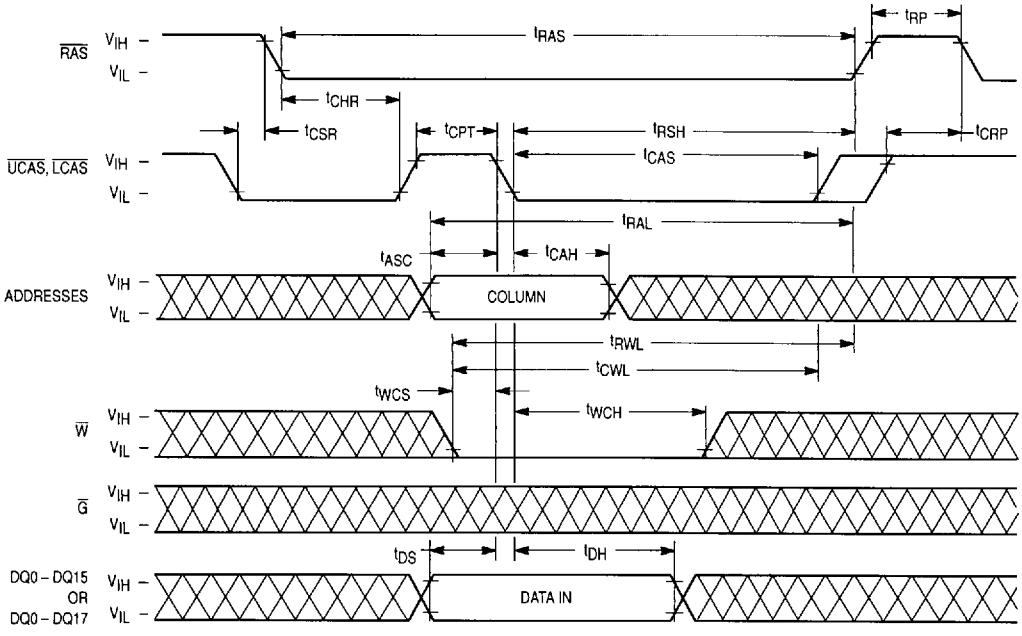
NOTE: D_{out} = Open

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



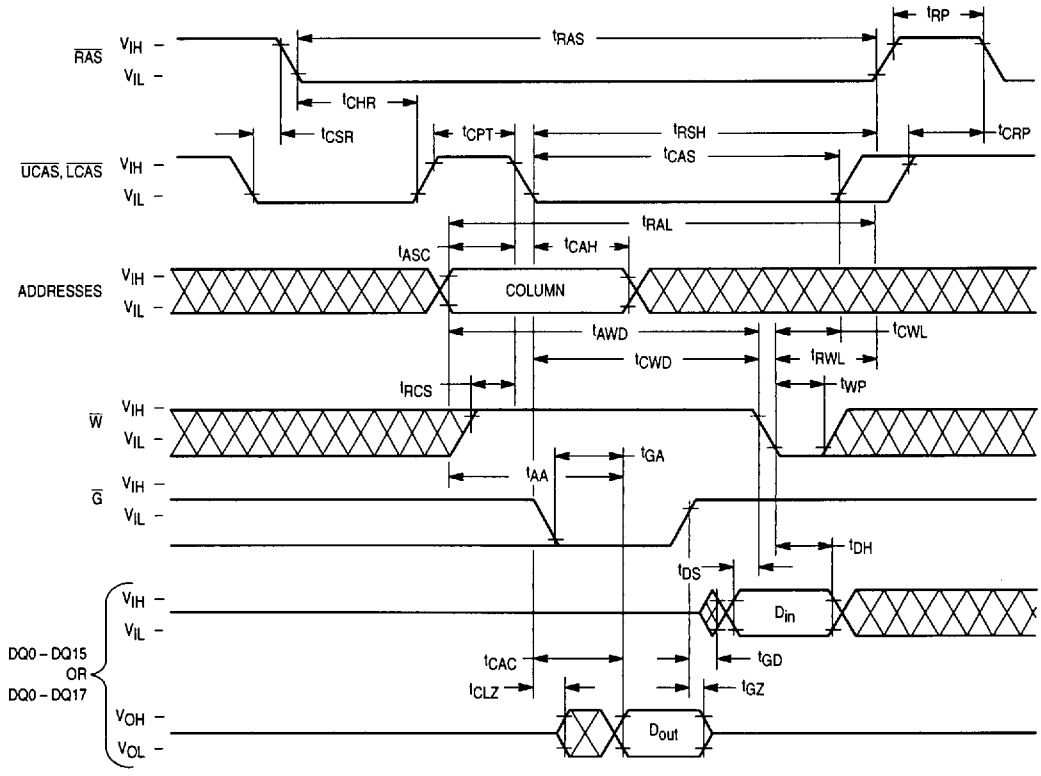
NOTE: Addresses: MCM516xxxA — A0 to A7; MCM518xxxA — A0 to A9
D_{in} = Open

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



NOTE: Addresses: MCM516xxxA — A0 to A7; MCM518xxxA — A0 to A9
D_{in} = Open

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-WRITE CYCLE



NOTE: Addresses: MCM516xxxA — A0 to A7; MCM518xxxA — A0 to A9.

ORDERING INFORMATION
(Order by Full Part Number)

	51x160A or				
MCM	51x180A	X	XX	X	
Motorola Memory Prefix					
Part Number					
					Shipping Method (R = Tape and Reel, Blank = Rails for SOJ, Trays for TSOP II)
					Speed (60 = 60 ns, 70 = 70 ns)
					Package (J = 400 mil SOJ, T = 400 mil TSOP II)

MCM516160AJ60	MCM516160AJ60R	MCM516160AT60	MCM516160AT60R
MCM516160AJ70	MCM516160AJ70R	MCM516160AT70	MCM516160AT70R
MCM518160AJ60	MCM518160AJ60R	MCM518160AT60	MCM518160AT60R
MCM518160AJ70	MCM518160AJ70R	MCM518160AT70	MCM518160AT70R
MCM516180AJ60	MCM516180AJ60R	MCM516180AT60	MCM516180AT60R
MCM516180AJ70	MCM516180AJ70R	MCM516180AT70	MCM516180AT70R
MCM518180AJ60	MCM518180AJ60R	MCM518180AT60	MCM518180AT60R
MCM518180AJ70	MCM518180AJ70R	MCM518180AT70	MCM518180AT70R