8-Line Multiplexer

Military 10H564

ELECTRICALLY TESTED PER:
5962-8772901

The 10H564 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

The 10H564 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The 10H564 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the 10H564 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional 10H564's.

- Propagation Delay, 1.5 ns Typical
- 455 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8772901
3) 883: 10H564/BXAJC
X = CASE OUTLINE AS FOLLOWS:

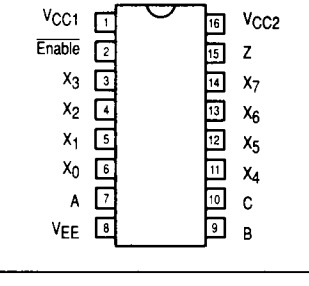
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

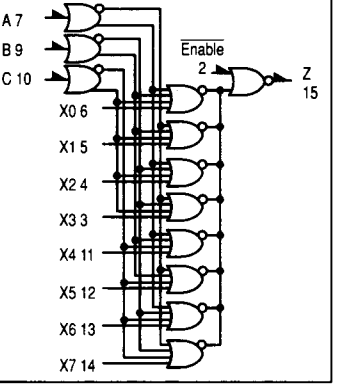
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{Enable}$	2	6	3	OPEN
X_3	3	7	4	OPEN
X_2	4	8	5	OPEN
X_1	5	9	7	OPEN
X_0	6	10	8	GND
A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
C	10	14	13	OPEN
X_4	11	15	14	OPEN
X_5	12	16	15	OPEN
X_6	13	1	17	OPEN
X_7	14	2	18	OPEN
Z	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



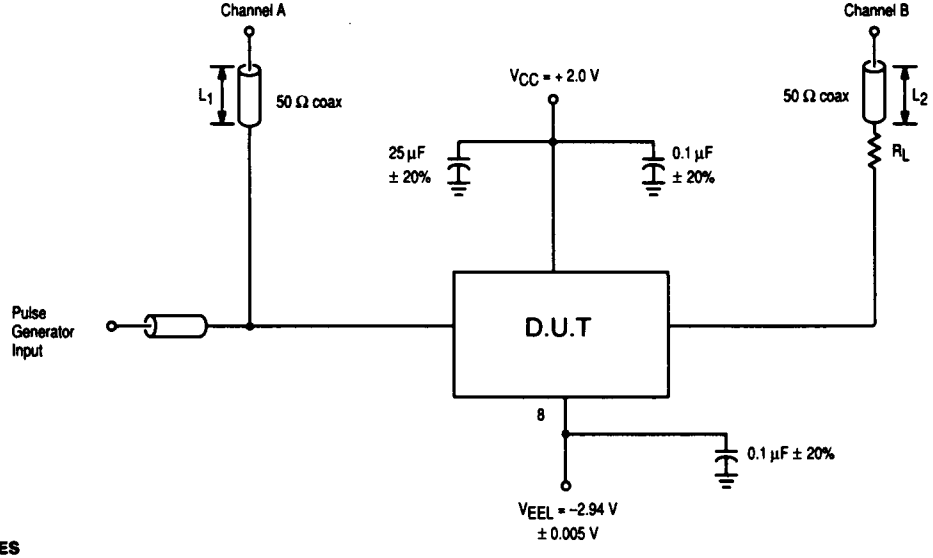
LOGIC DIAGRAM



TRUTH TABLE

	ADDRESS INPUTS			
$\overline{\text{ENABLE}}$	C	B	A	Z
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	Ø	Ø	Ø	L

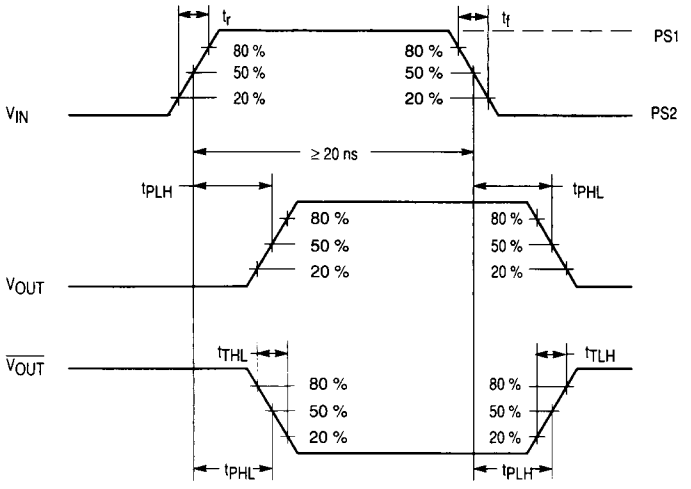
Ø = Don't Care



NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. $R_L = 50\ \Omega$.

Figure 1. Switching Test Circuit



NOTES

V_{IN} has the following characteristics:

1. P_W = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

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QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14	2, 9 10				8	1, 16	15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	2, 7, 9 10, 14	2 - 7 9 - 14				8	1, 16	15
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 13	2, 7, 9 10	3 - 5, 7 9 - 14	2, 7 9, 10	8	8	1, 16	15
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	7, 9 10, 14	2, 7, 9 10	2	3 - 6 11 - 14	8	8	1, 16	15
I_{EE}	Power Supply Current	-75		-83		-83		mA						8	1, 16	8
I_{IH}	Input Current High		320		510		510	µA	2 - 7 9 - 14					8	1, 16	2 - 7, 9- 14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2 - 7 9 - 14			8		1, 16	2 - 7, 9 - 14

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QUIESCENT LIMIT TABLE *

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T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{THL}	Fall Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Address to Output	1.45	2.7	1.6	3.2	1.4	2.6	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Address to Output	1.45	3.2	1.6	3.4	1.4	3.1	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Data to Output	1.0	2.3	1.15	2.6	1.0	2.2	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Data to Output	1.1	2.7	1.6	3.4	1.0	2.5	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Enable to Output	0.5	1.9	0.55	2.0	0.45	2.0	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Enable to Output	0.66	2.0	0.7	2.0	0.55	2.0	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15