Supertex inc.

HCT/SC137
HCT/SC138
HCT/SC139
HCT/SC237
HCT/SC238
HCT/SC239

Octal Decoders/Demultiplexers

Product Summary

Device Parameter	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
1 of 8 decoder/demultiplexer with latched addresses	Inverted	74HCT137	74SC137	54HCT137
	Non-Inverted	74HCT237	74SC237	54HCT237
1 of 8 decoder/demultiplexer	Inverted	74HCT138	74SC138	54HCT138
	Non-Inverted	74HCT238	74SC238	54HCT238
Dual 1 of 4 decoder/demultiplexer	Inverted	74HCT139	74SC139	54HCT139
	Non-Inverted	74HCT239	74SC239	54HCT239
Operating temperature range (°C)		-40 to +85	-40 to +85	-55 to +125
Recommended operating voltage (V)		4.75 to 5.25	4.75 to 5.25	4.50 to 5.50
Maximum gate propagation delay (ns)		25/30	45	45

Features

- ☐ Pin and function compatible to 54/74LS equivalent circuits
- ☐ Typical DC operating supply current: 10μA
- ☐ Input hysteresis improves noise immunity
- ☐ Fast propagation delay times
- ☐ Fan out of 15 LSTTL loads
- ☐ Full TTL and CMOS compatibility
- ☐ -40°C to +85°C operating temperature range
- ☐ Capable of operating over 3-volt to 6-volt range
- ☐ High speed silicon-gate CMOS technology
- ☐ MIL STD 883B Screening/Leadless chip carrier available.

General Description

This family of decoders/demultiplexers is designed for use in high speed memory and peripheral address decoding systems.

138 and 238 decode three binary inputs to select one of eight mutually exclusive outputs. Three Enable inputs, two active low and one active high, reduce the need for external gates in an expanded system.

137 and 237 feature additional latches on address inputs for glitch-free applications. When latch enable is high,the latch is disabled. When latch enable is low, the address present at the address inputs is stored.

The 139 and 239 feature two individual, two-line to four-line decoders.

Absolute Maximum Ratings

Rating	Value
Supply voltage, VCC	−0.5V to +7.0V
Input voltage, VI	−0.3V to VCC+0.3V
Short circuit output current, ISC (not more than 1 output for 1 second)	±100mA
Operating temperature range, TA: 74HCT, 74SC (Commercial) 54HCT (Military)	−40° C to +85° C −55°C to +125°C
Storage temperature, TS	−65°C to +150°C
Power dissipation, PD	500mW

Recommended Operating Conditions

Symbol	Parameter	54HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
VCC	Supply voltage	4.50	5.00	5.50	4.75	5.00	5.25	V	
VI	Input Voltage	0		VCC	0		VCC	V	
TA	Operating free-air temperature	−55		125	−40		85	°C	
VCCF	Functional operating VCC Range	3.00		6.00	3.00		6.00	V	

Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	54HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
VIH	High-level input voltage	2.0			2.0			V	
VIL	Low-level input voltage			0.8			0.8		
	Hysteresis (VT+ − VT−)		0.3			0.3		V	VCC = min
VOH	High-level output voltage	2.4			2.4			V	VCC = min, IOH = −5mA VIH = 2.0V VIL = 0.8V
VOL	Low-level output voltage			0.4			0.4		VCC = min, IOL = 6mA VIH = 2.0V VIL = 0.8V
II	Input current			5			1	μA	VCC = max, VI = VCC
ICC	Supply current		0.01	0.5		0.01	0.1	mA	VCC = max, outputs open and enabled, VI = VCC or GND

Switching Characteristics (VCC = 5.0V, TA = 25°C)

137, 237

Symbol	Parameter	54HCT/74HCT			74SC			Unit	Conditions
		min	typ	max	min	typ	max		
t_{PLH}	Propagation delay time, address to output			30			45	ns	CL = 50pF, RL = 1KΩ
t_{PHL}	Propagation delay time, address to output			30			45		
t_{PLH}	Propagation delay time, $\overline{E2}$ or E1 to output			30			45		
t_{PHL}	Propagation delay time, $\overline{E2}$ or E1 to output			30			45		
t_s	Set-up time, address to latch enable hold	10			10				
t_h	Hold time output, from latch disable	10			10				
C_I	Input capacitance		8			8		pF	

138, 238

Symbol	Parameter	54HCT/74HCT			74SC			Unit	Conditions
		min	typ	max	min	typ	max		
t_{PLH}	Propagation delay time, address to output			30			45	ns	CL = 50pF, RL = 1KΩ
t_{PHL}	Propagation delay time, address to output			30			45		
t_{PLH}	Propagation delay time, E to output			30			45		
t_{PHL}	Propagation delay time, E to output			30			45		
C_I	Input capacitance		8			8		pF	

139, 239

Symbol	Parameter	54HCT/74HCT			74SC			Unit	Conditions
		min	typ	max	min	typ	max		
t_{PLH}	Propagation delay time, address to output			25			45	ns	CL = 50pF, RL = 1KΩ
t_{PHL}	Propagation delay time, address to output			25			45		
t_{PLH}	Propagation delay time, E to output			25			45		
t_{PHL}	Propagation delay time, E to output			25			45		
C_I	Input capacitance		8			8		pF	

Ordering Information

1 of 8 Decoder with Latched Address

Package	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
16-pin plastic DIP	Inverted	74HCT137P	74SC137P	N/A
	Non-Inverted	74HCT237P	74SC237P	N/A
16-pin CERDIP	Inverted	74HCT137D	74SC137D	54HCT137D
	Non-Inverted	74HCT237D	74SC237D	54HCT237D
16-pin ceramic side-brazed DIP	Inverted	74HCT137C	74SC137C	54HCT137C
	Non-Inverted	74HCT237C	74SC237C	54HCT237C

1 of 8 Decoder

Package	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
16-pin plastic DIP	Inverted	74HCT138P	74SC138P	N/A
	Non-Inverted	74HCT238P	74SC238P	N/A
16-pin CERDIP	Inverted	74HCT138D	74SC138D	54HCT138D
	Non-Inverted	74HCT238D	74SC238D	54HCT238D
16-pin ceramic side-brazed DIP	Inverted	74HCT138C	74SC138C	54HCT138C
	Non-Inverted	74HCT238C	74SC238C	54HCT238C

Dual 1 of 4 Decoder

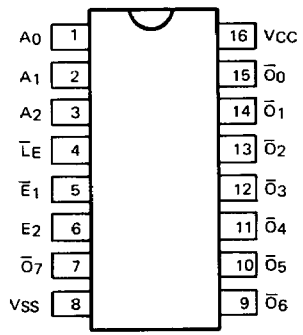
Package	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
16-pin plastic DIP	Inverted	74HCT139P	74SC139P	N/A
	Non-Inverted	74HCT239P	74SC239P	N/A
16-pin CERDIP	Inverted	74HCT139D	74SC139D	54HCT139D
	Non-Inverted	74HCT239D	74SC239D	54HCT239D
16-pin ceramic side-brazed DIP	Inverted	74HCT139C	74SC139C	54HCT139C
	Non-Inverted	74HCT239C	74SC239C	54HCT239C

Note: See Switching Waveforms and Test Circuit at end of this section.

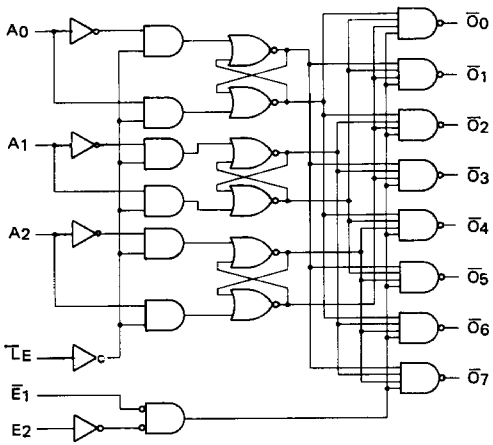
Pin Configurations, Functional Block Diagrams and Function Tables

137

Pin Configuration



Functional Block Diagram



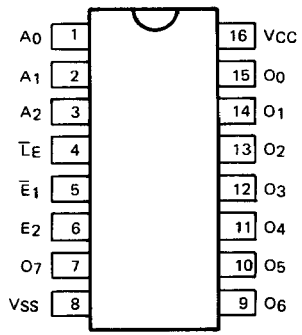
Function Table

Inputs						Outputs							
Enable			Select										
$\overline{LE}$	E2	$\overline{E}_1$	A2	A1	A0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L, all others H							

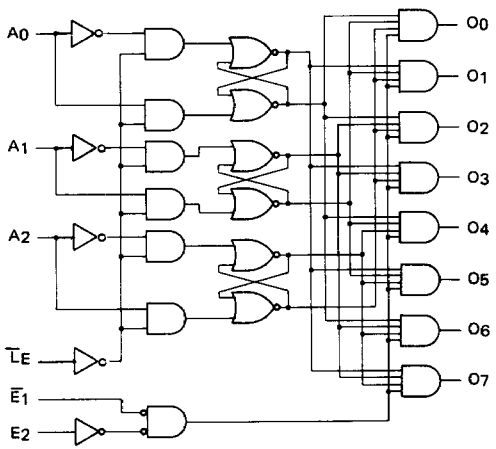
H = high level, L = low level, X = irrelevent

237

Pin Configuration



Functional Block Diagram



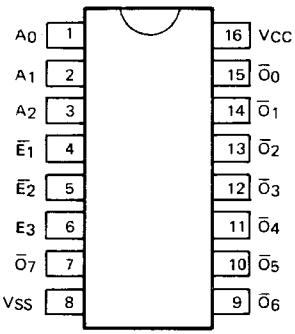
Function Table

Inputs						Outputs							
Enable			Select										
$\overline{LE}$	E2	$\overline{E}_1$	A2	A1	A0	O0	O1	O2	O3	O4	O5	O6	O7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address H, all others L							

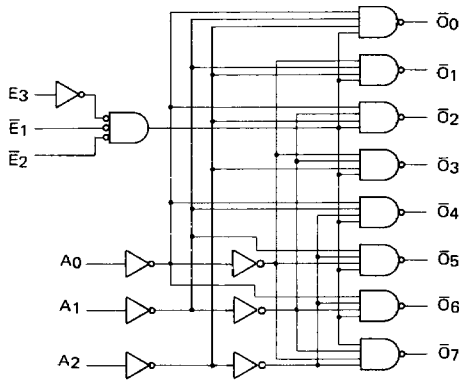
H = high level, L = low level, X = irrelevent

138

Pin Configuration



Functional Block Diagram



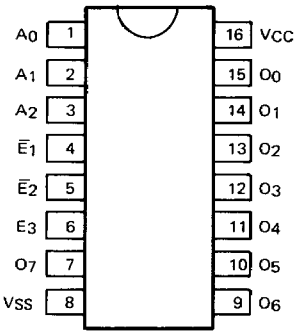
Function Table

Inputs					Outputs							
Enable			Select									
E3	$\overline{E}_1$	$\overline{E}_2$	A2	A1	A0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
X	H		X	X	X	H	H	H	H	H	H	H	H
L	X		X	X	X	H	H	H	H	H	H	H	H
H	L		L	L	L	L	H	H	H	H	H	H	H
H	L		L	L	H	H	L	H	H	H	H	H	H
H	L		L	H	L	H	H	L	H	H	H	H	H
H	L		L	H	H	H	H	H	L	H	H	H	H
H	L		H	L	L	H	H	H	H	L	H	H	H
H	L		H	L	H	H	H	H	H	H	L	H	H
H	L		H	H	L	H	H	H	H	H	H	L	H
H	L		H	H	H	H	H	H	H	H	H	H	L

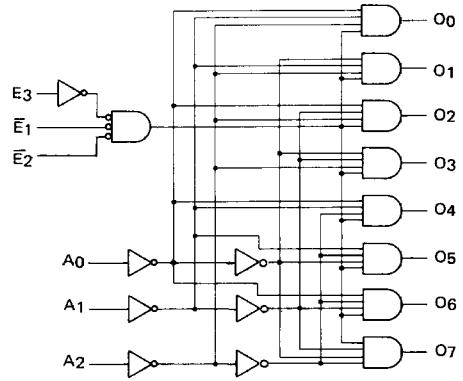
H = high level, L = low level, X = irrelevent

238

Pin Configuration



Functional Block Diagram



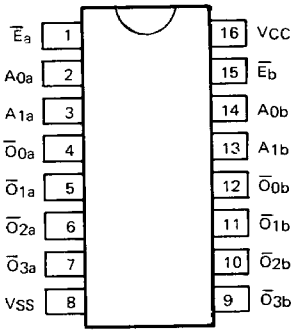
Function Table

Inputs					Outputs							
Enable			Select									
E3	$\overline{E}_1$	$\overline{E}_2$	A2	A1	A0	O0	O1	O2	O3	O4	O5	O6	O7
X	H		X	X	X	L	L	L	L	L	L	L	L
L	X		X	X	X	L	L	L	L	L	L	L	L
H	L		L	L	L	H	L	L	L	L	L	L	L
H	L		L	L	H	L	H	L	L	L	L	L	L
H	L		L	H	L	L	L	H	L	L	L	L	L
H	L		L	H	H	L	L	L	H	L	L	L	L
H	L		H	L	L	L	L	L	L	H	L	L	L
H	L		H	L	H	L	L	L	L	L	H	L	L
H	L		H	H	L	L	L	L	L	L	L	H	L
H	L		H	H	H	L	L	L	L	L	L	L	H

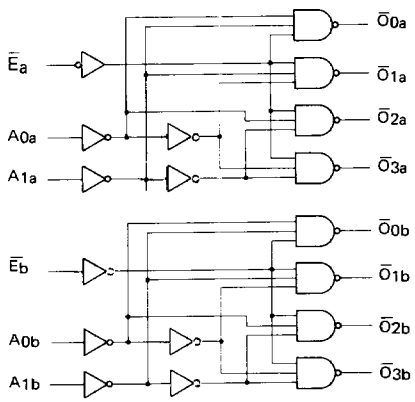
H = high level, L = low level, X = irrelevent

139

Pin Configuration



Functional Block Diagram



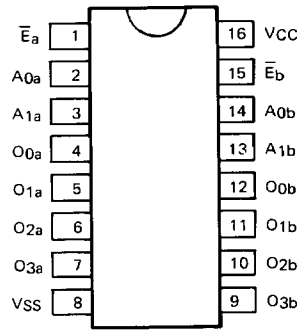
Function Table

Inputs			Outputs			
Enable	Select					
$\overline{E}$	A1	A0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

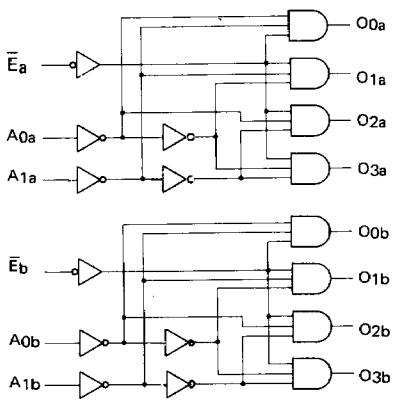
H = high level, L = low level, X = irrelevent

239

Pin Configuration



Functional Block Diagram



Function Table

Inputs			Outputs			
Enable	Select					
$\overline{E}$	A1	A0	O0	O1	O2	O3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

H = high level, L = low level, X = irrelevent