



Integrated Device Technology, Inc.

CMOS SyncFIFO™
64 X 9, 256 x 9, 512 x 9,
1024 X 9, 2048 X 9 and 4096 x 9

IDT72421
IDT72201
IDT72211
IDT72221
IDT72231
IDT72241

FEATURES:

- 64 x 9-bit organization (IDT72421)
- 256 x 9-bit organization (IDT72201)
- 512 x 9-bit organization (IDT72211)
- 1024 x 9-bit organization (IDT72221)
- 2048 x 9-bit organization (IDT72231)
- 4096 x 9-bit organization (IDT72241)
- 12 ns read/write cycle time (IDT72421/72201/72211)
- 15 ns read/write cycle time (IDT72221/72231/72241)
- Read and write clocks can be independent
- Dual-Ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be set to any depth
- Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively
- Output enable puts output data bus in high-impedance state
- Advanced submicron CMOS technology
- Available in 32-pin plastic leaded chip carrier (PLCC), ceramic leadless chip carrier (LCC), and 32-pin Thin Quad Flat Pack (TQFP) on 72421, 72201 and 72211
- For Through-Hole product please see the IDT72420/72200/72210/72220/72230/72240 data sheet
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

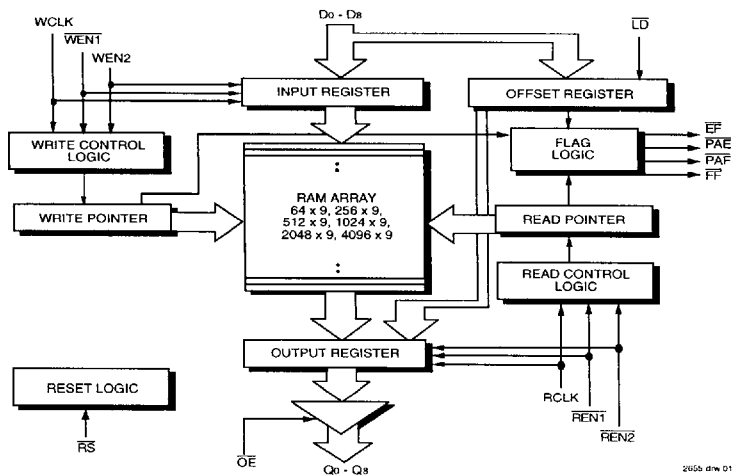
The IDT72421/72201/72211/72221/72231/72241 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. The IDT72421/72201/72211/72221/72231/72241 have a 64, 256, 512, 1024, 2048, and 4096 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks and interprocessor communication.

These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two write enable pins (WEN1, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins (REN1, REN2). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An output enable pin (OE) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty (EF) and Full (FF). Two programmable flags, Almost-Empty (PAE) and Almost-Full (PAF), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for PAE and PAF, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the load pin (LD).

The IDT72421/72201/72211/72221/72231/72241 are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

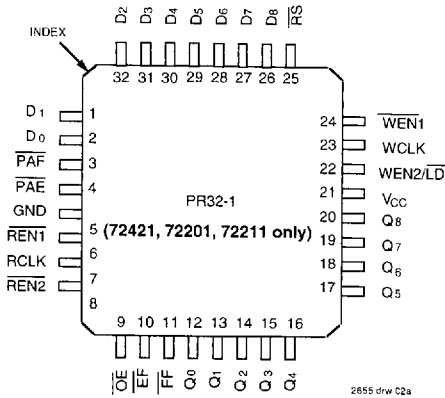


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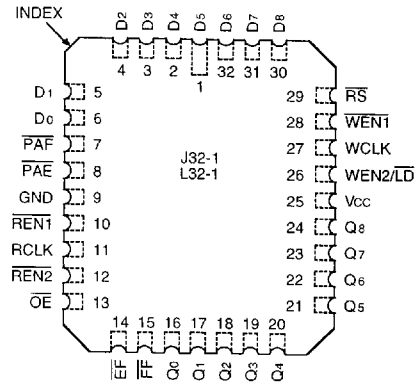
MILITARY AND COMMERCIAL TEMPERATURE RANGES

DECEMBER 1996

PIN CONFIGURATION



**TQFP
TOP VIEW**



**LCC/PLCC
TOP VIEW**

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D8	Data Inputs	I	Data inputs for a 9-bit bus.
RS	Reset	I	When RS is set LOW, internal read and write pointers are set to the first location of the RAM array, FF and PAF go HIGH, and PAE and EF go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
WEN1	Write Enable 1	I	If the FIFO is configured to have programmable flags, WEN1 is the only write enable pin. When WEN1 is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW.
WEN2/LD	Write Enable 2/ Load	I	The FIFO is configured at reset to have either two write enables or programmable flags. If WEN2/LD is HIGH at reset, this pin operates as a second write enable. If WEN2/LD is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
Q0-Q8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when REN1 and REN2 are asserted.
REN1	Read Enable 1	I	When REN1 and REN2 are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the EF is LOW.
REN2	Read Enable 2	I	When REN1 and REN2 are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the EF is LOW.
OE	Output Enable	I	When OE is LOW, the data output bus is active. If OE is HIGH, the output data bus will be in a high-impedance state.
EF	Empty Flag	O	When EF is LOW, the FIFO is empty and further data reads from the output are inhibited. When EF is HIGH, the FIFO is not empty. EF is synchronized to RCLK.
PAE	Programmable Almost-Empty Flag	O	When PAE is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. PAE is synchronized to RCLK.
PAF	Programmable Almost-Full Flag	O	When PAF is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. PAF is synchronized to WCLK.
FF	Full Flag	O	When FF is LOW, the FIFO is full and further data writes into the input are inhibited. When FF is HIGH, the FIFO is not full. FF is synchronized to WCLK.
VCC	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +135	°C
IOUT	DC Output Current	50	50	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL	Input Low Voltage Commercial & Military	—	—	0.8	V

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CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN ⁽²⁾	Input Capacitance	VIN = 0V	10	pF
COUT ^(1,2)	Output Capacitance	VOUT = 0V	10	pF

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NOTES:

- With output deselected (\overline{OE} = HIGH).
- Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72421 IDT72201 IDT72211 Commercial			IDT72421 IDT72201 IDT72211 Military			Unit
		tCLK = 12, 15, 20, 25, 35, 50ns Min.	Typ.	Max.	tCLK = 20, 25, 35, 50ns Min.	Typ.	Max.	
ILI ⁽¹⁾	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
ILO ⁽²⁾	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = -2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8mA	—	—	0.4	—	—	0.4	V
Icc ⁽³⁾	Active Power Supply Current	—	—	80	—	—	100	mA

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Symbol	Parameter	IDT72221 IDT72231 IDT72241 Commercial			IDT72221 IDT72231 IDT72241 Military			Unit
		tCLK = 15, 20, 25, 35, 50ns Min.	Typ.	Max.	tCLK = 25, 35, 50ns Min.	Typ.	Max.	
ILI ⁽¹⁾	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
ILO ⁽²⁾	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = -2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8mA	—	—	0.4	—	—	0.4	V
Icc ⁽⁴⁾	Active Power Supply Current	—	—	80	—	—	100	mA

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NOTES:

- Measurements with 0.4 ≤ VIN ≤ VCC.
- OE ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
- Measurements are made with outputs unloaded. Tested at fCLK = 20MHz.
- Typical Icc1 = 30 + (fCLK*0.5/MHz) + (fCLK*CL*0.02/MHz-pF) mA
 (4) Typical Icc1 = 32 + (fCLK*0.6/MHz) + (fCLK*CL*0.02/MHz-pF) mA
 fCLK = 1/tCLK
 CL = external capacitive load (30pF typical)

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AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	Commercial		Commercial & Military		Com'l.		Com'l./Mil.		Unit						
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.							
											72421L12	72421L15	72421L20	72421L25	72421L35	72421L50
											72201L12	72201L15	72201L20	72201L25	72201L35	72201L50
fS	Clock Cycle Frequency	—	83.3	—	66.7	—	50	—	40	—	28.6	—	20	ns		
tA	Data Access Time	2	8	2	10	2	12	3	15	3	20	3	25	ns		
tCLK	Clock Cycle Time	12	—	15	—	20	—	25	—	35	—	50	—	ns		
tCLKH	Clock High Time	5	—	6	—	8	—	10	—	14	—	20	—	ns		
tCLKL	Clock Low Time	5	—	6	—	8	—	10	—	14	—	20	—	ns		
tDS	Data Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns		
tDH	Data Hold Time	0	—	1	—	1	—	1	—	2	—	2	—	ns		
tENS	Enable Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns		
tENH	Enable Hold Time	0	—	1	—	1	—	1	—	2	—	2	—	ns		
tRS	Reset Pulse Width ⁽¹⁾	12	—	15	—	20	—	25	—	35	—	50	—	ns		
tRSS	Reset Set-up Time	12	—	15	—	20	—	25	—	35	—	50	—	ns		
tRSR	Reset Recovery Time	12	—	15	—	20	—	25	—	35	—	50	—	ns		
tRSF	Reset to Flag and Output Time	—	12	—	15	—	20	—	25	—	35	—	50	ns		
tOLZ	Output Enable to Output in Low-Z ⁽²⁾	0	—	0	—	0	—	0	—	0	—	0	—	ns		
tOE	Output Enable to Output Valid	3	7	3	8	3	10	3	13	3	15	3	28	ns		
tOHZ	Output Enable to Output in High-Z ⁽²⁾	3	7	3	8	3	10	3	13	3	15	3	28	ns		
tWFF	Write Clock to Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns		
tREF	Read Clock to Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns		
tAF	Write Clock to Almost-Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns		
tAE	Read Clock to Almost-Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns		
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	5	—	6	—	8	—	10	—	12	—	15	—	ns		
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	22	—	28	—	35	—	40	—	42	—	45	—	ns		

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to + 70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial		Commercial & Military		Com'l.		Com'l./Mil.		Unit										
		72221L12	72221L15	72221L20	72221L25	72221L35	72221L50	72231L12	72231L15		72231L20	72231L25	72231L35	72231L50	72241L12	72241L15	72241L20	72241L25	72241L35	72241L50
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tS	Clock Cycle Frequency	—	83.3	—	66.7	—	50	—	40	—	28.6	—	20							MHz
tA	Data Access Time	2	8	2	10	2	12	3	15	3	20	3	25							ns
tCLK	Clock Cycle Time	12	—	15	—	20	—	25	—	35	—	50	—							ns
tCLKH	Clock High Time	5	—	6	—	8	—	10	—	14	—	20	—							ns
tCLKL	Clock Low Time	5	—	6	—	8	—	10	—	14	—	20	—							ns
tDS	Data Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—							ns
tDH	Data Hold Time	0	—	1	—	1	—	1	—	2	—	2	—							ns
tENS	Enable Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—							ns
tENH	Enable Hold Time	0	—	1	—	1	—	1	—	2	—	2	—							ns
tRS	Reset Pulse Width ⁽¹⁾	12	—	15	—	20	—	25	—	35	—	50	—							ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	25	—	35	—	50	—							ns
tRSR	Reset Recovery Time	12	—	15	—	20	—	25	—	35	—	50	—							ns
tRSF	Reset to Flag and Output Time	—	12	—	15	—	20	—	25	—	35	—	50							ns
tOLZ	Output Enable to Output in Low-Z ⁽²⁾	0	—	0	—	0	—	0	—	0	—	0	—							ns
tOE	Output Enable to Output Valid	3	7	3	8	3	10	3	13	3	15	3	28							ns
tOHZ	Output Enable to Output in High-Z ⁽²⁾	3	7	3	8	3	10	3	13	3	15	3	28							ns
tWFF	Write Clock to Full Flag	—	8	—	10	—	12	—	15	—	20	—	30							ns
tREF	Read Clock to Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30							ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	8	—	10	—	12	—	15	—	20	—	30							ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30							ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	5	—	6	—	8	—	10	—	12	—	15	—							ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Programmable Almost-Full Flag	22	—	28	—	35	—	40	—	42	—	45	—							ns

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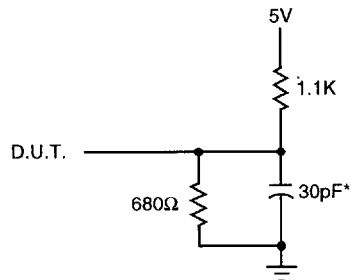
NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D₀ - D₈) — Data inputs for 9-bit wide data.

CONTROLS:

Reset (\overline{RS}) — Reset is accomplished whenever the Reset (\overline{RS}) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag (\overline{FF}) and Programmable Almost-Full Flag (\overline{PAF}) will be reset to HIGH after \overline{RSF} . The Empty Flag (\overline{EF}) and Programmable Almost-Empty Flag (\overline{PAE}) will be reset to LOW after \overline{RSF} . During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag (\overline{FF}) and Programmable Almost-Full Flag (\overline{PAF}) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$) — If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is low, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag (\overline{FF}) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag (\overline{FF}) will go HIGH after \overline{twFF} , allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag (\overline{EF}) and Programmable Almost-Empty Flag (\overline{PAE}) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN1}$, $\overline{REN2}$) — When both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When either Read Enable ($\overline{REN1}$, $\overline{REN2}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag (\overline{EF}) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag (\overline{EF}) will go HIGH after \overline{tREF} and a valid read can begin. The Read Enables ($\overline{REN1}$, $\overline{REN2}$) are ignored when the FIFO is empty.

Output Enable (\overline{OE}) — When Output Enable (\overline{OE}) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable (\overline{OE}) is disabled (HIGH), the Q output data bus is in a high-impedance state.

Write Enable 2/Load ($\overline{WEN2/LD}$) — This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load ($\overline{WEN2/LD}$) is set high at Reset (\overline{RS} = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load ($\overline{WEN2/LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is HIGH and/or Write Enable 2/Load ($\overline{WEN2/LD}$) is LOW, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag (\overline{FF}) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag (\overline{FF}) will go HIGH after \overline{twFF} , allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load ($\overline{WEN2/LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load ($\overline{WEN2/LD}$) is set LOW at Reset (\overline{RS} = low). The IDT72421/72201/72211/72221/72231/72241 devices contain four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load ($\overline{WEN2/LD}$) are set low, data on the inputs D is written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

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However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/LD) pin HIGH, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/LD) pin is set LOW, and Write Enable 1 (WEN1) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Write Enable 2/Load (WEN2/LD) pin is set low and both Read Enables (REN1, REN2) are set LOW. Data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

A read and write should not be performed simultaneously to the offset registers.

LD	WEN1	WCLK ⁽¹⁾	Selection
0	0		Empty Offset (LSB) → Empty Offset (MSB) → Full Offset (LSB) → Full Offset (MSB) →
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE: 2855 drw 04
 1. The same selection sequence applies to reading from the registers. REN1 and REN2 are enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

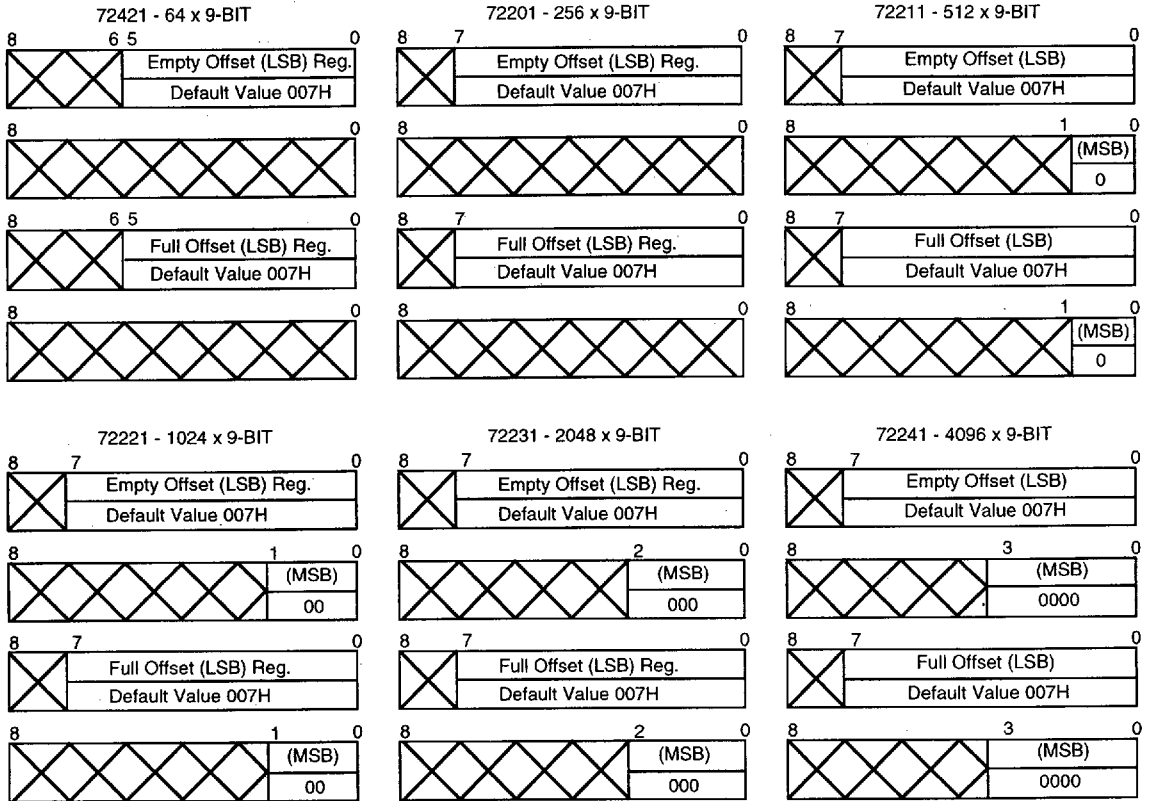


Figure 3. Offset Register Location and Default Values

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OUTPUTS:

Full Flag (FF) — The Full Flag (FF) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset (RS), the Full Flag (FF) will go LOW after 64 writes for the IDT72421, 256 writes for the IDT72201, 512 writes for the IDT72211, 1024 writes for the IDT72221, 2048 writes for the IDT72231, and 4096 writes for the IDT72241.

The Full Flag (FF) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag (EF) — The Empty Flag (EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag (EF) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag (PAF) — The Programmable Almost-Full Flag (PAF) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset (RS), the Programmable Almost-Full Flag (PAF) will go LOW after (64-m) writes for the IDT72421, (256-m) writes for the IDT72201, (512-m) writes for the IDT72211, (1024-m) writes for the IDT72221, (2048-m) writes

for the IDT72231, and (4096-m) writes for the IDT72241. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag (PAF) will go LOW at Full-7 words.

The Programmable Almost-Full Flag (PAF) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag (PAE) — The Programmable Almost-Empty Flag (PAE) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag (PAE) will go HIGH after "n+1" for the IDT72421/72201/72211/72221/72231/72241.

If there is no Empty offset specified, the Programmable Almost-Empty Flag (PAE) will go LOW at Empty+7 words.

The Programmable Almost-Empty Flag (PAE) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q0 - Q8) — Data outputs for a 9-bit wide data.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO			FF	PAF	PAE	EF
72421	72201	72211				
0	0	0	H	H	L	L
1 to n ⁽¹⁾	1 to n ⁽¹⁾	1 to n ⁽¹⁾	H	H	L	H
(n+1) to (64-(m+1))	(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	H	H	H	H
(64-m) ⁽²⁾ to 63	(256-m) ⁽²⁾ to 255	(512-m) ⁽²⁾ to 511	H	L	H	H
64	256	512	L	L	H	H

2655 tbl 11

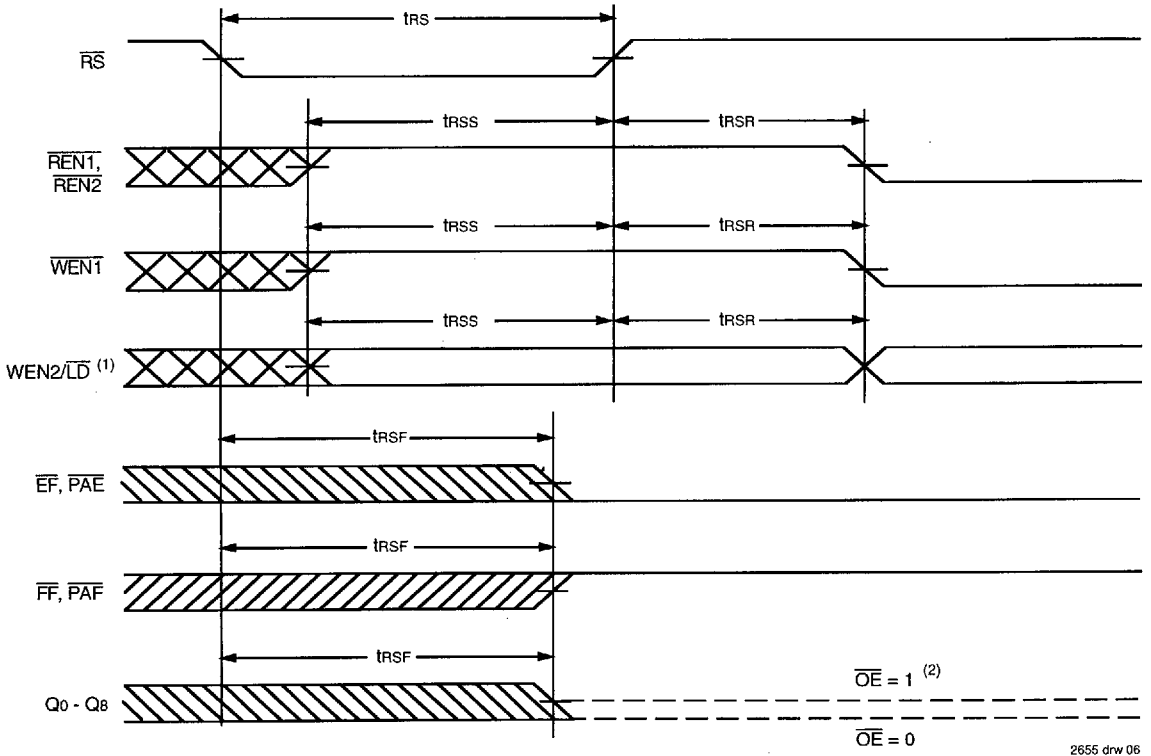
NUMBER OF WORDS IN FIFO			FF	PAF	PAE	EF
72221	72231	72241				
0	0	0	H	H	L	L
1 to n ⁽¹⁾	1 to n ⁽¹⁾	1 to n ⁽¹⁾	H	H	L	H
(n+1) to (1024-(m+1))	(n+1) to (2048-(m+1))	(n+1) to (4096-(m+1))	H	H	H	H
(1024-m) ⁽²⁾ to 1023	(2048-m) ⁽²⁾ to 2047	(4096-m) ⁽²⁾ to 4095	H	L	H	H
1024	2048	4096	L	L	H	H

NOTES:

1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)

2655 tbl 11

■ 4825771 0026439 808 ■

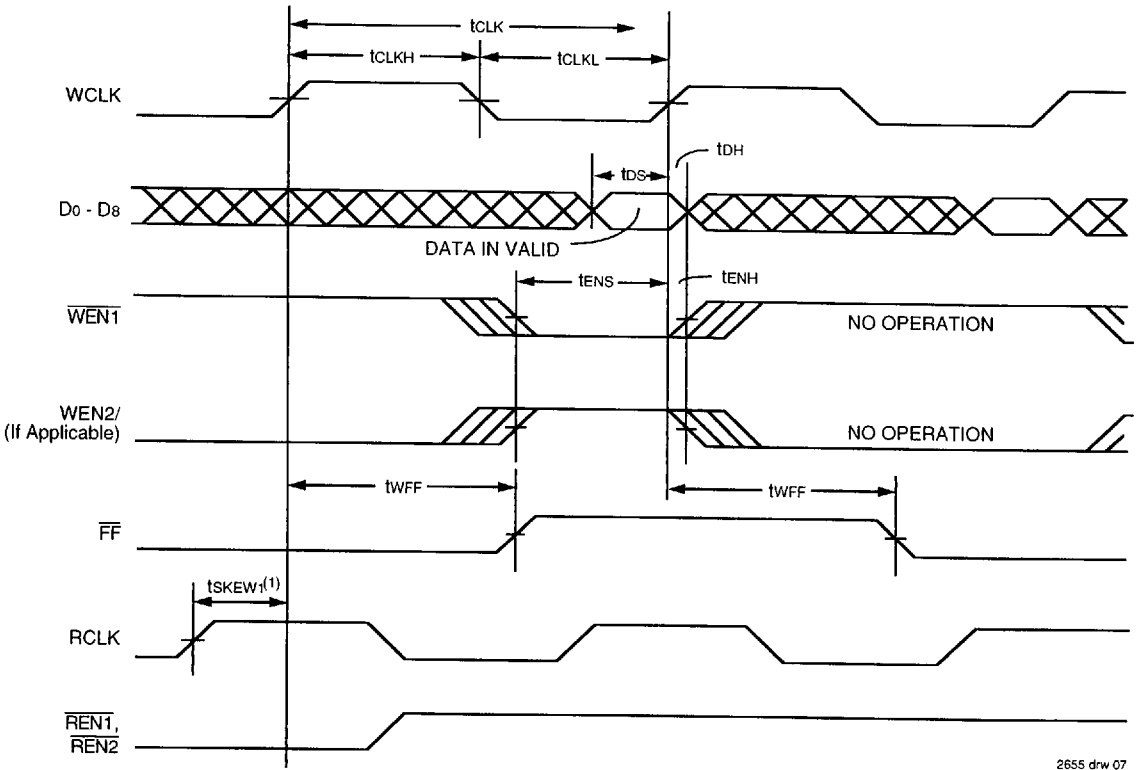


2655 drw 06

NOTES:

1. Holding $\overline{WEN2}/\overline{LD}$ HIGH during reset will make the pin act as a second write enable pin. Holding $\overline{WEN2}/\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be LOW if $\overline{OE} = 0$ and tri-state if $\overline{OE} = 1$.
3. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing



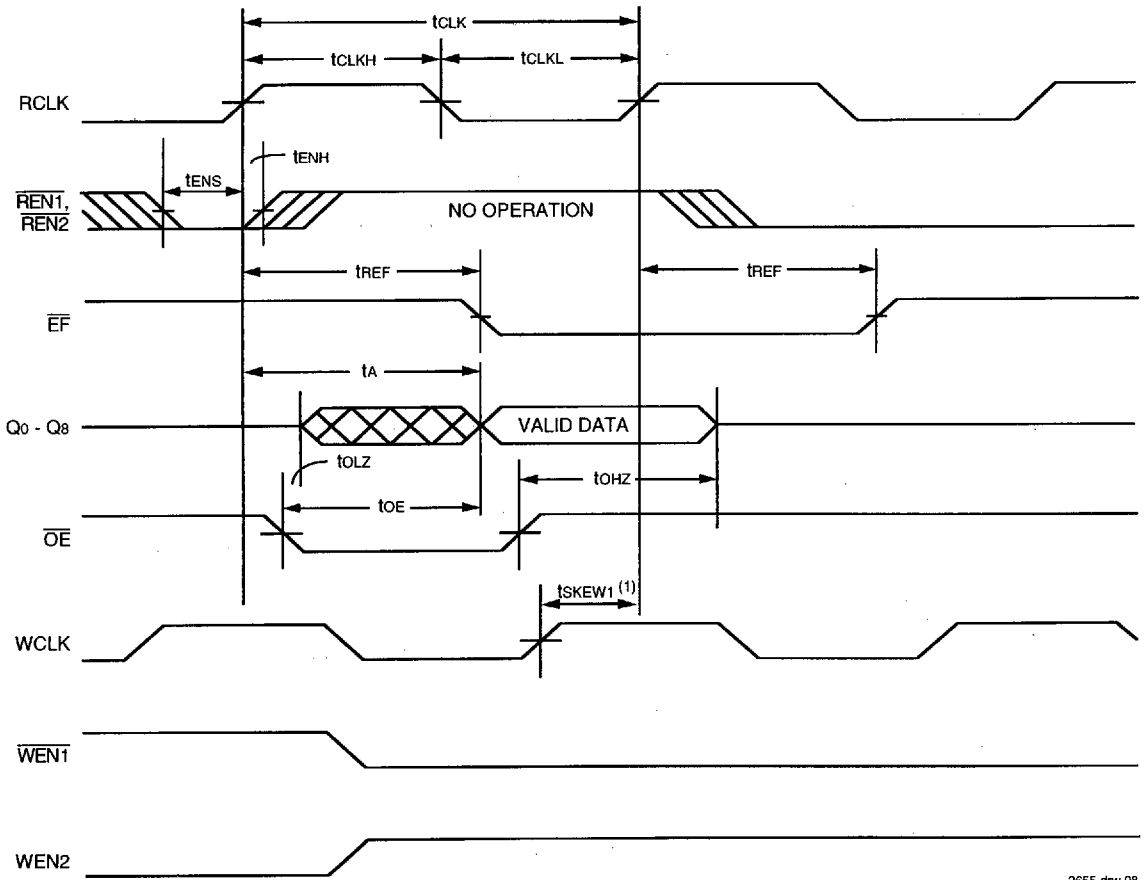
2655 drw 07

NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then FF may not change state until the next WCLK edge.

Figure 5. Write Cycle Timing

5

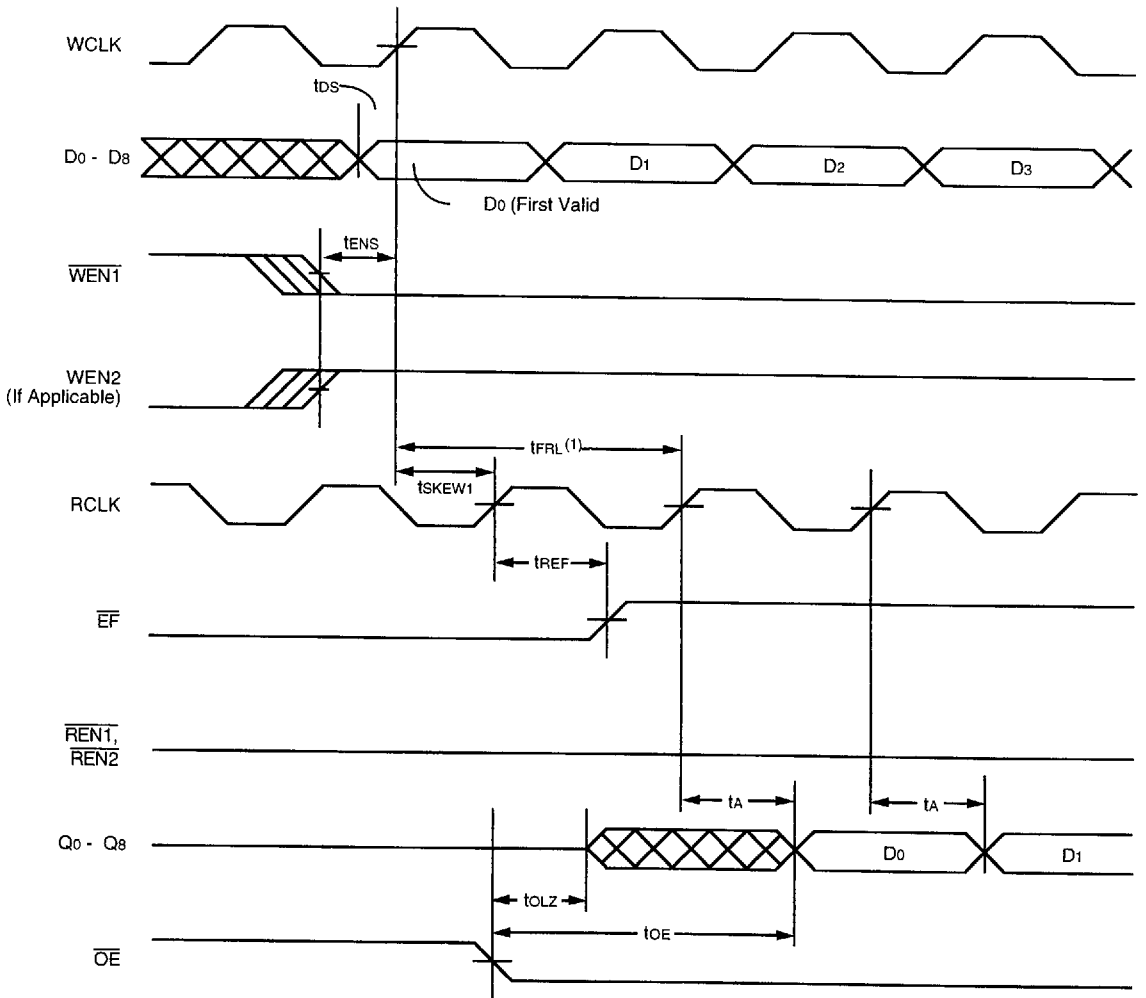


2655 drw 08

NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for \overline{EF} to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{EF} may not change state until the next RCLK edge. Figure 6. Read Cycle Timing

Figure 6. Read Cycle Timing



5

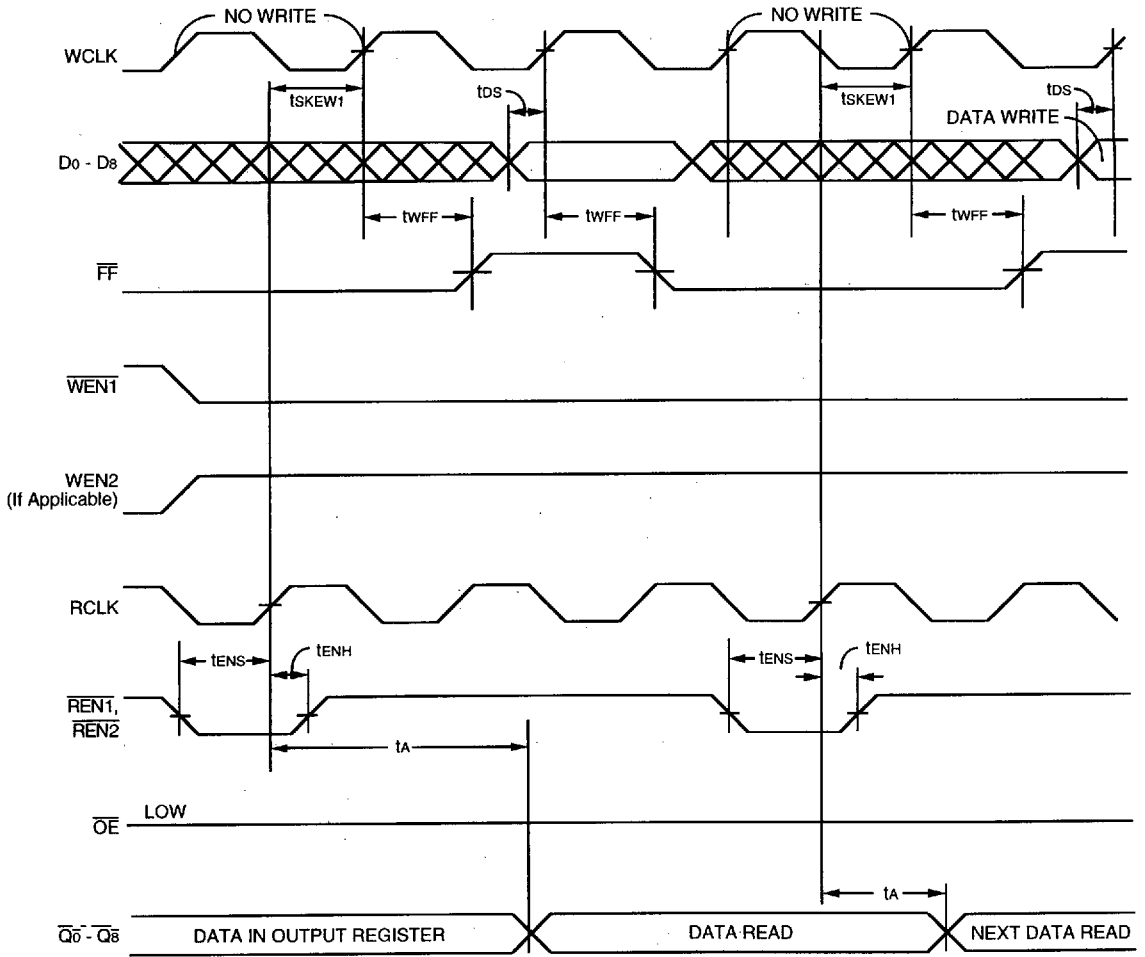
2655 drw 09

NOTE:

- When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
 If $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
 The Latency Timings apply only at the Empty Boundary (EF = LOW).

Figure 7. First Data Word Latency Timing

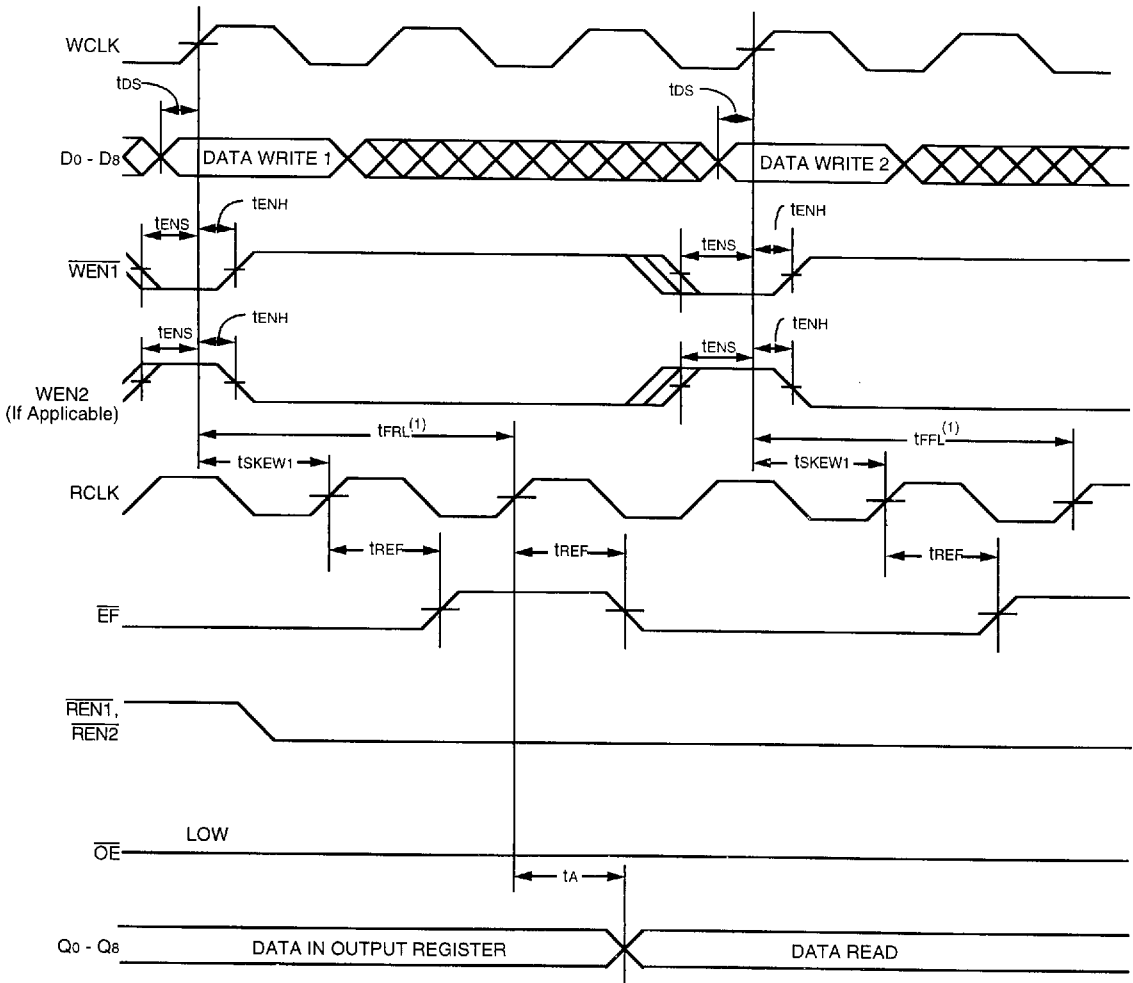
482577J 0026443 239



2655 drw 10

Figure 8. Full Flag Timing

■ 4825771 0026444 175 ■



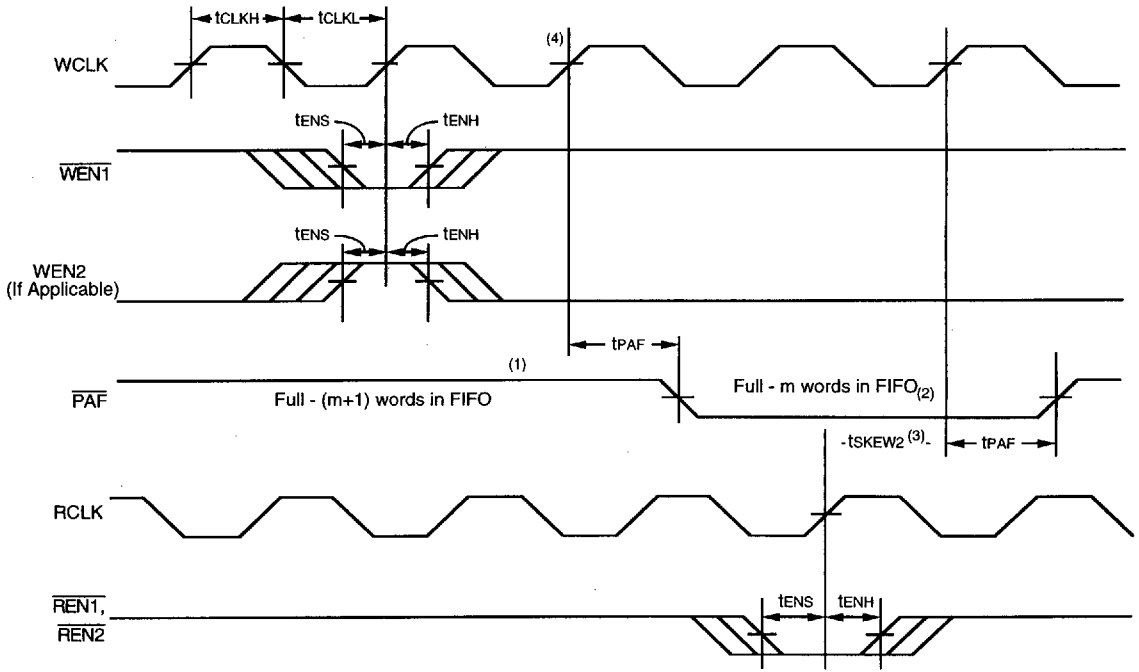
5

2655 drw 11

NOTE:
 1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
 If $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
 The Latency Timings apply only at the Empty Boundary ($\overline{EF} = \text{LOW}$).

Figure 9. Empty Flag Timing

4825771 0026445 001



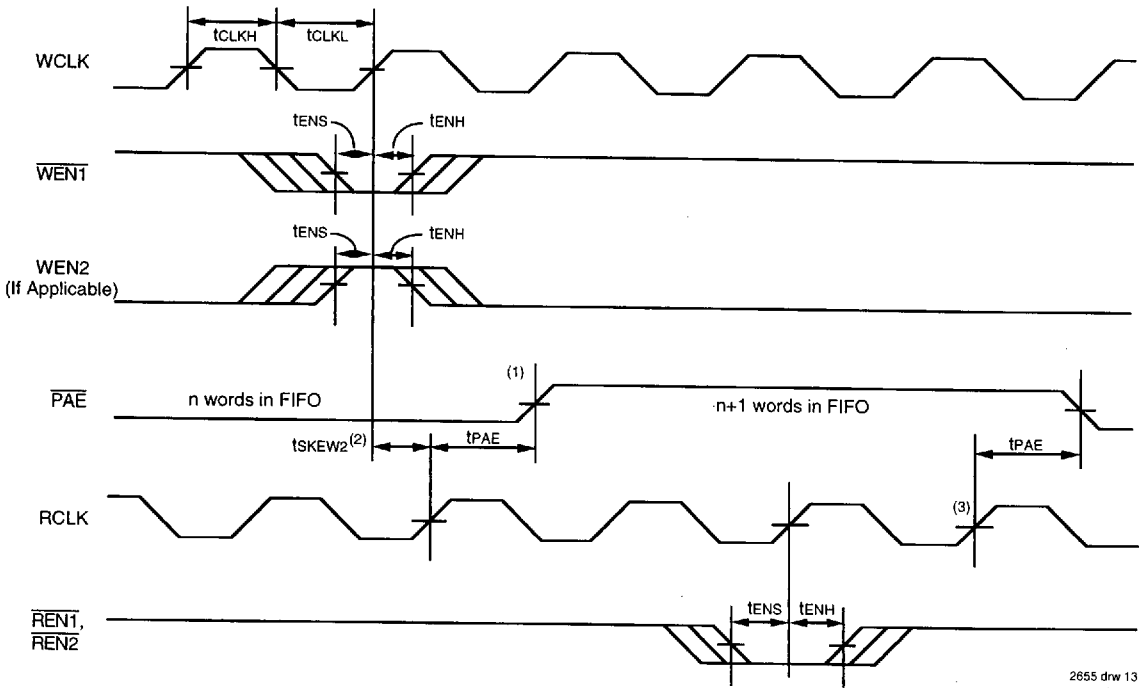
2655 dnr 12

NOTES:

1. PAF offset = m.
2. 64 - m words in for IDT72421, 256 - m words in FIFO for IDT72201, 512 - m words for IDT72211, 1024 - m words for IDT72221, 2048 - m words for IDT72231, 4096 - m words for IDT72241.
3. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for PAF to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then PAF may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when PAF goes LOW.

Figure 10. Programmable Full Flag Timing

482577J 0026446 T48

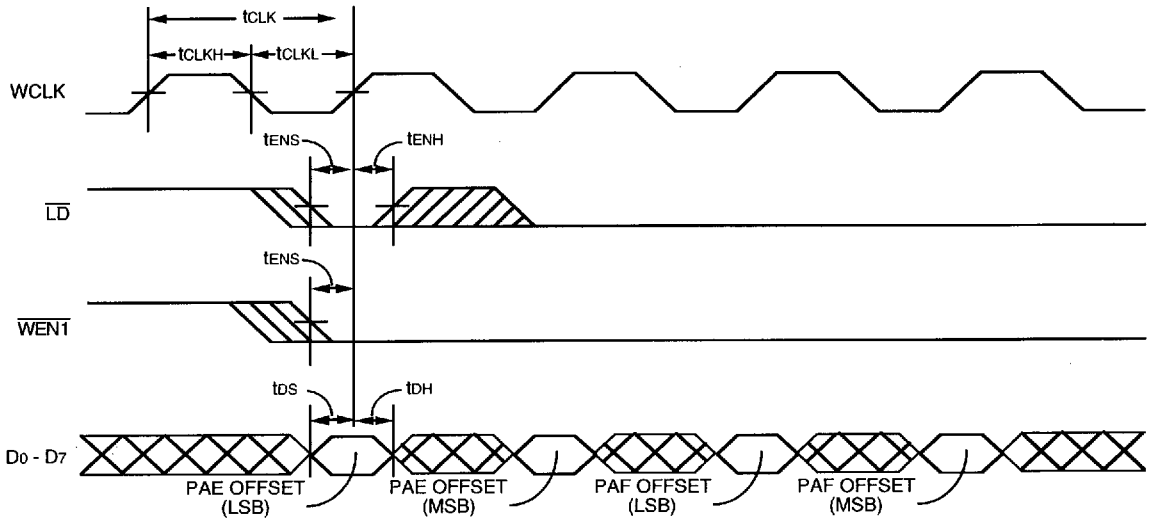


2655 drw 13

5

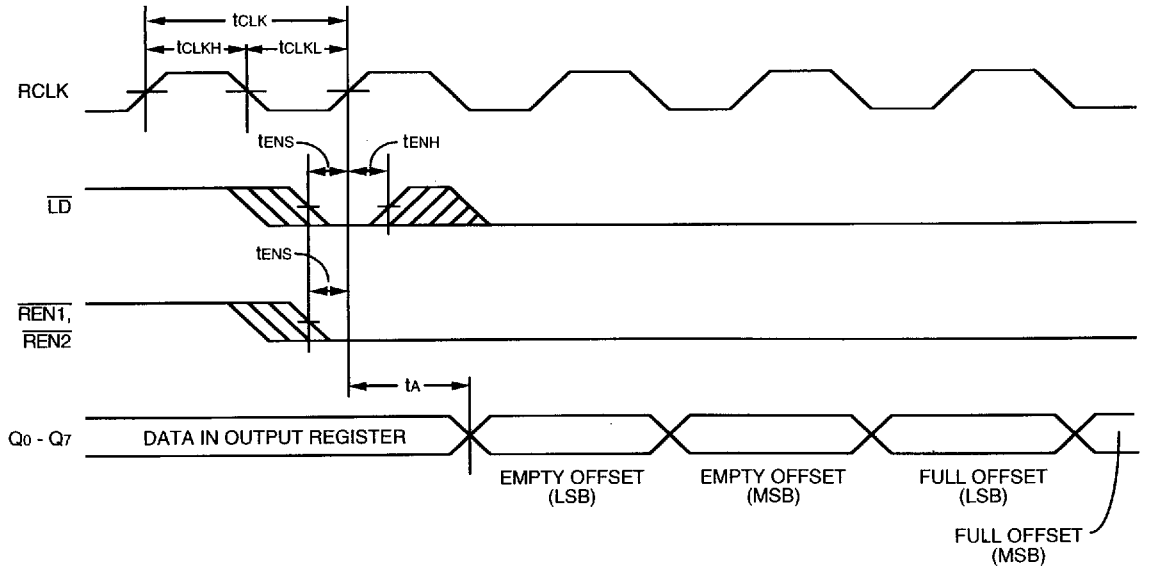
- NOTES:**
1. PAE offset = n.
 2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for \overline{PAE} to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2} , then \overline{PAE} may not change state until the next RCLK rising edge.
 3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when \overline{PAE} goes LOW.

Figure 11. Programmable Empty Flag Timing



2655 drw 14

Figure 12. Write Offset Registers Timing



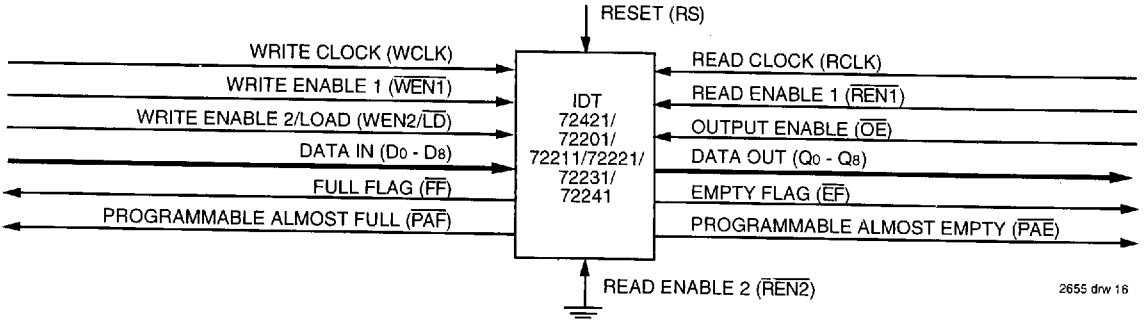
2655 drw 15

Figure 13. Read Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72421/72201/72211/72221/72231/72241 may be used when the application requirements are for 64/256/512/1024/2048/4096 words or less. When the IDT72421/72201/72211/72221/

72231/72241 are in a Single Device Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load ($\overline{WEN2}/\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

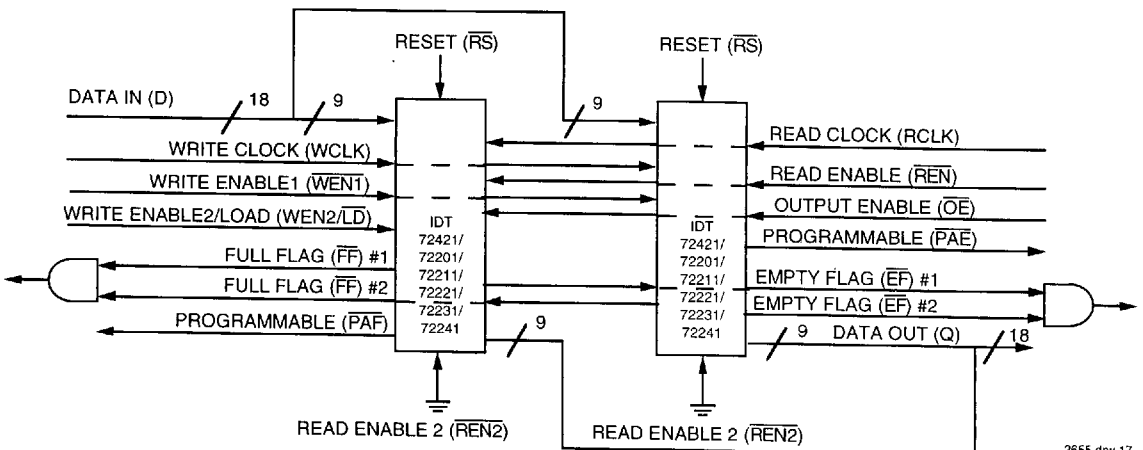


2655 drw 16

Figure 14. Block Diagram of Single 64 x 9/256 x 9/512 x 9/1024 x 9/2048 x 9/4096 x 9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags (\overline{EF} and \overline{FF}). The partial status flags (\overline{AE} and \overline{AF}) can be detected from any one device. Figure 15 demonstrates a 18-bit word width by using two IDT72421/72201/72211/72221/72231/72241s. Any word width can be attained by adding additional IDT72421/72201/72211/72221/72231/72241s.

When the IDT72421/72201/72211/72221/72231/72241 are in a Width Expansion Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load ($\overline{WEN2}/\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.



2655 drw 17

Figure 15. Block Diagram of 64 x 18/256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO Used in a Width Expansion Configuration

482577J 0026449 757

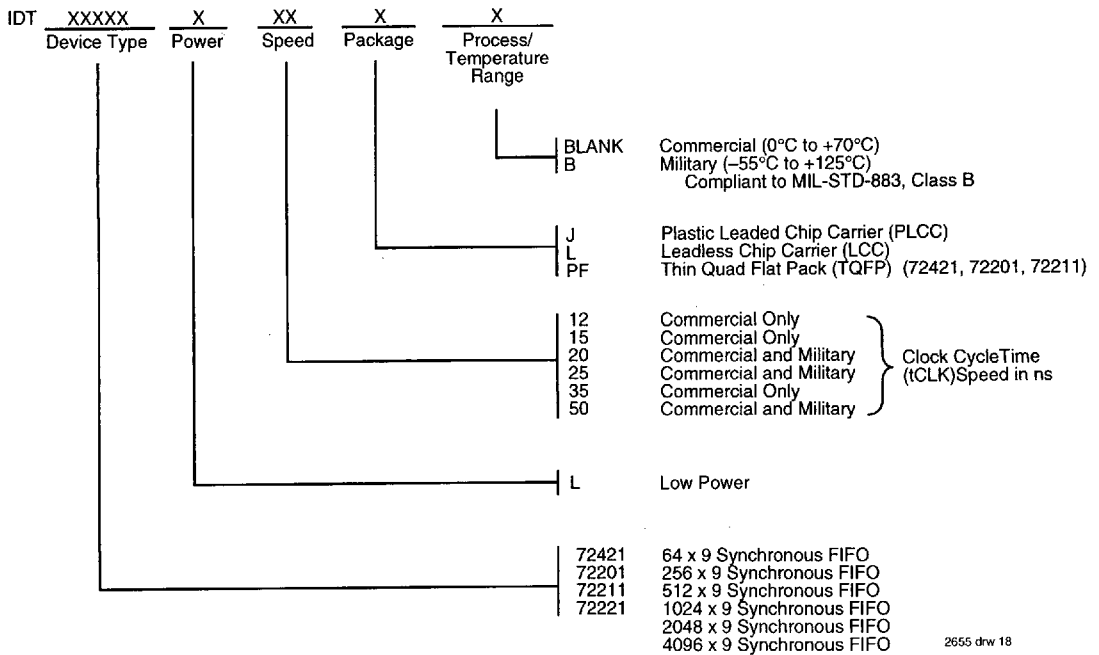
DEPTH EXPANSION - The IDT72421/72211/72211/72221/72231/72241 can be adapted to applications when the requirements are for greater than 64/256/512/1024/2048/4096 words. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data

access from one device to the next in a sequential manner. The IDT72421/72211/72211/72221/72231/72241 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/ \overline{LD} pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

Please see the Application Note "DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



2655 drw 18

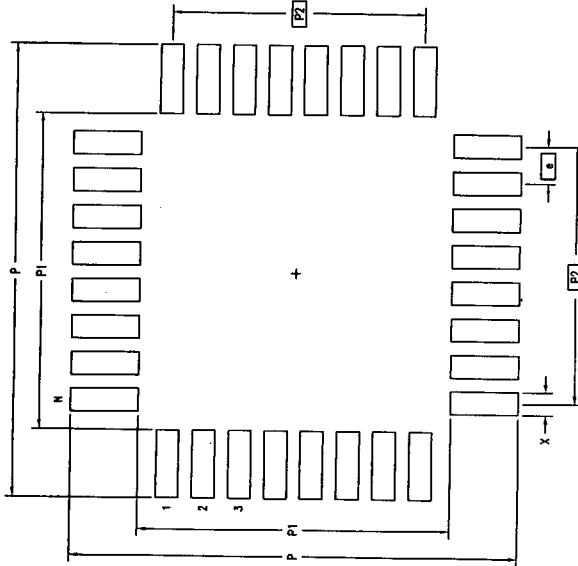
4825771 0026450 479

PACKAGE DIAGRAM OUTLINES
TQFP (Continued)

DCN	REV	DESCRIPTION	DATE	APPROVED
28215	00	INITIAL RELEASE	10/15/95	

DWG #	PR32-1	N	P	E
JEDEC VARIATION				
BBA				
MIN	MAX			
A	-	1.60		
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC	4		
D1	7.00 BSC	5.2		
E	9.00 BSC	4		
E1	7.00 BSC	5.2		
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	-	-	.10	
ddd	-	-	.20	

LAND PATTERN DIMENSIONS



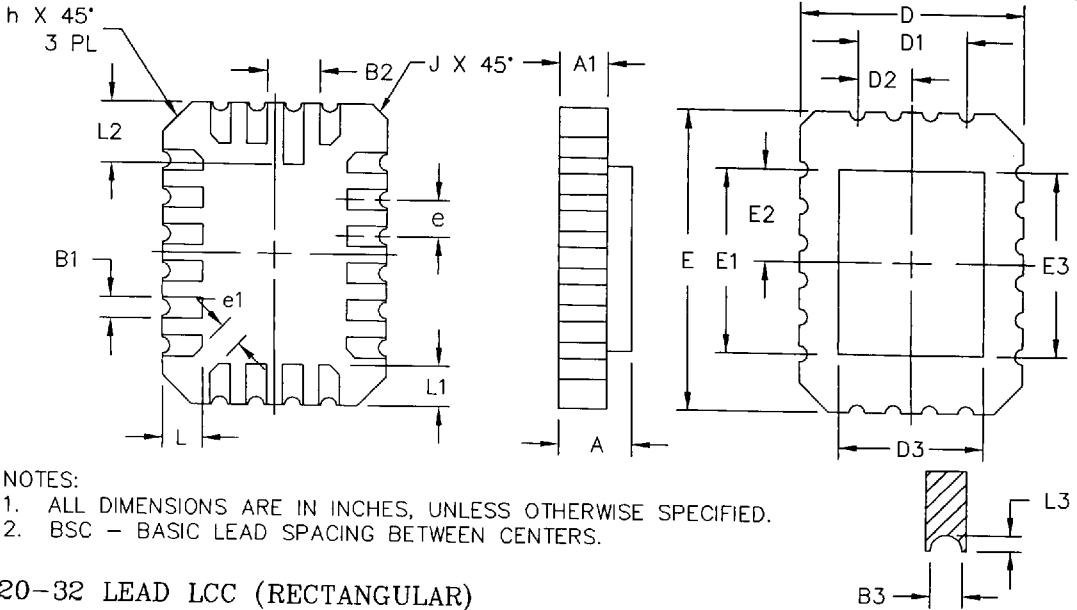
	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.60	BSC
X	.40	.60
e	.80	BSC
N	32	

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1992
- TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- DATUMS [A-B] AND [D-E] TO BE DETERMINED AT DATUM PLANE [H-I]
- DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [C-D]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION BBA

RELEASES UNLESS SPECIFIED DECIMAL SIZE 33224	INTEGRATED DEVICE TECHNOLOGY, INC. 2875 STANDER HWY, SANTA CRUZ, CA 95054 PHONE: (408) 737-0118 FAX: (408) 492-8874 TEC 910-538-3070
APPROVALS DRAWN BY CHECKED	TITLE PR PACKAGE OUTLINE 7.0 X 7.0 X 1.4 mm TQFP 1.00/10 FORM
SIZE C	DRAWING NO. PSC-4052
REV 00	SHEET 2 OF 2

LEADLESS CHIP CARRIERS (Continued)



NOTES:

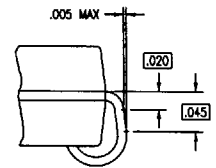
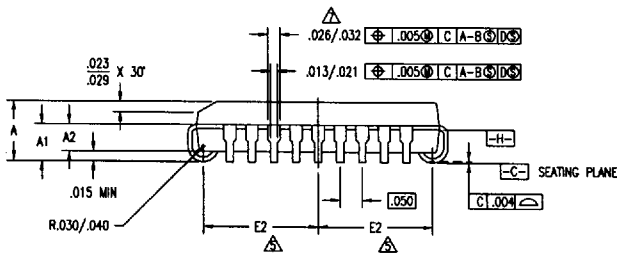
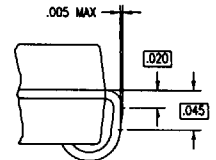
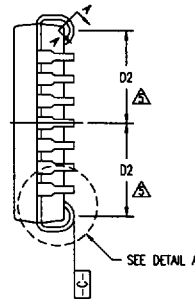
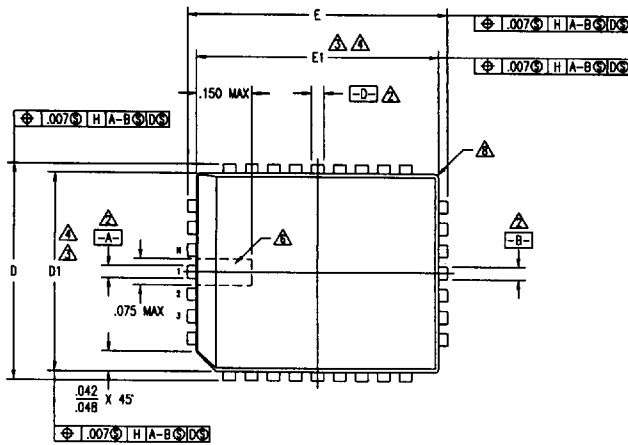
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.

20-32 LEAD LCC (RECTANGULAR)

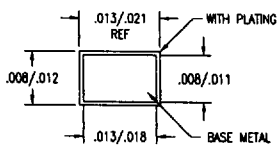
DWG #	L20-1		L22-1		L24-1		L28-2		L32-1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072	REF	.072	REF	.072	REF	.072	REF	.072	REF
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150	BSC	.150	BSC	.200	BSC	.200	BSC	.300	BSC
D2	.075	BSC	.075	BSC	.100	BSC	.100	BSC	.150	BSC
D3	-	.280	-	.280	-	.308	-	.358	-	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250	BSC	.300	BSC	.300	BSC	.400	BSC	.400	BSC
E2	.125	BSC	.150	BSC	.150	BSC	.200	BSC	.200	BSC
E3	-	.410	-	.480	-	.408	-	.558	-	.558
e	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC
e1	.015	-	.015	-	.015	-	.015	-	.015	-
h	.040	REF	.012	RADIUS	.025	REF	.040	REF	.040	REF
J	.020	REF	.012	RADIUS	.015	REF	.020	REF	.020	REF
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PACKAGE DIAGRAM OUTLINES
PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27846	07	REDRAW TO JEDEC FORMAT	03/15/95	



DETAIL A



SECTION A-A

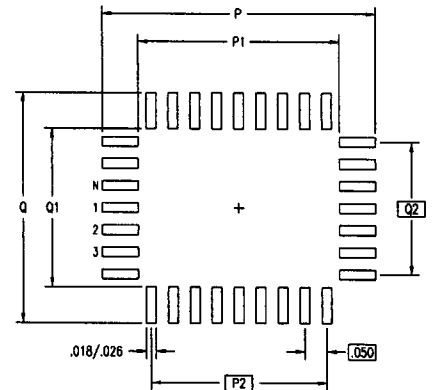
TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, Inc.	
DECIMAL	ANGULAR	2875 Stoner Way, Santa Clara, CA 95054	
±	±	PHONE: (408) 727-8118	
±	±	FAX: (408) 482-8674	
±	±	TWR: 910-338-2070	
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE	
DRAWN	03/15/90	RECTANGULAR PLCC	
CHECKED		.050 PITCH	
SIZE		DRAWING No.	REV
C		PSC-4013	07
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES
PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27846	07	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	JEDEC VARIATION			NOTE
	AE			
	MIN	NOM	MAX	
A	.125	.132	.140	
A1	.075	.078	.095	
A2	.053	-	.068	
D	.485	.490	.495	
D1	.449	.451	.453	3,4
D2	.195	.205	.215	5
E	.585	.590	.595	
E1	.549	.551	.553	3,4
E2	.245	.255	.265	5
ND	7			
NE	9			
N	32			

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.620	.628
P1	.454	.462
P2	.400 BSC	
Q	.520	.562
Q1	.354	.362
Q2	.300 BSC	
N	32	

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-016, VARIATION AE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XXX±	±	PHONE: (408) 727-8118	
XXXX±		FAX: (408) 492-8674 TWC: 910-338-2070	
XXXX±			
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE	
DRAWN <i>Ad</i>	08/15/90	RECTANGULAR PLCC	
CHECKED		.050 PITCH	
		SIZE C	DRAWING No. PSC-4013
			REV 07
DO NOT SCALE DRAWING			

4825771 0021956 945

87