

### Features

512Kx8 bit CMOS Static

Random Access Memory

- Access Times: 17\*, 20, 25, 35, and 45ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

32 lead JEDEC Approved Evolutionary Pinout

- Ceramic Sidebrazed 600 mil DIP, No. 9
- Ceramic 32 Pin Flatpack No. 344
- Ceramic Sidebrazed 400 mil Dip, NO. 326
- Ceramic SOJ, No. 140
- Ceramic Thinpack™ Flatpack, No. 321

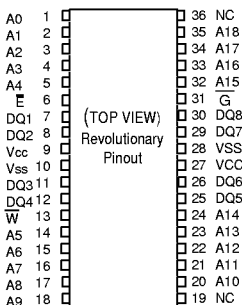
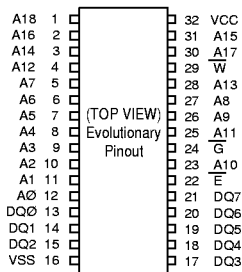
36 lead, JEDEC Approved Revolutionary Pinout

- Ceramic Flatpack, No. 316
- Ceramic SOJ, No. 327

Single +5V (±10%) Supply Operation

\* Commercial and Industrial Temp Range Only

### Pin Configurations and Block Diagram



### 512Kx8 Static RAM CMOS, Monolithic

The ED188512CA is a 4 megabit Monolithic CMOS Static RAM.

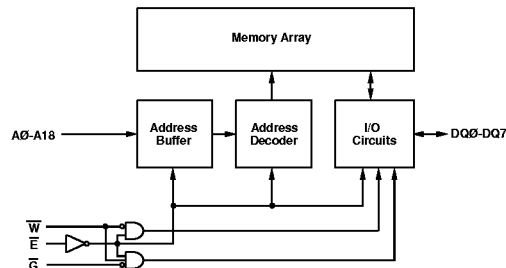
The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device and is a replacement for the 512K x 8 module, ED18M8512C. All 32 pin packages are pin for pin upgrades for the single chip enable 128K x 8, the ED188128CS. Pins 1 and 30 become the higher order addresses.

The 36 pin revolutionary pinout also adheres to the JEDEC standard for the four megabit device. The center pin power and ground pins help to reduce noise in high performance systems. The 36 pin pinout also allows the user an upgrade path to the future 2Mx8.

A Low Power version with Data Retention (ED188512LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

### Pin Names

A0-A18	Address Inputs
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



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### Absolute Maximum Ratings\*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature, Ceramic	-65°C to +150°C
Power Dissipation	1.5 Watt
Output Current	20 mA
Junction Temperature, TJ	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

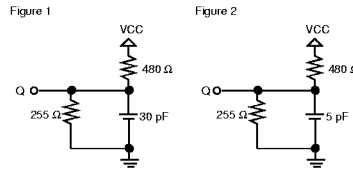
### Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	V+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

### AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	See Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)



### DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA$	17ns	--	250	mA
Supply Current		Min Cycle	20-45ns	--	225	mA
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH, VIN \leq VIL$	--	--	60	mA
Supply Current		$VIN \geq VIH$				
Full Standby Power	ICC3	$\bar{E} \geq VCC-0.2V$	CA	--	25	mA
Supply Current		$VIN \geq VCC-0.2V$ or $VIN \leq 0.2V$	LPA	--	10	mA
Input Leakage Current	ILI	$VIN = 0V$ to VCC	-10	--	10	$\mu A$
Output Leakage Current	ILO	$VIO = 0V$ to VCC	-10	--	10	$\mu A$
Output High Voltage	VOH	$I/OH = -4mA$	2.4	--	--	V
Output Low Voltage	VOL	$I/OH = 8mA$	--	--	0.4	V

\*Typical: TA=25°C, VCC=5.0V

### Truth Table

$\bar{G}$	$\bar{E}$	$\bar{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DO/OUT	ICC1
X	L	L	Write	DIN	ICC1

### Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	12	pF
Data Lines	CD/Q	14	pF

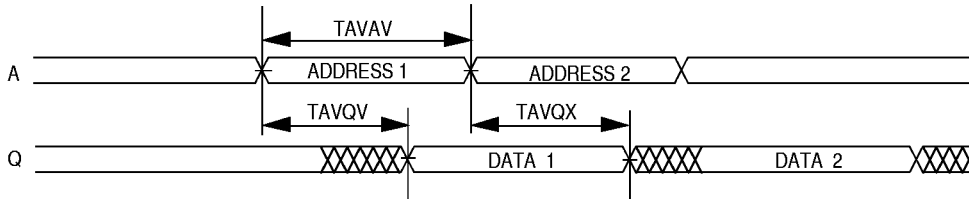
These parameters are sampled, not 100% tested.

**AC Characteristics Read Cycle**

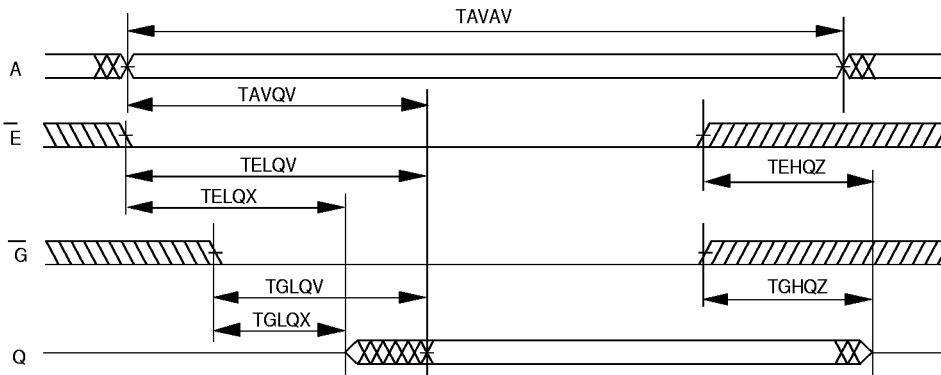
Parameter	Symbol		17ns*		20ns		25ns		35ns		45ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	17		20		25		35		45		ns
Address Access Time	TAVQV	TAA		17		20		25		35		45	ns
Chip Enable Access Time	TELQV	TACS		17		20		25		35		45	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	7	0	8	0	10	0	15	0	20	ns
Output Hold from Address Change	TAVQX	TOH	4		5		5		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		8		10		12		15		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ	0	7	0	8	0	10	0	15	0	20	ns

\*Commercial, Industrial Temp Range  
Note 1: Parameter guaranteed, but not tested.

**Read Cycle 1 -  $\bar{W}$  High,  $\bar{G}$ ,  $\bar{E}$  Low**



**Read Cycle 2 -  $\bar{W}$  High**

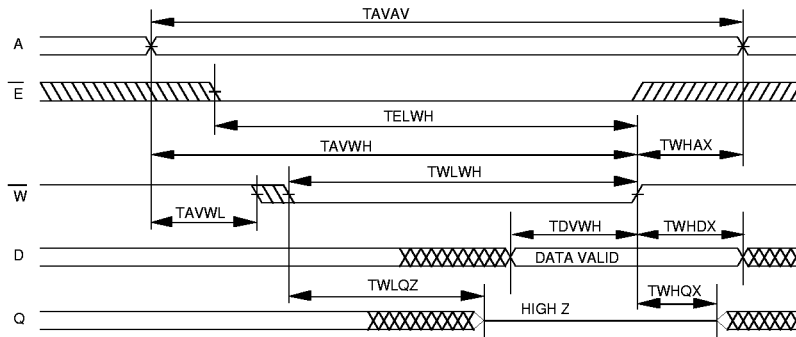


### AC Characteristics Write Cycle

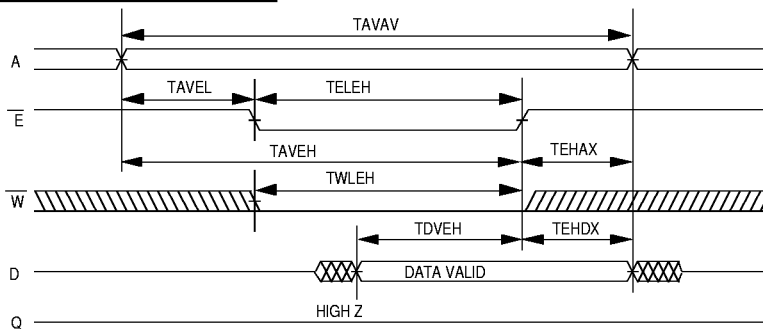
Parameter	Symbol		17ns*		20ns		25ns		35ns		45ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	17		20		25		35		45		ns
Chip Enable to End of Write	TELWH	TCW	14		15		17		25		30		ns
	TELEH	TCW	14		15		17		25		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	14		15		17		25		30		ns
	TAVEH	TAW	14		15		17		25		30		ns
Write Pulse Width	TWLWH	TWP	14		15		17		25		30		ns
	TWLEH	TWP	14		15		17		25		30		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time (1)	TWHDX	TDH	0		0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	8	0	10	0	25	0	30	ns
Data to Write Time	TDVWH	TDW	8		10		12		20		25		ns
	TDVEH	TDW	8		10		12		20		25		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		0		0		ns

\*Commercial, Industrial Temp Range Only  
 Note 1: Parameter guaranteed, but not tested.

### Write Cycle 1 - $\bar{W}$ Controlled



### Write Cycle 2 - $\bar{E}$ Controlled



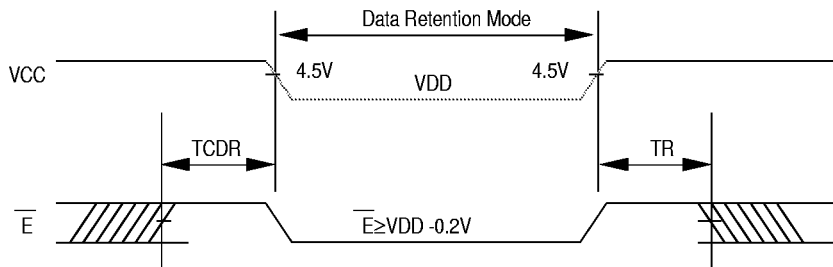
**Data Retention Characteristics**

ED188512LPA Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	$\bar{E} \geq VDD - 0.2V$ $V_{IN} \geq VDD - 0.2V$ or $V_{IN} \leq 0.2V$		2	-	-	V
Data Retention Quiescent Current	ICCDR		2V	-	-	2	mA
Chip Disable to Data Retention Time	TCDR			0	-	-	ns
Operation Recovery Time	TR			TAVAV	-	-	ns

\*Read Cycle Time

**Data Retention  $\bar{E}$  Controlled**





### Ordering Information

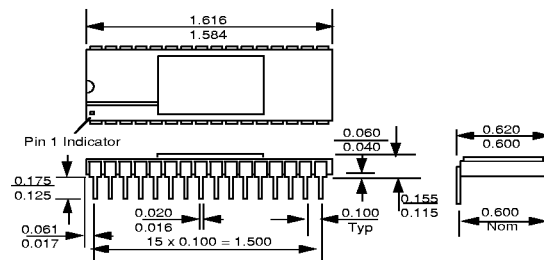
Part No.	Speed (ns)	Package No.
ED188512CA17CI	17	9
ED188512CA20CB	20	9
ED188512CA25CB	25	9
ED188512CA35CB	35	9
ED188512CA45CB	45	9
ED188512CA17TI	17	326
ED188512CA20TB	20	326
ED188512CA25TB	25	326
ED188512CA35TB	35	326
ED188512CA45TB	45	326
ED188512CA17NI	17	140
ED188512CA20NB	20	140
ED188512CA25NB	25	140
ED188512CA35NB	35	140
ED188512CA45NB	45	140
ED188512CA17B32I	17	321
ED188512CA20B32B	20	321
ED188512CA25B32B	25	321
ED188512CA35B32B	35	321
ED188512CA45B32B	45	321
ED188512CA17F32I	17	344
ED188512CA20F32B	20	344
ED188512CA25F32B	25	344
ED188512CA35F32B	35	344
ED188512CA45F32B	45	344
ED188512CA17F36I	17	316
ED188512CA20F36B	20	316
ED188512CA25F36B	25	316
ED188512CA35F36B	35	316
ED188512CA45F36B	45	316
ED188512CA17N36I	17	327
ED188512CA20N36B	20	327
ED188512CA25N36B	25	327
ED188512CA35N36B	35	327
ED188512CA45N36B	45	327

Part No.	Speed (ns)	Package No.
ED188512LPA17CI	17	9
ED188512LPA20CB	20	9
ED188512LPA25CB	25	9
ED188512LPA35CB	35	9
ED188512LPA45CB	45	9
ED188512LPA17TI	17	326
ED188512LPA20TB	20	326
ED188512LPA25TB	25	326
ED188512LPA35TB	35	326
ED188512LPA45TB	45	326
ED188512LPA17NI	17	140
ED188512LPA20NB	20	140
ED188512LPA25NB	25	140
ED188512LPA35NB	35	140
ED188512LPA45NB	45	140
ED188512LPA17B32I	17	321
ED188512LPA20B32B	20	321
ED188512LPA25B32B	25	321
ED188512LPA35B32B	35	321
ED188512LPA45B32B	45	321
ED188512LPA17F32I	17	344
ED188512LPA20F32B	20	344
ED188512LPA25F32B	25	344
ED188512LPA35F32B	35	344
ED188512LPA45F32B	45	344
ED188512LPA17F36I	17	316
ED188512LPA20F36B	20	316
ED188512LPA25F36B	25	316
ED188512LPA35F36B	35	316
ED188512LPA45F36B	45	316
ED188512LPA17N36I	17	327
ED188512LPA20N36B	20	327
ED188512LPA25N36B	25	327
ED188512LPA35N36B	35	327
ED188512LPA45N36B	45	327

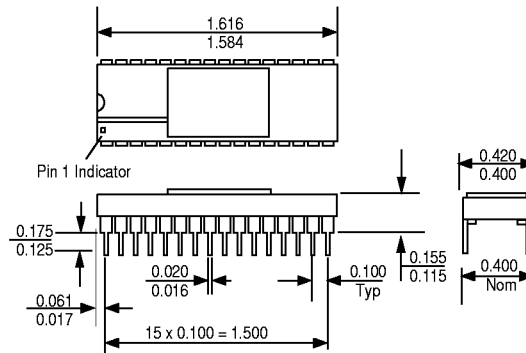
For Commercial, Industrial or Military grade product use C, I or M respectively, to replace B in the suffix of the part number, e.g. ED188512CA20CB becomes ED188512CA20CC (Commercial temp. range), ED188512CA20CI (Industrial temp. range), or ED188512CA20CM (Military temp range).

**Package Description**

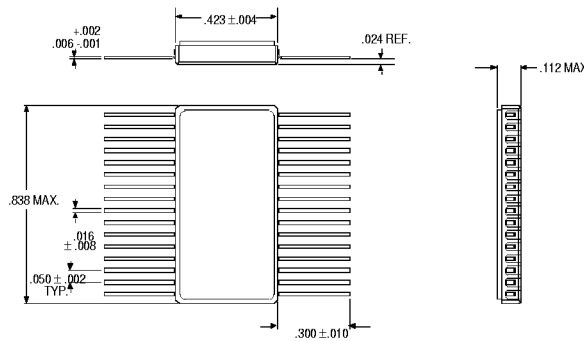
**Package No. 9**  
32 Pin Sidebrazed Ceramic  
Dual-in-line Package  
Weight = 5.80g  
Theta  $J_A$  = 20°C/W  
Theta  $J_C$  = 6.5°C/W



**Package No. 326**  
32 Pin Sidebrazed Ceramic  
Dual-in line Package  
Weight = 3.85g  
Theta  $J_A$  = 22.0°C/W  
Theta  $J_C$  = 7.0°C/W

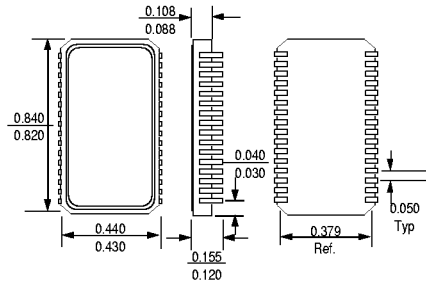


**Package No. 344**  
32 Pin Flatpack  
Weight = 2.00g  
Theta  $J_A$  = 38.0°C/W  
Theta  $J_C$  = 15°C/W

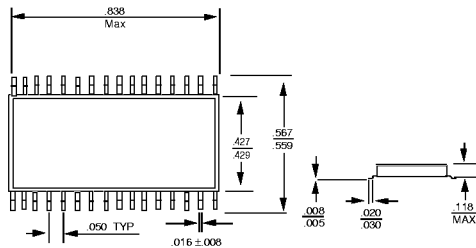




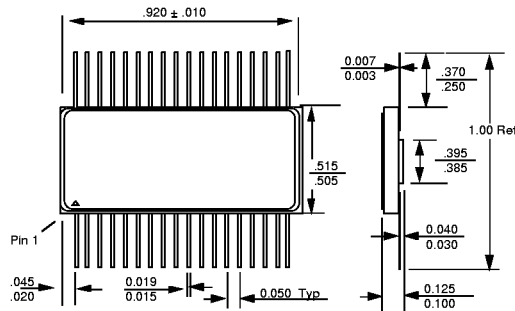
**Package No. 140**  
**32 Pin Ceramic**  
**SOJ Package**  
 Weight = 1.90g  
 Theta  $J_A$  = 40°C/W  
 Theta  $J_C$  = 8°C/W



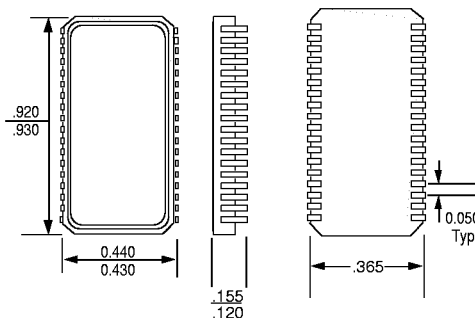
**Package No. 321**  
**32 Pin Ceramic**  
**Thinpack™ Flatpack**  
 Weight = 1.90g  
 Theta  $J_A$  = 38°C/W  
 Theta  $J_C$  = 15°C/W



**Package No. 316**  
**36 Pin Ceramic**  
**Flatpack**  
 Weight = 3.02g  
 Theta  $J_A$  = 20°C/W  
 Theta  $J_C$  = 2°C/W



**Package No. 327**  
**36 Pin Ceramic SOJ**  
 Weight = 1.95g  
 Theta  $J_A$  = 40°C/W  
 Theta  $J_C$  = 8°C/W



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