

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

74ALS651/651-1 Octal transceiver/register, inverting (3-State)
74ALS652/652-1 Octal transceiver/register, non-inverting (3-State)

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- 3-State outputs
- The -1 versions sinks 48mA I_{OL} within the $\pm 5\%$ V_{CC} range

DESCRIPTION

The 74ALS651 and 74ALS652 transceivers/registers consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output enable (\overline{OEAB} , \overline{OEBA}) and select (SAB, SBA) pins are provided for bus management. The 74ALS651-1 and 74ALS652-1 will sink 48mA if the V_{CC} is limited to $5.0V \pm 0.25V$.

| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|---------------------|-------------------|--------------------------------|
| 74ALS651/74ALS651-1 | 140MHz | 40mA |
| 74ALS652/74ALS652-1 | 140MHz | 46mA |

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | DRAWING NUMBER |
|--------------------|------------------------------------------------------------------------------------------|----------------|
| | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | |
| 24-pin plastic DIP | 74ALS651N, 74ALS651-1N, 74ALS652N, 74ALS652-1N | SOT222-1 |
| 24-pin plastic SOL | 74ALS651D, 74ALS651-1D, 74ALS652D, 74ALS652-1D | SOT137-1 |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

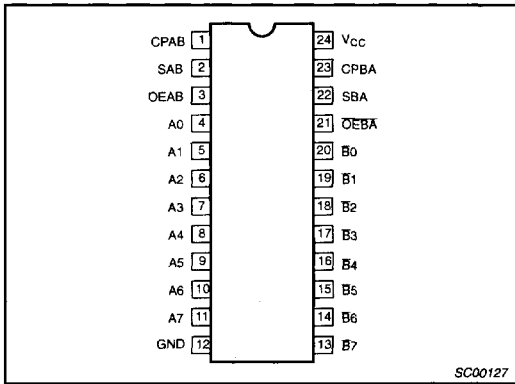
| PINS | DESCRIPTION | 74ALS (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-------------------|----------------------------|-----------------------|---------------------|
| A0 – A7 | A inputs | 1.0/1.0 | 70 μ A/0.1mA |
| B0 – B7 | B inputs | 1.0/1.0 | 70 μ A/0.1mA |
| CPAB | A-to-B clock input | 1.0/1.0 | 20 μ A/0.1mA |
| CPBA | B-to-A clock input | 1.0/1.0 | 20 μ A/0.1mA |
| SAB | A-to-B select input | 1.0/1.0 | 20 μ A/0.1mA |
| SBA | B-to-A select input | 1.0/1.0 | 20 μ A/0.1mA |
| \overline{OEAB} | A-to-B output enable input | 1.0/1.0 | 20 μ A/0.1mA |
| \overline{OEBA} | B-to-A output enable input | 1.0/1.0 | 20 μ A/0.1mA |
| A0 – A7, B0 – B7 | A, B outputs | 750/240 | 15mA/24mA |
| A0 – A7, B0 – B7 | A, B outputs (-1 version) | 750/480 | 15mA/48mA |

NOTE: One (1.0) ALS unit load is defined as: 20 μ A in the High state and 0.1mA in the Low state.

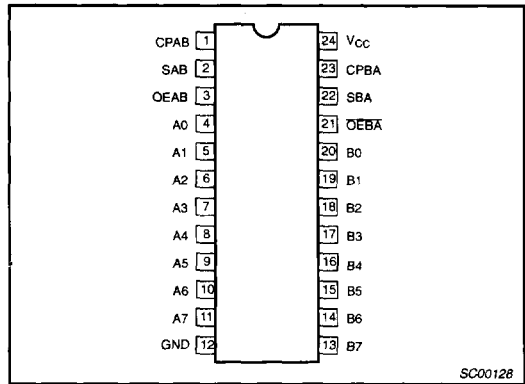
Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

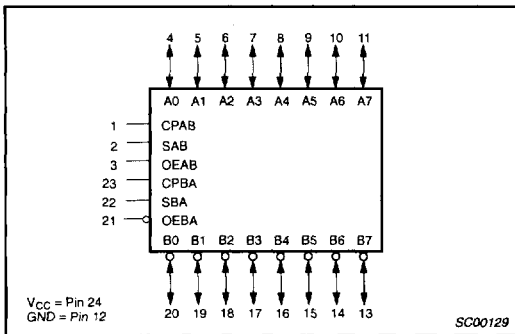
PIN CONFIGURATION – 74ALS651/651-1



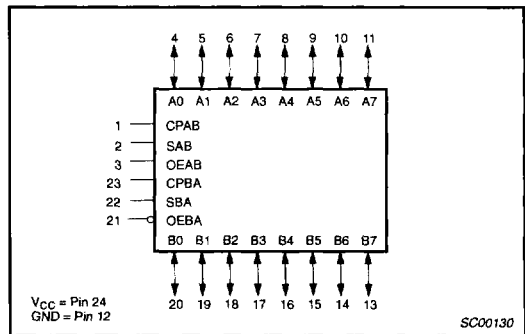
PIN CONFIGURATION – 74ALS652/652-1



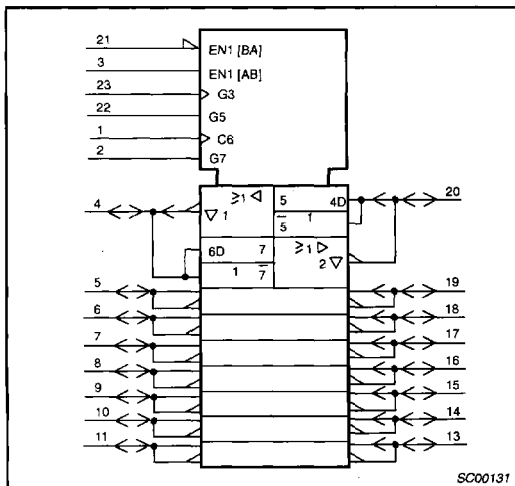
LOGIC SYMBOL – 74ALS651/651-1



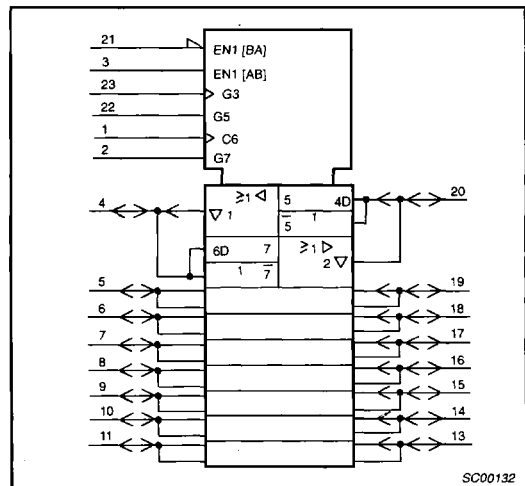
LOGIC SYMBOL – 74ALS652/652-1



IEC/IEEE SYMBOL – 74ALS651/651-1



IEC/IEEE SYMBOL – 74ALS652/652-1

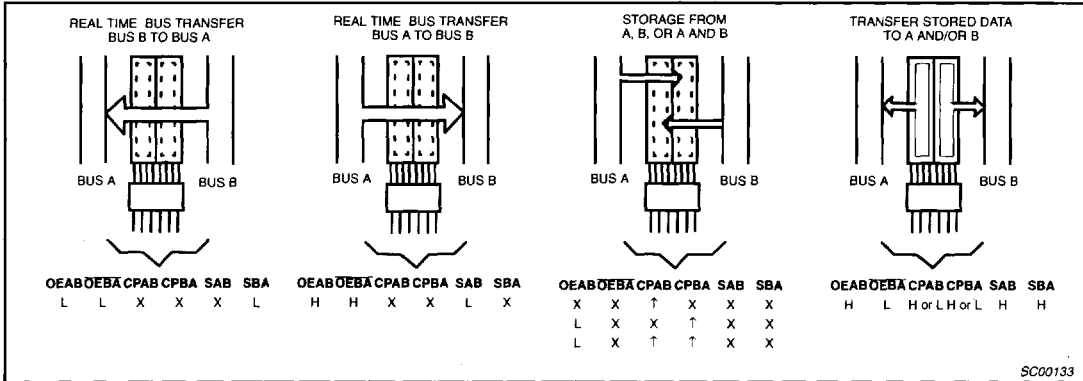


Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

BUS MANAGEMENT FUNCTIONS

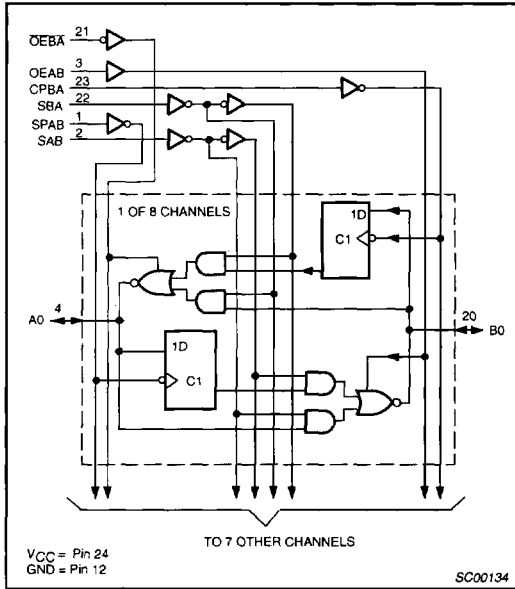
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALS651/74ALS651-1 and 74ALS652/74ALS652-1. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.



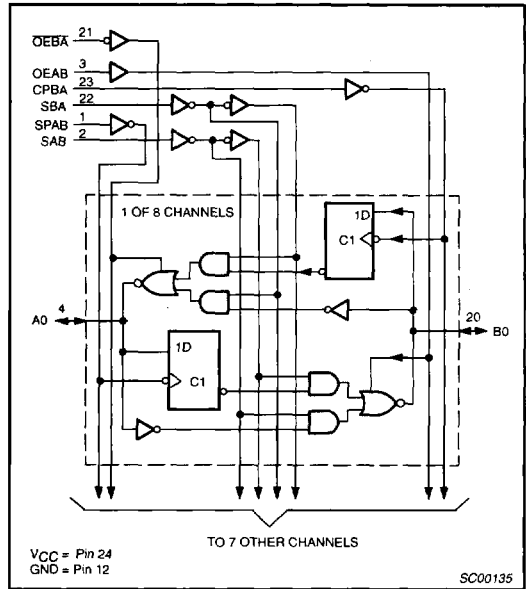
Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

LOGIC DIAGRAM – 74ALS651/651-1



LOGIC DIAGRAM – 74ALS652/652-1



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATING MODE | |
|--------|------|--------|--------|-----|-----|----------------|----------------|----------------------------|----------------------------|
| OEAB | OEBA | CPAB | CPBA | SAB | SBA | A _n | B _n | 74ALS651/74ALS651-1 | 74ALS652/74ALS652-1 |
| L | H | H or L | H or L | X | X | Input | Input | Isolation | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified* | Store A, hold B | Store A, hold B |
| H | H | ↑ | ↑ | L | X | Input | Output | Store A in both registers | Store A in both registers |
| L | X | H or L | ↑ | X | S | Unspecified* | Input | Hold A, store B | Hold A, store B |
| L | L | ↑ | ↑ | X | L | Output | Input | Store B in both registers | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real time B̄ data to A bus | Real time B̄ data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B̄ data to A bus | Stored B̄ data to A bus |
| H | H | X | X | L | X | Input | Output | Real time Ā data to B bus | Real time A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Stored Ā data to B bus | Stored A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored Ā data to B bus | Stored A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored B̄ data to A bus | Stored B data to A bus |

NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

* = The data output function may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ = Low-to-High clock transition

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | | RATING | UNIT |
|-----------|------------------------------------------------|--------------|------------------|------|
| V_{CC} | Supply voltage | | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | | -0.5 to +7.0 | V |
| i_{IN} | Input current | | -30 to +5 | mA |
| V_{OUT} | Voltage applied to output in High output state | | -0.5 to V_{CC} | V |
| I_{OUT} | Current applied to output in Low output state | All versions | 48 | mA |
| | | -1 version | 96 | mA |
| T_{amb} | Operating free-air temperature range | | 0 to +70 | °C |
| T_{stg} | Storage temperature range | | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|--------------|-----|-----------------|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| i_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -15 | mA |
| I_{OL} | Low-level output current | All versions | | 24 | mA |
| | | -1 version | | 48 ¹ | mA |
| T_{amb} | Operating free-air temperature range | 0 | | +70 | °C |

NOTE:

- The 48mA limit applies only under the condition of $V_{CC} = 5.0V \pm 5\%$.

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS ¹ | | LIMITS | | | UNIT |
|-----------------|----------------------------------------|-------------------------|--------------------------------------------------------------------------|--------------------------|---------------------|------------------|------|------|
| | | | | | MIN | TYP ² | MAX | |
| V _{OH} | High-level output voltage | | V _{CC} ± 10%, V _{IL} = MAX, V _{IH} = MIN | I _{OH} = -0.4mA | V _{CC} - 2 | | | V |
| | | | | I _{OH} = -3mA | 2.4 | 3.2 | | V |
| | | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OH} = -15mA | 2.0 | | | V |
| V _{OL} | Low-level output voltage | All versions | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = 12mA | | 0.25 | 0.40 | V |
| | | | | I _{OL} = 24mA | | 0.35 | 0.50 | V |
| | | -1 versions | V _{CC} = 4.75V, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = 48mA | | 0.35 | 0.50 | V |
| V _{IK} | Input clamp voltage | | V _{CC} = MIN, I _I = I _{IK} | | | -0.73 | -1.5 | V |
| I _I | Input current at maximum input voltage | control inputs | V _{CC} = MAX, V _I = 7.0V | | | | 0.1 | mA |
| | | A or B ports | V _{CC} = MAX, V _I = 5.5V | | | | 0.1 | mA |
| I _{IH} | High-level input current ³ | | V _{CC} = MAX, V _I = 2.7V | | | | 20 | μA |
| I _{IL} | Low-level input current ³ | | V _{CC} = MAX, V _I = 0.4V | | | | -0.1 | mA |
| I _O | Output current ⁴ | | V _{CC} = MAX, V _O = 2.25V | | -30 | | -112 | mA |
| I _{CC} | Supply current (total) | 74ALS651/ 74ALS651-1 | I _{CCH} | V _{CC} = MAX | | 32 | 50 | mA |
| | | | I _{CCL} | | | 45 | 68 | mA |
| | | | I _{CCZ} | | | 44 | 68 | mA |
| | | 74ALS652/ 74ALS652-1 | I _{CCH} | V _{CC} = MAX | | 36 | 58 | mA |
| | | | I _{CCL} | | | 53 | 78 | mA |
| | | | I _{CCZ} | | | 49 | 72 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS FOR 74ALS651/74ALS651-1

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|--------------------------------------|-----------------------------------------------------------|--------------------------|------------------------------------------------------------------------------------------------------------------|--------------|------|
| | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | MIN | MAX | |
| f _{max} | Maximum clock frequency | Waveform 1 | 100 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CPBA to An, CPAB to Bn | Waveform 1 | 5.0 6.0 | 13.0 13.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay An to Bn or Bn to An | Waveform 2, 3 | 1.0 2.0 | 7.0 9.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay SBA to An or SAB to Bn (A or B Low) | Waveform 2, 3 | 6.0 5.0 | 14.0 11.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay SBA to An or SAB to Bn (A or B High) | Waveform 2, 3 | 4.0 5.0 | 11.0 12.0 | ns |
| t _{PZH} t _{PZL} | Output enable time OEBA to An | Waveform 7 Waveform 8 | 2.0 5.0 | 8.0 12.0 | ns |
| t _{PHZ} t _{PLZ} | Output disable time OEBA to An | Waveform 7 Waveform 8 | 2.0 3.0 | 8.0 10.0 | ns |
| t _{PZH} t _{PZL} | Output enable time OEAB to Bn | Waveform 7 Waveform 8 | 2.0 5.0 | 9.0 12.0 | ns |
| t _{PHZ} t _{PLZ} | Output disable time OEAB to Bn | Waveform 7 Waveform 8 | 3.0 5.0 | 11.0 13.0 | ns |

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

AC ELECTRICAL CHARACTERISTICS FOR 74ALS652/74ALS652-1

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|------------------------|-----------------------------------------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------|--------------|------|
| | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | MIN | MAX | |
| f_{max} | Maximum clock frequency | Waveform 1 | 100 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CPBA to An, CPAB to Bn | Waveform 1 | 5.0 6.0 | 13.0 13.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | Waveform 2, 3 | 2.0 4.0 | 8.0 9.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay SBA to An or SAB to Bn (A or B Low) | Waveform 2, 3 | 4.0 5.0 | 11.0 11.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay SBA to An or SAB to Bn (A or B High) | Waveform 2, 3 | 6.0 5.0 | 14.0 11.0 | ns |
| t_{pZH} t_{pZL} | Output enable time OEBA to An | Waveform 7 Waveform 8 | 2.0 5.0 | 8.0 11.0 | ns |
| t_{pHZ} t_{pLZ} | Output disable time OEBA to An | Waveform 7 Waveform 8 | 2.0 3.0 | 8.0 10.0 | ns |
| t_{pZH} t_{pZL} | Output enable time OEAB to Bn | Waveform 7 Waveform 8 | 2.0 5.0 | 9.0 11.0 | ns |
| t_{pHZ} t_{pLZ} | Output disable time OEAB to Bn | Waveform 7 Waveform 8 | 3.0 5.0 | 11.0 13.0 | ns |

AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|----------------------------|----------------------------------------------------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------|-----|------|
| | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | MIN | MAX | |
| $t_{su}(H)$ $t_{su}(L)$ | Setup time, High or Low An or Bn to CPAB or CPBA | Waveform 4 | 5.0 5.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, High or Low An or Bn to CPAB or CPBA | Waveform 4 | 0.0 1.0 | | ns |
| $t_{su}(H)$ $t_{su}(L)$ | Setup time, High or Low ¹ OEBA to OEAB or OEAB to OEBA | Waveform 5, 6 | 5.0 5.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, High or Low OEBA to OEAB or OEAB to OEBA | Waveform 5, 6 | 0.0 0.0 | | ns |
| $t_w(H)$ $t_w(L)$ | Pulse width, High or Low CPAB or CPBA | Waveform 1 | 6.0 4.0 | | ns |

NOTE:

1. Setup time is to protect against current surge caused by enabling 16 outputs (24mA per output) simultaneously.

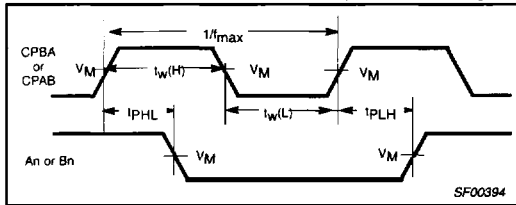
Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

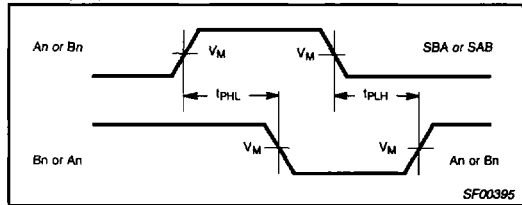
AC WAVEFORMS

For all waveforms, $V_M = 1.3V$.

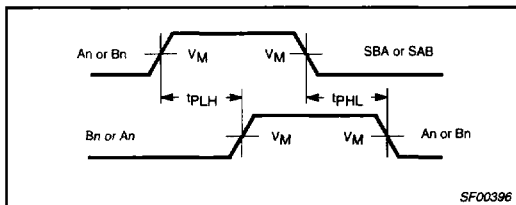
The shaded areas indicate when the input is permitted to change for predictable output performance.



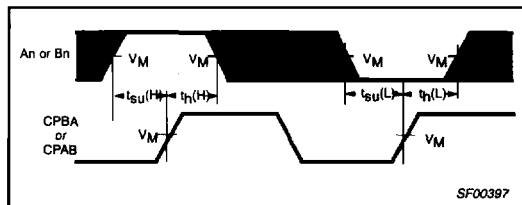
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



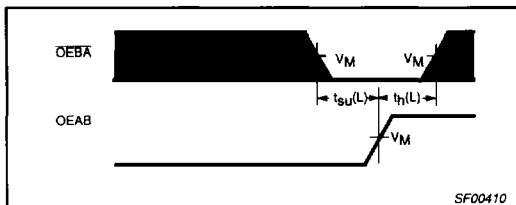
Waveform 2. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



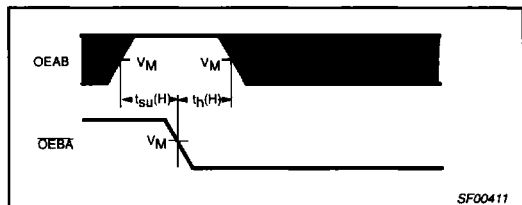
Waveform 3. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



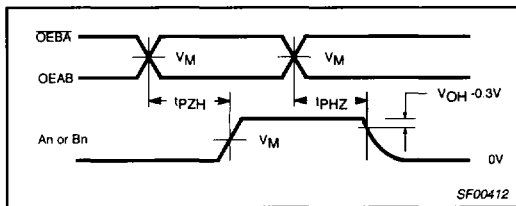
Waveform 4. Data Setup Time and Hold Times



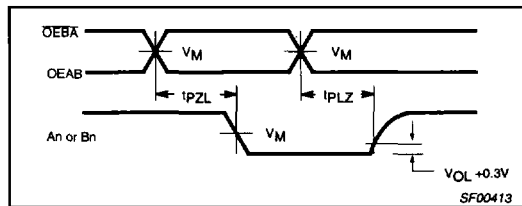
Waveform 5. OEBA to OEAB Setup Time and Hold Times



Waveform 6. OEAB to OEBA Setup Time and Hold Times



Waveform 7. 3-State Output Enable Time to High Level and Output Disable Time from High Level

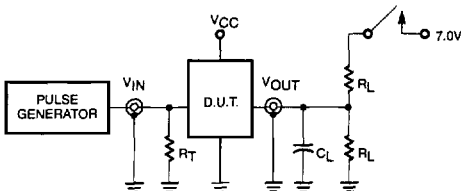


Waveform 8. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

TEST CIRCUIT AND WAVEFORMS



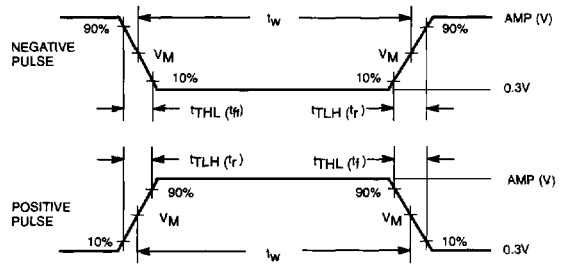
Test Circuit for 3-State and Open Collector Outputs

SWITCH POSITION

| TEST | SWITCH |
|-----------------------|--------|
| t_{PLZ} , t_{PZL} | closed |
| open collector | closed |
| All other | open |

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

| Family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|----------|-------|-----------|-----------|
| | Amplitude | V_M | Rep.Rate | t_w | t_{TLH} | t_{THL} |
| 74ALS | 3.5V | 1.3V | 1MHz | 500ns | 2.0ns | 2.0ns |

SC00126