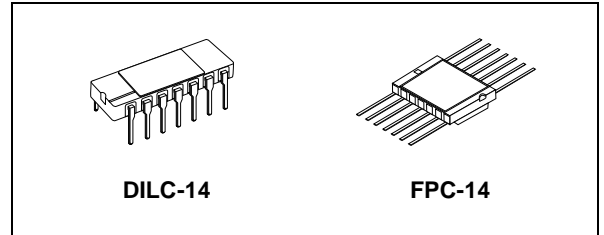


RAD HARD DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
 $f_{MAX} = 80\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 73
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9203-071

DESCRIPTION

The M54HC73 is an high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated with silicon gate C²MOS technology.



ORDER CODES

PACKAGE	FM	EM
DILC	M54HC73D	M54HC73D1
FPC	M54HC73K	M54HC73K1

Depending on the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse (\overline{CK}). The clear function is accomplished independently of the clock condition when the clear input (\overline{CLR}) is taken low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

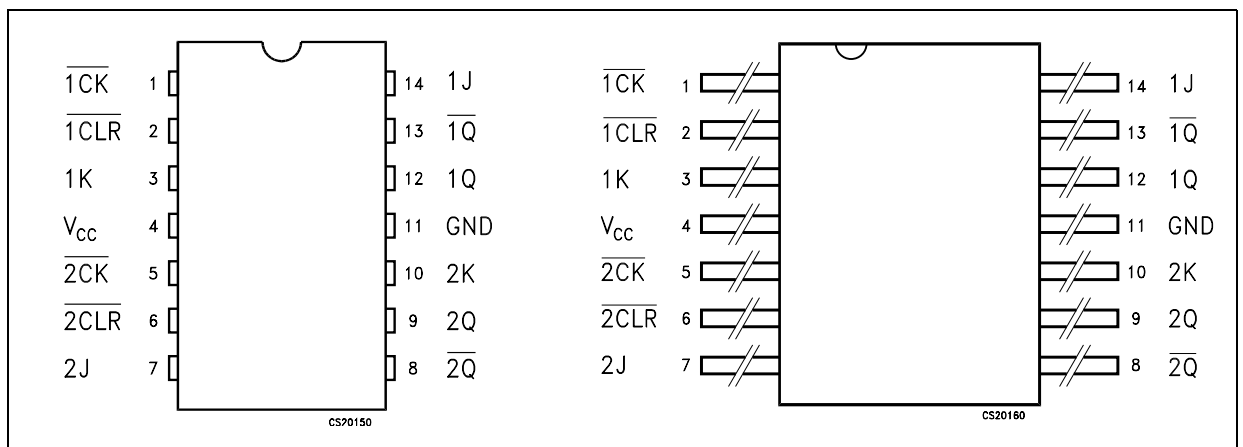


Figure 1: IEC Logic Symbols

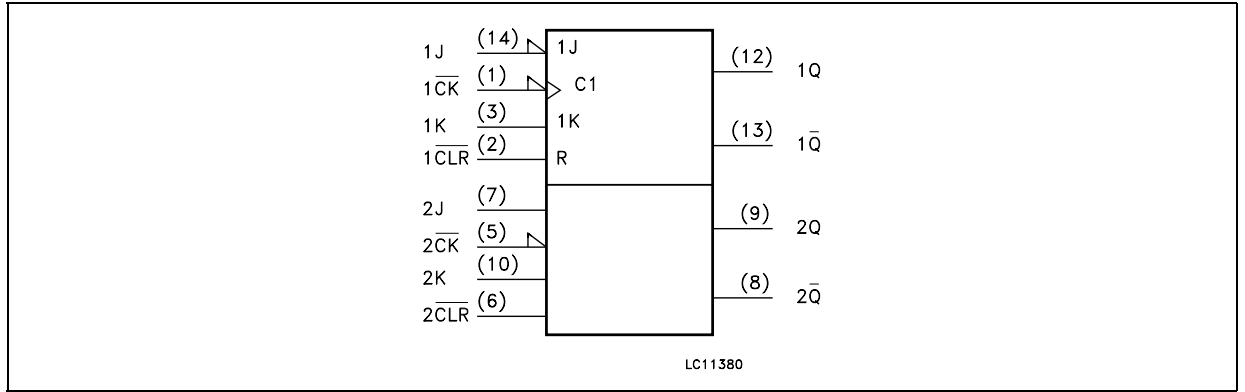


Figure 2: Input And Output Equivalent Circuit

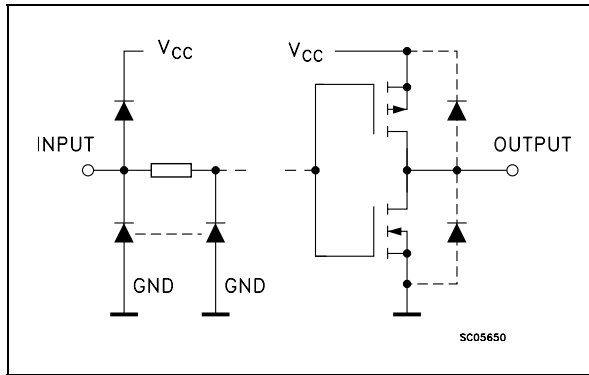


Table 1: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 5	1CK, 2CK	Clock Input
2, 6	1CLR, 2CLR	Asynchronous Reset Inputs
12, 9	1Q, 2Q	True Flip-Flop Outputs
13, 8	1Q-bar, 2Q-bar	Complement Flip-Flop Outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	Synchronous Inputs Flip-Flop 1 and 2
11	GND	Ground (0V)
4	V _{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS				OUTPUTS		FUNCTION
CLR	J	K	CK	Q	Q-bar	
L	X	X	X	L	H	CLEAR
H	L	L	⌋	Q _n	Q _n -bar	NO CHANGE
H	L	H	⌋	L	H	----
H	H	L	⌋	H	L	----
H	H	H	⌋	Q _n -bar	Q _n	TOGGLE
H	X	X	⌋	Q _n	Q _n -bar	NO CHANGE

X : Don't Care

Figure 3: Logic Diagram

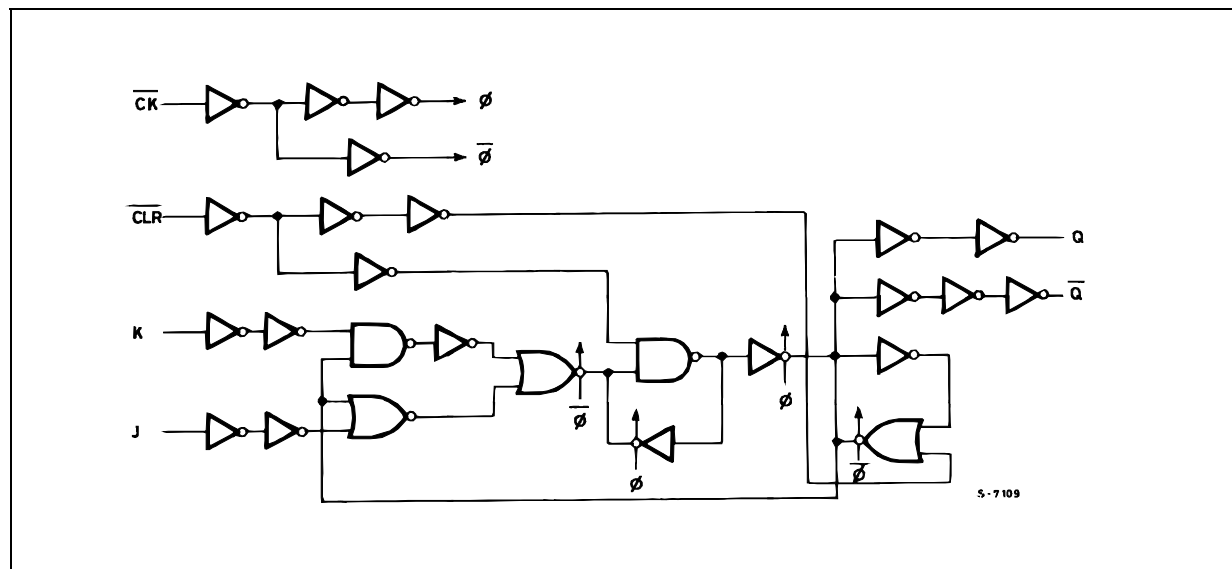


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	265	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Recommended Operating Conditions

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			2		20		40	μA

Table 6: AC Electrical Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

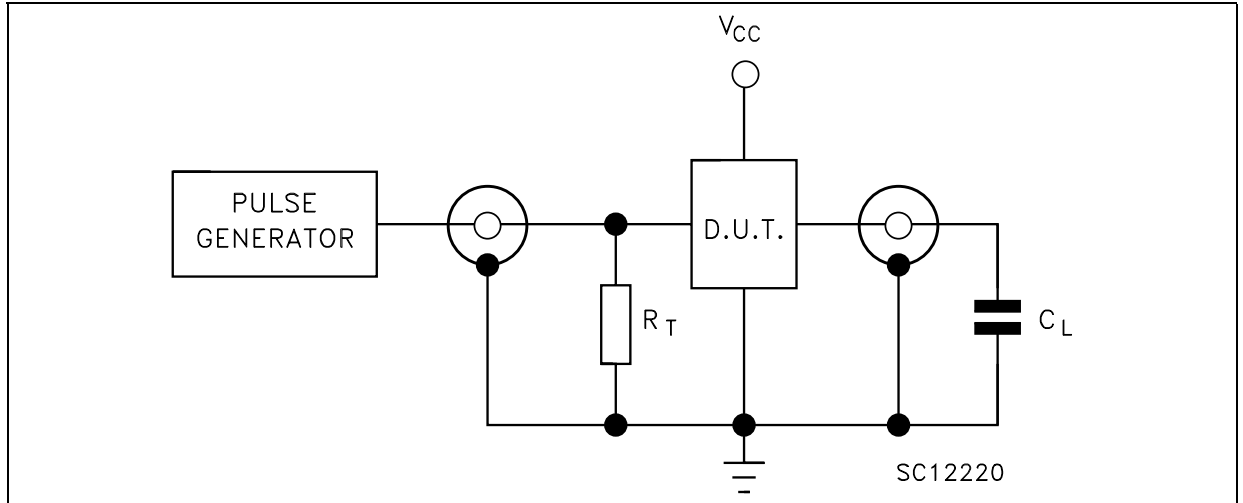
Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	V_{CC} (V)			30	75		95		110	ns
					8	15		19		22	
					7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	V_{CC} (V)			42	125		155		190	ns
					14	25		31		38	
					12	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (CLR - Q)	V_{CC} (V)			54	145		180		220	ns
					18	29		36		44	
					15	25		31		37	
f_{MAX}	Maximum Clock Frequency	V_{CC} (V)		6	15		4.8		4		MHz
				30	60		24		20		
				35	80		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	V_{CC} (V)			18	75		95		110	ns
					6	15		19		22	
					6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLR)	V_{CC} (V)			21	75		95		110	ns
					7	15		19		22	
					6	13		16		19	
t_s	Minimum Set-up Time	V_{CC} (V)			30	75		95		110	ns
					8	15		19		22	
					6	13		16		19	
t_h	Minimum Hold Time	V_{CC} (V)				0		0		0	ns
						0		0		0	
						0		0		0	
t_{REM}	Minimum Removal Time	V_{CC} (V)			25	75		95		110	ns
					7	15		19		22	
					6	13		16		19	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	V_{CC} (V)			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	V_{CC} (V)	5.0		35						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

Figure 4: Test Circuit



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Waveform - Minimum Removal Time ($f=1\text{MHz}$; 50% duty cycle)

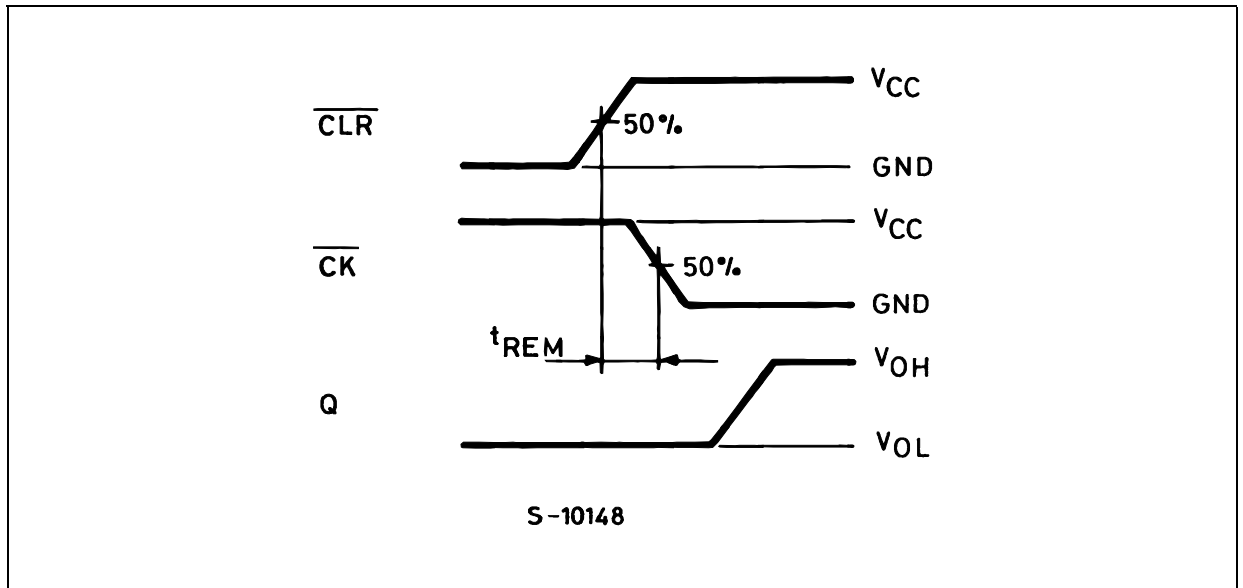


Figure 6: Waveform - Minimum Pulse Width, Propagation Delay Time ($f=1\text{MHz}$; 50% duty cycle)

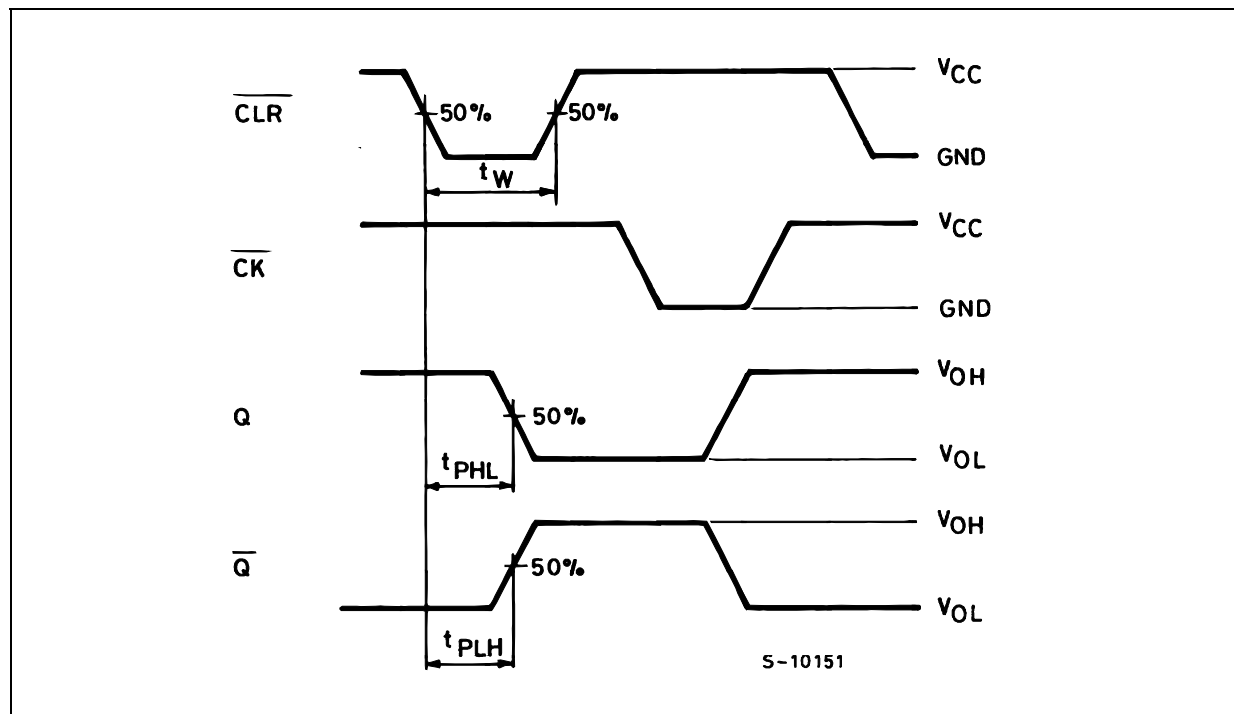
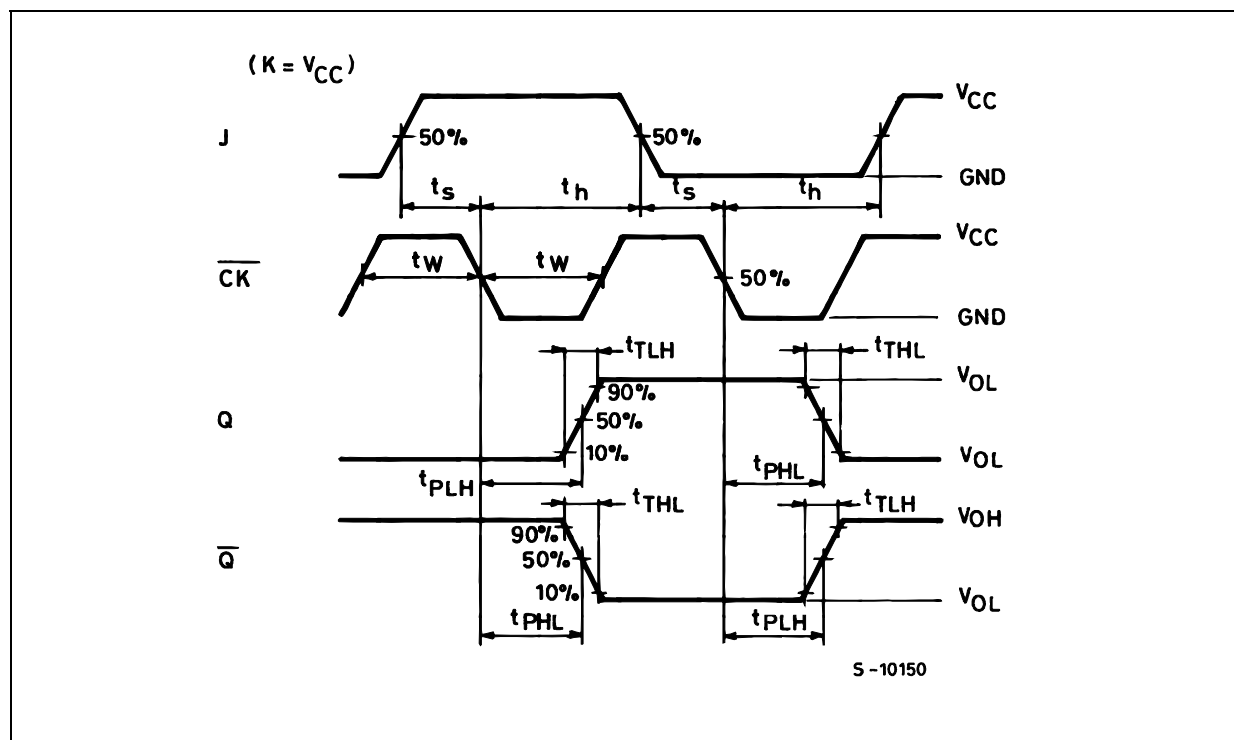
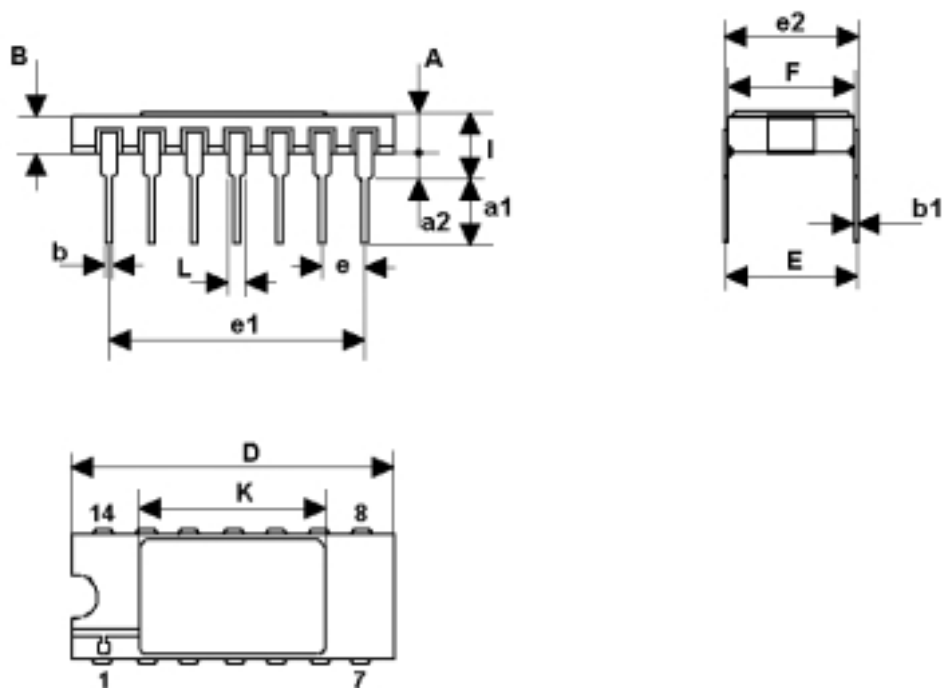


Figure 7: Waveform - Propagation Delay Time, Minimum Pulse Width, Setup And Hold Time ($f=1\text{MHz}$; 50% duty cycle)



DILC-14 MECHANICAL DATA

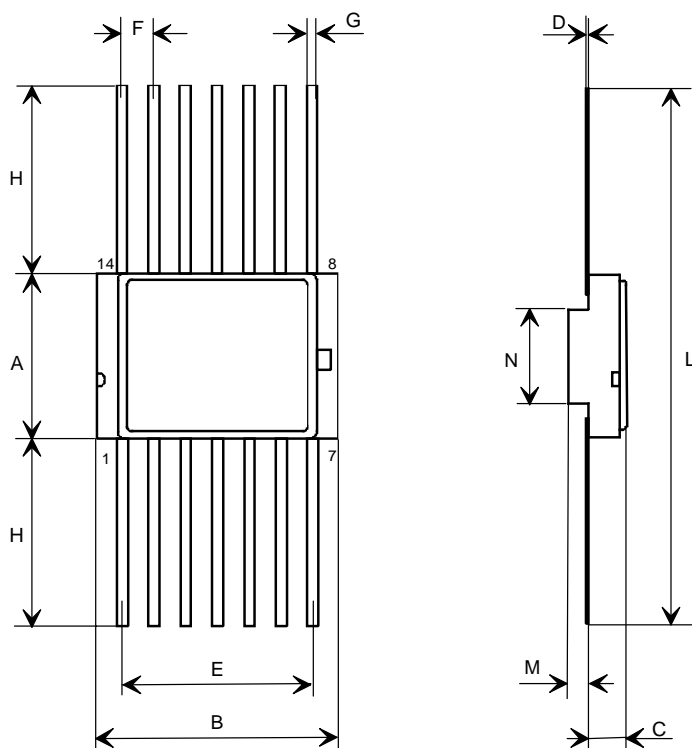
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.54	0.083		0.100
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82	2.03	2.39	0.072	0.080	0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	18.79	19.00	19.20	0.740	0.748	0.756
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	15.11	15.24	15.37	0.595	0.600	0.605
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.11		7.75	0.280		0.305
I			3.70			0.146
K	10.90		12.1	0.429		0.476
L	1.14	1.27	1.5	0.045	0.050	0.059



0016173H

FPC-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.95	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.10	0.127	0.15	0.004	0.005	0.006
E	7.50	7.62	7.75	0.295	0.300	0.305
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H		6.0			0.236	
L	18.75		22.0	0.738		0.866
M		0.38			0.015	
N		4.31			0.170	



016029E

Table 8: Revision History

Date	Revision	Description of Changes
01-Jun-2004	1	First Release

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>