REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical and editorial changes throughout. Add vendor CAGE 04713 for device type 01. Add characterization for device classes B, S, Q, and V. Add ground bounce and latch-up immunity characterization. Add appendix A. - jak	92-12-15	Monica L. Poelking
B	Technical and editorial changes throughout. Add RHA requirements. - CS	97-10-16	Monica L. Poelking
C	Add device type 03. Add vendor CAGE F8859. Add case outlines X and Z. Add radiation features for device type 01. Update boilerplate to MIL-PRF-38535 requirements. - jak	02-07-03	Thomas M. Hess
D	Change lead temperature for case outline X in section 1.3. Add radiation features for device type 03 in section 1.5. Editorial changes throughout. - LTG	05-01-04	Thomas M. Hess
E	Change I_{CCH} and I_{CCL} max limits for device type 03 in table I. - LTG	05-08-23	Thomas M. Hess
F	Add appendix A, microcircuit die. Update the boilerplate to MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. - jak	07-04-02	Thomas M. Hess
G	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-08-27	Thomas M. Hess
H	Update absolute rating maximum supply voltage range in section 1.3 for Vendor cage code F8859 supplying devices.- MAA	17-01-26	Thomas M. Hess
J	Add case outline Y for device type 03. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	19-01-29	Thomas M. Hess

REV																				
SHEET																				
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
88-01-06

REVISION LEVEL
J

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, DUAL D-TYPE FLIP-FLOP WITH PRESET AND CLEAR, TTL COMPATIBLE INPUTS MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87525**

SHEET 1 OF 28

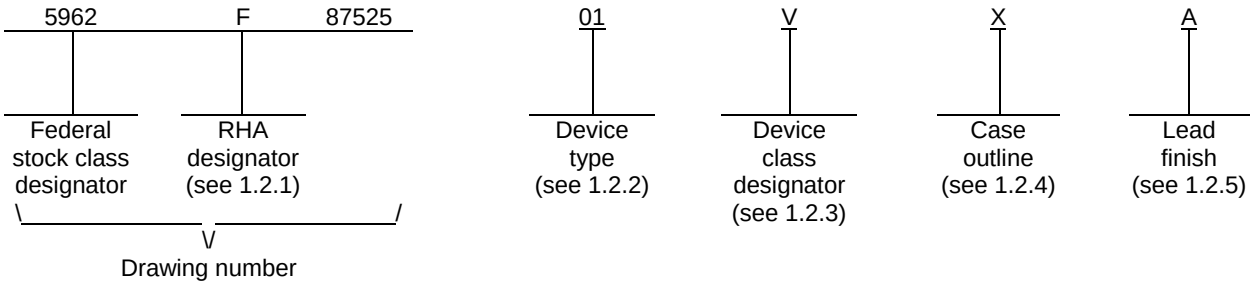
DSCC FORM 2233
APR 97

5962-E178-19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes M. B and Q) and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes B, S,Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT74	Dual D-type flip-flop with preset and clear, TTL compatible inputs
02	54ACT11074	Dual D-type flip-flop with preset and clear, TTL compatible inputs
03	54ACT74	Dual D-type flip-flop with preset and clear, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
B, S, Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
Z	GDFP1-G14	14	Flat pack with gullwing
X	CDFP3-F14	14	Flat pack 1/
Y	CDFP3-F14	14	Flat pack 2/
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes B, S Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Package case outline X flat pack with isolated lid.
2/ Package case outline Y flat pack with grounded lid.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}):
For device types 01-02 ..... -0.5 V dc to +6.0 V dc
For device type 03(Vendor cage code F8859) ..... -0.5 V dc to +7.0 V dc
DC input voltage (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA 3/
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds):
Case outlines X and Y ..... 260°C
Other case outlines except cases X and Y ..... 300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) ..... 0.8 V at V_{CC} = 4.5 V
0.8 V at V_{CC} = 5.5 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V at V_{CC} = 4.5 V
2.0 V at V_{CC} = 5.5 V
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise and fall rate (t_r and t_f) maximum:
V_{CC} = 4.5 V ..... 10 ns/V
V_{CC} = 5.5 V ..... 8 ns/V
Maximum high level output current (I_{OH}) ..... -24 mA
Maximum low level output current (I_{OL}) ..... 24 mA

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 Rad (Si)/s):
Device type 01 ..... 100K Rad (Si)
Device type 03 ..... 300K Rad (Si)
Heavy ion single event phenomenon (SEP):
Device type 01
No single event latch-up (SEL) occurs at effective LET (see 4.4.5.2) ..... ≤ 100 MeV-cm^2/ mg 5/
Device type 03:
No single event latch-up (SEL) occurs at effective LET (see 4.4.5.2) ..... ≤ 93 MeV-cm^2/ mg 5/
No single event upset (SEU) occurs at effective LET (see 4.4.5.2) ..... ≤ 93 MeV-cm^2/ mg 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.
4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.
5/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

JESD78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1} 5/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	4.5 V	1, 2, 3	4.4		V
	V_{OH2}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	5.5 V	1, 2, 3	5.4		
			M, D, P, L, R	01 B, S, Q, V		1	5.4		
	V_{OH3}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	4.5 V	1, 2, 3	3.7		
			M, D, P, L, R	01 B, S, Q, V		1	3.7		
	V_{OH4} 5/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	5.5 V	1, 2, 3	4.7		
	V_{OH5} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$		All All	5.5 V	1, 2, 3	3.85		
			M, D, P, L, R	01 B, S, Q, V		1	3.85		
Low level output voltage 3007	V_{OL1} 5/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = +50\ \mu A$		All All	4.5 V	1, 2, 3		0.1	V
	V_{OL2}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = +50\ \mu A$		All All	5.5 V	1, 2, 3		0.1	
			M, D, P, L, R	01 B, S, Q, V		1		0.1	
	V_{OL3}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = +24\ mA$		All B, S, Q, V	4.5 V	1, 3		0.4	V
						2		0.5	
				All M		1		0.4	
						2, 3		0.5	
			M, D, P, L, R	01 B, S, Q, V		1		0.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Low level output voltage 3007	V_{OL4} 5/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = +24\ mA$	All B, S, Q, V	5.5 V	1, 3		0.4	V
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
	V_{OL5} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = +50\ mA$	All All	5.5 V	1, 2, 3		1.65	
		M, D, P, L, R	01 B, S, Q, V		1		1.65	
Positive input clamp voltage 3022	V_{IC+}	For input under test, $I_{IN} = 1\ mA$	All B, S, Q, V	GND	1	0.4	1.5	V
		M, D, P, L, R	01 B, S, Q, V		1	0.4	1.5	
Negative input clamp voltage 3022	V_{IC-}	For input under test, $I_{IN} = -1\ mA$	All B, S, Q, V	Open	1	-0.4	-1.5	V
		M, D, P, L, R	01 B, S, Q, V		1	-0.4	-1.5	
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All B, S, Q, V	5.5 V	1		0.1	µA
					2		1.0	
			All M		1		0.1	
					2, 3		1.0	
		M, D, P, L, R	01 B, S, Q, V		1		0.1	
Input current low 3009	I_{IL}	For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All B, S, Q, V	5.5 V	1		-0.1	µA
					2		-1.0	
			All M		1		-0.1	
					2, 3		-1.0	
		M, D, P, L, R	01 B, S, Q, V		1		-0.1	
Input capacitance 3012	C_{IN}	See 4.4.1b $T_C = +25°C$	01, 03 All	GND	4		10.0	pF
			02 All		4		7.0	pF
Power dissipation capacitance	C_{PD} 7/	See 4.4.1b $T_C = +25°C$	01, 03 All	5.0 V	4		70.0	pF
			02 All		4		38.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 8/	For input under test, $V_{IN} = V_{CC} - 2.1\ V$; For all other inputs, $V_{IN} = V_{CC}$ or GND	01 B, S, Q, V	5.5 V	3		1.6	mA
					1, 2		1.0	
			03 Q, V		1, 2, 3		1.6	
			All M		1, 2, 3		1.6	
		M, D	01 B, S, Q, V		1		1.6	
		P, L, R					3.5	
Quiescent supply current output high 3005	I_{CCH}	For all other inputs, $V_{IN} = V_{CC}$ or GND	01, 02 B, S, Q, V	5.5 V	1		1.0	µA
					2		20.0	
			01, 02 M		1		4.0	
					2, 3		80.0	
			03 All		1		2.0	
					2, 3		40.0	
		M	01 B, S, Q, V		1		100.0	
		D					1.0	mA
		P, L, R					3.5	
		M, D, P, L, R, F 9/	03 Q, V		1		50	µA
Quiescent supply current output low 3005	I_{CCL}	For all other inputs, $V_{IN} = V_{CC}$ or GND	01, 02 B, S, Q, V	5.5 V	1		1.0	µA
					2		20.0	
			01, 02 M		1		4.0	
					2, 3		80.0	
			03 All		1		2.0	
					2, 3		40.0	
		M	01 B, S, Q, V		1		100.0	
		D					1.0	mA
		P, L, R					3.5	
		M, D, P, L, R, F 9/	03 Q, V		1		50	µA
Low level ground bounce noise	V_{GBL} 10/	$V_{LD} = 2.5\ V$, $I_{OL} = +24\ mA$ See figure 4	All B, S, Q, V	4.5 V	4		1000	mV
High level ground bounce noise	V_{GBH} 10/	$V_{LD} = 2.5\ V$, $I_{OH} = -24\ mA$ See figure 4	All B, S, Q, V	4.5 V	4		1000	mV

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Latch-up input/ output over-voltage	I_{CC} (O/V1) 11/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$, See 4.4.1b	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 11/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$, See 4.4.1b	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 11/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$, See 4.4.1b	All B, S, Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 11/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$, See 4.4.1b	All B, S, Q, V	5.5 V	2		100	mA
Truth table test output voltage 3014	12/	$V_{IL} = 0.40\ V$ $V_{IH} = 2.40\ V$ Verify output V_{OUT}	All All	4.5 V	7, 8	L	H	
			All M	5.5 V	7, 8	L	H	
		M, D, P, L, R	01 B, S, Q, V	4.5 V	7	L	H	
Propagation delay time, clock to output, CPn to Qn and $\overline{Qn}$ 3003	t_{PHL1}, t_{PLH1} 13/ 14/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 5	01, 03 B, S, Q, V	4.5 V	9, 11	1.0	11.0	ns
					10	1.0	14.0	
			01 M		9	1.0	11.0	
					10, 11	1.0	14.0	
			02 M		9	1.0	8.5	
					10, 11	1.0	10.0	
		M, D, P, L, R	01 B, S, Q, V		9	1.0	11.0	
Propagation delay time, clear and set to output $\overline{CDn}$ and $\overline{SDn}$ to $\overline{Qn}$ and Qn 3003	t_{PHL2}, t_{PLH2} 13/ 14/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 5	01, 03 B, S, Q, V	4.5 V	9, 11	1.0	10.0	ns
					10	1.0	12.5	
			01 M		9	1.0	10.0	
					10, 11	1.0	12.5	
			02 M		9	1.0	11.3	
					10, 11	1.0	13.3	
		M, D, P, L, R	01 B, S, Q, V		9	1.0	10.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Maximum operating frequency 3003	f_{MAX}	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1f	01, 03 B, S, Q, V	4.5 V	9, 11	95		MHz
					10	85		
			01 M		9	95		
					10, 11	85		
			02 M		9	100		
					10, 11	100		
Input set-up time, Dn (high and low) to CPn	t_s	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1g	01, 03 B, S, Q, V	4.5 V	9	3.0		ns
					10, 11	4.0		
			01 M		9	3.0		
					10, 11	4.0		
			02 M		9	4.5		
					10, 11	4.5		
Input hold time, Dn (high and low) after CPn	t_h	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1g	01, 03 B, S, Q, V	4.5 V	9, 10, 11	1.0		ns
			01 M		9, 10, 11	1.0		
			02 M		9, 10, 11	0.0		
Input recovery time, $\overline{CDn}$ and $\overline{SDn}$ to CPn	t_{REC}	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1g	01, 03 B, S, Q, V	4.5 V	9, 11	0.5		ns
					10	0.5		
			01 M		9	0.5		
					10, 11	0.5		
			02 M		9	2.0		
					10, 11	2.0		
Clock pulse width (high and low)	t_{w1}	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1g	01, 03 B, S, Q, V	4.5 V	9, 11	5.0		ns
					10	5.0		
			01 M		9	5.0		
					10, 11	6.0		
			02 M		9	5.0		
					10, 11	5.0		
$\overline{CDn}$ and $\overline{SDn}$ pulse width (low)	t_{w2}	C_L = 50 pF minimum R_L = 500Ω See figure 5 See 4.4.1g	01, 03 B, S, Q, V	4.5 V	9, 11	6.5		ns
					10	7.0		
			01 M		9	6.5		
					10, 11	7.0		
			02 M		9	5.0		
					10, 11	5.0		

See footnotes on next sheet.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

RHA parts for device type 03 supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table IA.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V. For device class M, subgroup 1 testing shall be guaranteed if not tested to the limits specified in table IA. For radiation hardness assured devices, subgroup 1 tests shall be performed.

7/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption (P_D) and the dynamic current consumption (I_S), where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$

f is the frequency of the input signal; n is the number of device inputs at TTL levels; d is the duty cycle of the input signal; and C_L is the external output load capacitance.

8/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0.0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum limit; and the preferred method and limits are guaranteed.

9/ The maximum limit for this parameter at 100 krads (Si) is 2 µA.

10/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = ±24 mA, for example) and 50 pF of load capacitance (see figure 4). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f$ = 3.5 ±1.5 ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 4). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

11/ See EIA/JESD78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent.

12/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances per MIL-STD-883 already incorporated.

13/ Device classes B, S, Q, and V are tested at V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested (see 4.4.1d).

14/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	Bias V_{CC} = 4.5 V Effective LET SEU	Bias V_{CC} = 5.5 V for SEL testt no SEL occurs effective LET
01		LET ≤ 100 MeV/(mg/cm^2)
03	LET ≤ 93 MeV/(mg/cm^2)	LET ≤ 93 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.5.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Tested for upsets at worst case temperature, T_A = +25°C ± 10°C and T_A = +125°C ± 10°C for latch-up.

Device types	01 and 03		02	
Case outlines	C, D, X, Y, and Z	2	C and D	2
Terminal number	Terminal symbol			
1	$\overline{CD1}$	NC	$\overline{SD1}$	NC
2	D1	$\overline{CD1}$	Q1	$\overline{CD1}$
3	CP1	D1	$\overline{Q}1$	D1
4	$\overline{SD1}$	CP1	GND	CP1
5	Q1	NC	$\overline{Q}2$	NC
6	$\overline{Q}1$	$\overline{SD1}$	Q2	$\overline{SD1}$
7	GND	NC	$\overline{SD2}$	NC
8	$\overline{Q}2$	Q1	CP2	Q1
9	Q2	$\overline{Q}1$	D2	$\overline{Q}1$
10	$\overline{SD2}$	GND	$\overline{CD2}$	GND
11	CP2	NC	V_{CC}	NC
12	D2	$\overline{Q}2$	$\overline{CD1}$	$\overline{Q}2$
13	$\overline{CD2}$	Q2	D1	Q2
14	V_{CC}	$\overline{SD2}$	CP1	$\overline{SD2}$
15	---	NC	---	NC
16	---	CP2	---	CP2
17	---	NC	---	NC
18	---	D2	---	D2
19	---	$\overline{CD2}$	---	$\overline{CD2}$
20	---	V_{CC}	---	V_{CC}

NC = No internal connection

FIGURE 1. Terminal connections.

Device types 01, 02, and 03					
Inputs				Outputs	
$\overline{SDn}$	$\overline{CDn}$	CPn	Dn	Qn	$\overline{Q}n$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H *	H *
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}0$

H = High voltage level
L = Low voltage level
X = Irrelevant
Q0 ($\overline{Q}0$) = Previous Qn ($\overline{Q}n$) before low-to-high transition of clock.
* = This configuration is nonstable; that is, it will not persist when either preset ($\overline{SDn}$) or clear ($\overline{CDn}$) returns to its inactive state (high voltage level).
↑ = Low-to-high clock transition

FIGURE 2. Truth table.

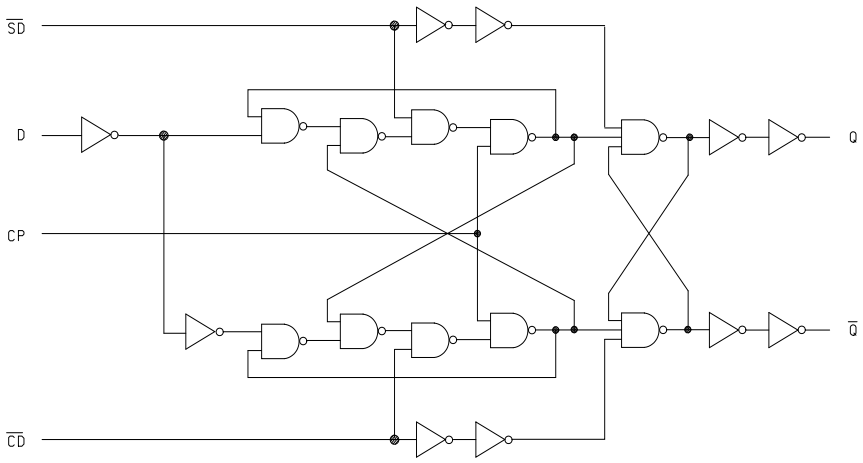
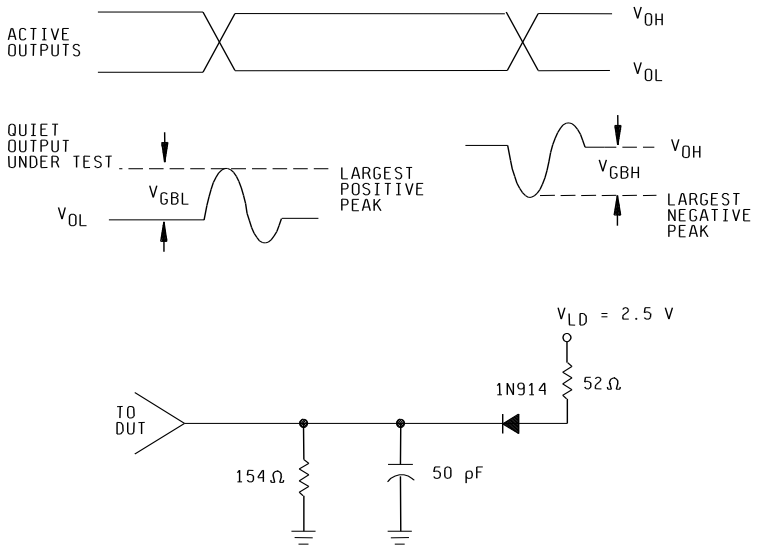


FIGURE 3. Logic diagram.



NOTE: Resistor and capacitor tolerances = ±10%

FIGURE 4. Ground bounce waveforms and test circuit.

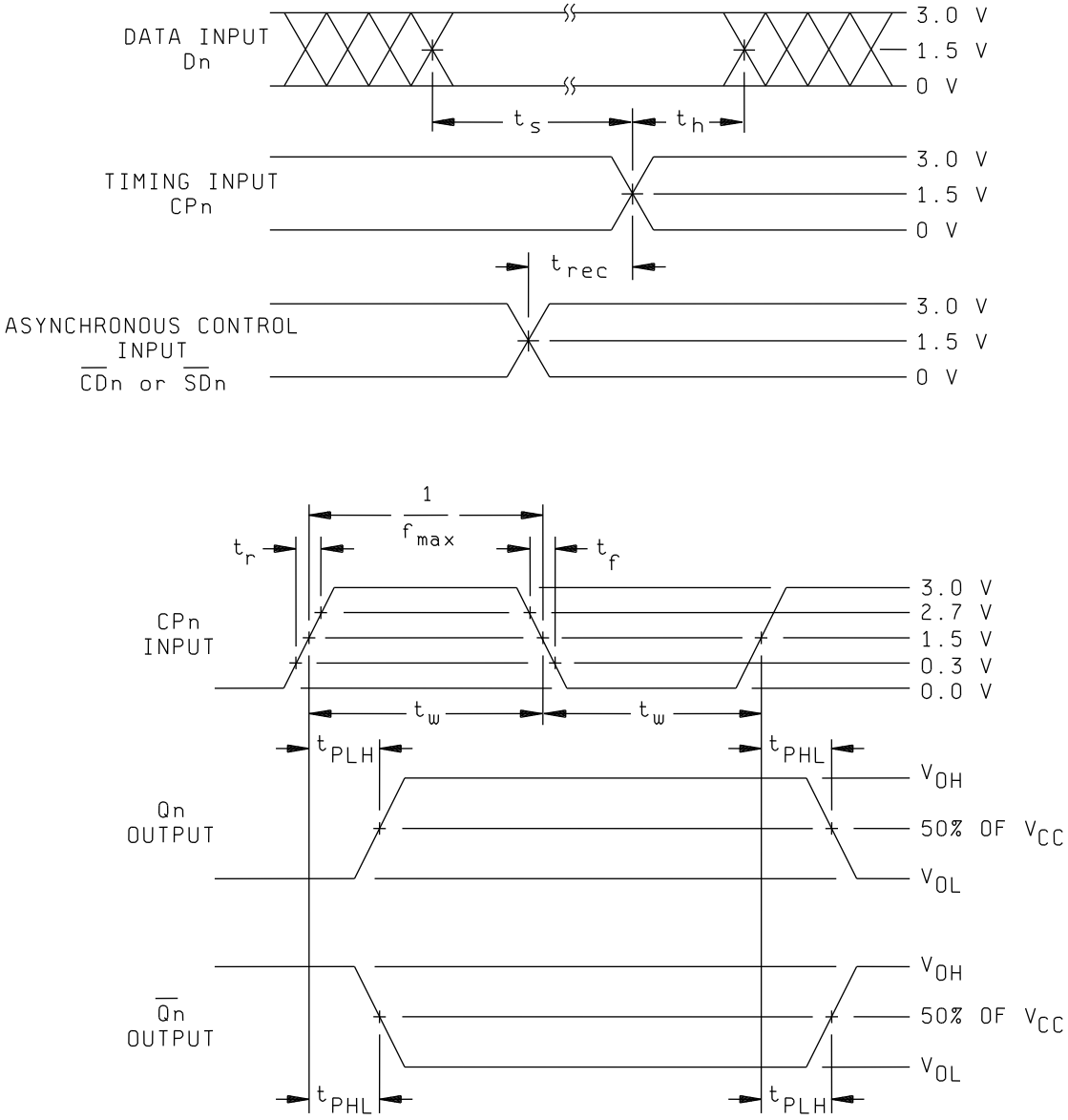
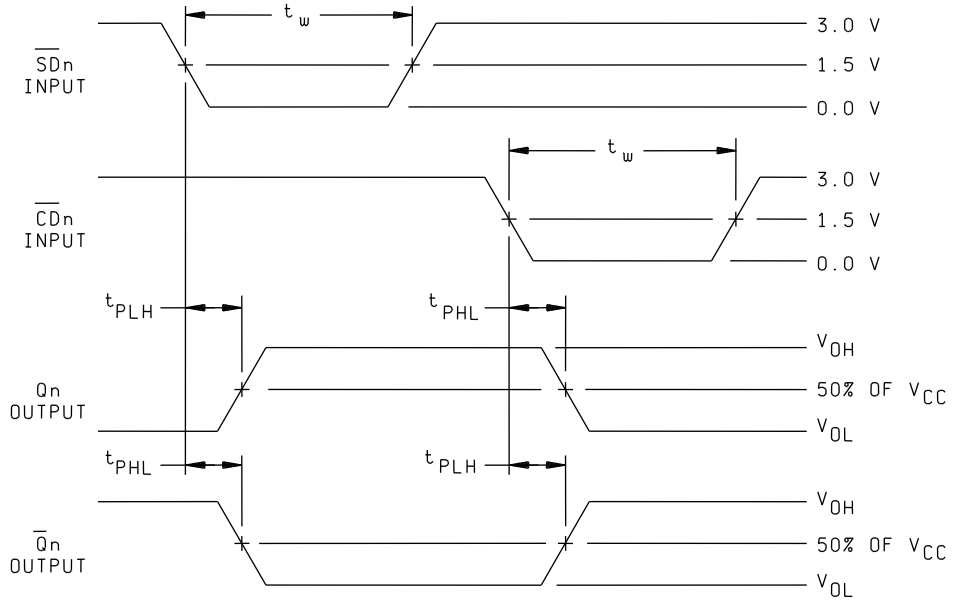
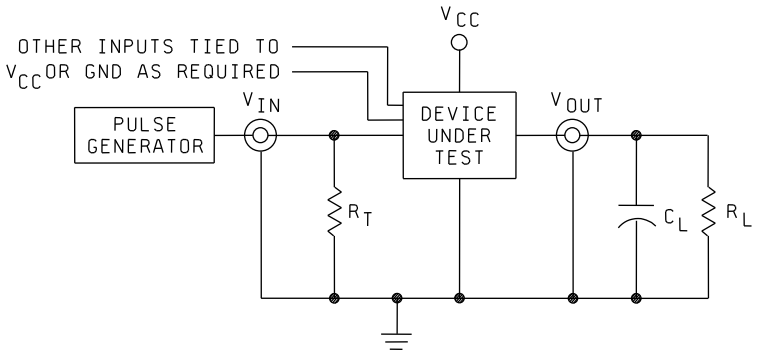


FIGURE 5. Switching waveforms and test circuit.





NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes B, S, Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute the first 7 test requirements of table IIA herein.

(4) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Unless otherwise specified in the QM plan for static burn-in, device classes B and S, test condition A of method 1015 of MIL-STD-883; the test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table IA of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ

(c) V_{CC} = 5.5 V +0.5 V, -0.0 V.

(6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D of method 1015 of MIL-STD-883, the following shall apply:

(a) Input resistors = 220Ω to 2 kΩ ±20 percent.

(b) Output resistors = 220Ω ±20 percent.

(c) V_{CC} = 5.5 V +0.5 V, -0.0 V.

(d) The $\overline{SDn}$ and $\overline{CDn}$ pins shall be connected through the resistors in parallel to V_{CC}. The clock inputs (CPn) shall be connected through resistors to a clock pulse (CP1). The data pins (Dn) shall be connected through resistors to a clock pulse (CP2). Outputs shall be connected through the resistors to $V_{CC}/2 \pm 0.5$ V.

(e) CP1, CP2 = 25 kHz to 1 MHz square wave; $f_{CP2} = f_{CP1}/2$; duty cycle = 50 percent ±15 percent; V_{IH} = 4.5 V to V_{CC}; V_{IL} = 0 V ±0.5 V; t_r, $t_f \leq 100$ ns.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table I)	Subgroups 1/ (in accordance with MIL-PRF-38535, table III)			
	Device class M	Device 2/ class B	Device 2/ class S	Device class Q	Device class V
Interim electrical parameters, method 5004		1	1	1	1
Static burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)		1 2/ 5/	1 2/ 5/	1 2/ 5/	1 2/ 5/
Dynamic burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004	1, 2, 3, 7, 8, 9 2/	1, 2, 7, 9 2/ 6/	1, 2, 7, 9 2/	1, 2, 3, 7, 8, 9, 10, 11 2/ 6/	1, 2, 3, 7,8, 9, 10, 11 2/
Group A test requirements, method 5005 (4.4.1)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters, method 5005 (4.4.2)			1, 2, 3, 7, 8, 9, 10, 11 5/		
Group C end-point electrical parameters, method 5005 (4.4.3)	1, 2, 3	1, 2 5/		1, 2, 3 5/	1, 2, 3, 7, 8, 9, 10, 11 5/
Group D end-point electrical parameters, method 5005 (4.4.4)	1, 2, 3	1, 2	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters, method 5005 (4.4.5)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).

3/ The burn-in shall meet the requirements of 4.2.1a herein.

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.

5/ Delta limits shall be required only on table IA , subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.

6/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device types	Delta limits
Supply current	I_{CCH}, I_{CCL}	01	±100 nA 2/
		03	±300 nA
Supply current delta	ΔI_{CC}	03	±0.4 mA
Input current low level	I_{IL}	03	±20 nA
Input current high level	I_{IH}	03	±20 nA
Output voltage low level V_{CC} = 5.5 V, I_{OL} = +24 mA	V_{OL}	03	±0.04 V
Output voltage high level V_{CC} = 5.5 V, I_{OH} = -24 mA	V_{OH}	03	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Guaranteed, if not tested.

4.2.2 Additional criteria for device classes B, S, Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device classes V or S beyond the requirements of device classes Q or B shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535, for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table IA, subgroup I, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection for device classes B, S, Q and V. Qualification inspection for device classes B, S, Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Latch-up and ground bounce tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD20 and table IA herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. The test vectors used to verify the truth table shall test all possible input to output logic patterns. For device classes B, S, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

f. For device classes B, S, Q, and V, f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with zero failures.

g. For device classes B, S, Q, and V, t_s, t_h, t_{REC}, and t_w shall be guaranteed, if not tested, to the limits specified in table IA.

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes B, S, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25□C □5□C, after exposure, to the subgroups specified in table IIA herein.

c. RHA tests for device classes M, B, S, Q, and V for levels M, D, P, L, R, and F, shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

a. Device type 01:

(1) Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Device type 03:

(1) Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.5.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.1.2.1 Substitution data.

New PIN	Old PIN
5962-8752501MCA	5962-8752501CA
5962-8752501MDA	5962-8752501DA
5962-8752501M2A	5962-87525012A
5962-8752502MCA	5962-8752502CA
5962-8752502M2A	5962-87525022A

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q and V. Sources of supply for device classes B, S, Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

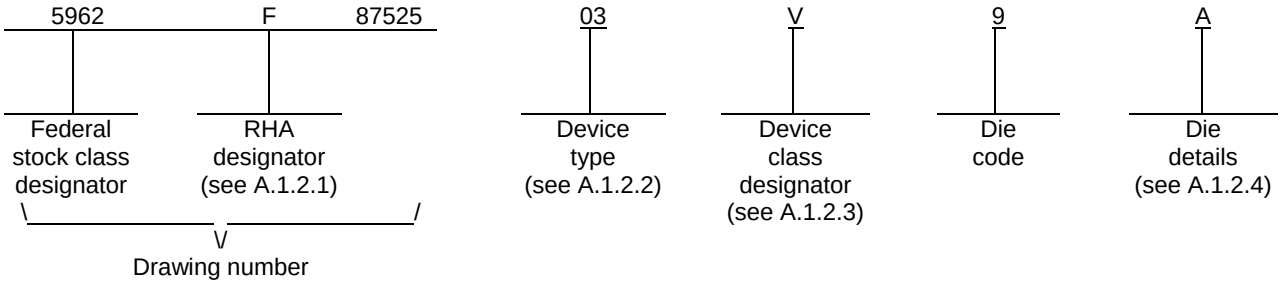
c. SEU as written.

d. SEL as written.

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
03	54ACT74	Dual D-type flip-flop with preset and clear TTL compatible inputs

A.1.2.3 Device class designator. Device class Q designator will not be included in the PIN and will not be marked on the device since the device class designator has been added after the original issuance of this drawing.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specification, standards, and handbooks. The following specification, standard, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

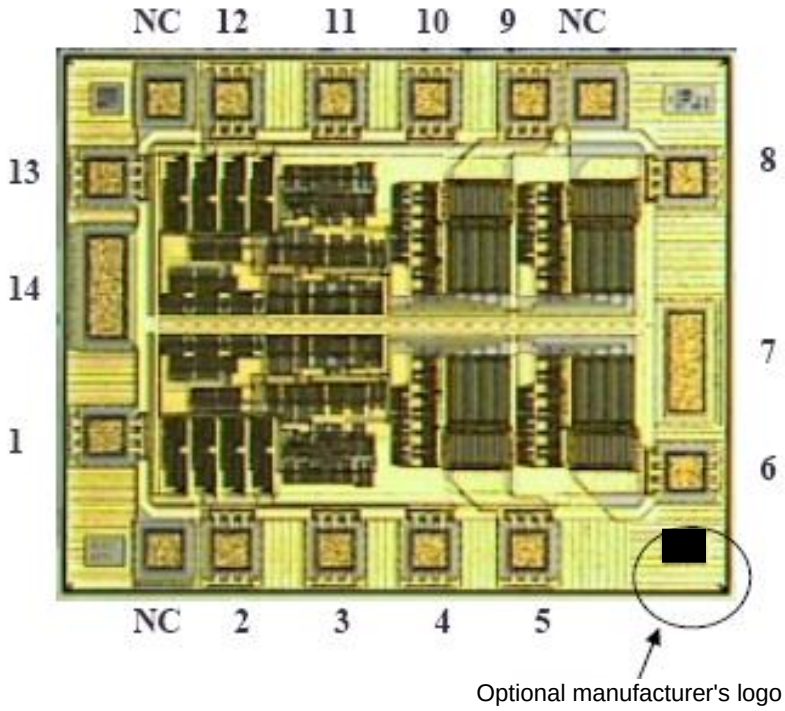
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Pad size:	Pad numbers 1 to 6 and 8 to 13:	100 x 100 μm
	Pad numbers 7 (GND) and 14 (V_{CC}):	100 x 280 μm

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1 Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	1941.2 x 1577.2 μm
Die thickness:	285 ±25 μm

Interface materials.

Top metallization:	Al Si Cu Thickness = 0.85 μm
Backside metallization:	None
Glassivation.	
Type:	P. Vapox + Nitride
Thickness:	0.5 μm – 0.7 μm
Substrate:	Silicon

Assembly related information.

Substrate potential:	Floating or tied to GND
Special assembly instructions:	Bond pad #14 (V_{CC}) first

FIGURE A-1 Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-01-29

Approved sources of supply for SMD 5962-87525 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8752501MCA	01295	SNJ54ACT74J
	0C7V7	54ACT74DMQB
		EV54ACT74DMQB
5962-8752501MDA	01295	SNJ54ACT74W
	0C7V7	54ACT74FMQB
		EV54ACT74FMQB
5962-8752501M2A	01295	SNJ54ACT74FK
	0C7V7	54ACT74LMQB
		EV54ACT74LMQB
5962-8752501BCA	0C7V7	JM54ACT74BCA
		EV54ACT74BCA
	3V146	54ACT74/BCA
5962-8752501BDA	0C7V7	JM54ACT74BDA
		EV54ACT74BDA
	3V146	54ACT74/BDA
5962-8752501B2A	0C7V7	JM54ACT74B2A
		EV54ACT74B2A
	3V146	54ACT74/B2A
5962-8752501SCA	3/	54ACT74
5962-8752501SDA	3/	JM 54ACT74SDA
5962-8752501S2A	3/	54ACT74
5962R8752501BCA	3/	54ACT74
5962R8752501BDA	3/	54ACT74
5962R8752501B2A	3/	54ACT74
5962R8752501SCA	3/	JM54ACT74SCA-RH
5962R8752501SDA	3/	JM54ACT74SDA-RH
5962R8752501SZA	3/	JM54ACT74SZA-RH
5962R8752501S2A	3/	JM54ACT74S2A-RH
5962-8752502M2A	3V146	54ACT11074/B2A
5962-8752502MCA	3V146	54ACT11074/BCA
5962-8752502MDA	3V146	54ACT11074/BDA
5962-8752503QXA	3/	54ACT74K02Q
5962-8752503QXC	3/	54ACT74K01Q
5962-8752503VXA	3/	54ACT74K02V
5962-8752503VXC	3/	54ACT74K01V

See footnotes on next sheet.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F8752503QCA	F8859	RHFACT74D04Q
5962F8752503QCC	F8859	RHFACT74D03Q
5962F8752503QXA	F8859	RHFACT74K02Q
5962F8752503QXC	F8859	RHFACT74K01Q
5962F8752503VCA	F8859	RHFACT74D04V
5962F8752503VCC	F8859	RHFACT74D03V
5962F8752503VXA	F8859	RHFACT74K02V
5962F8752503VYA	F8859	RHFACT74K04V
5962F8752503VXC	F8859	RHFACT74K01V
5962F8752503VYC	F8859	RHFACT74K03V
5962F8752503V9A	F8859	ACT74DIE2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243