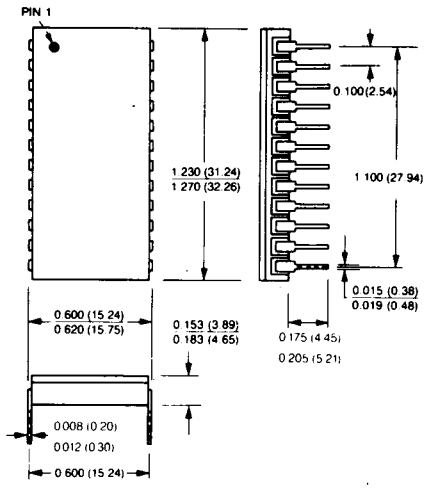
12-bit D/A Converter with Input Register

FEATURES

- Complete With Internal:
  - Input Register
  - Output Op Amp
  - Low-Drift Reference
- ±1/2 LSB Max Linearity Error
- Monotonicity Guaranteed Over Temperature
- 50nsec Data Setup Time
- 4μsec Settling Time
- 5 Output Ranges
  2 Coding Options
- Multisourced
- Full Mil Operation
  −55°C to +125°C
- MIL-PRF-38534 Screening Optional

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

DACHK is a complete, voltage-output, 12-bit D/A converter that contains a low-drift reference and a high-speed input register to facilitate microprocessor interfacing. The register has a minimum setup time of 50nsec; a hold time of 0nsec; and pulses as narrow as 60nsec can be used to latch new data. Output settling time for a 20V step settling to ±½LSB is 4μsec.

DACHK is packaged in a standard, hermetically-sealed, 24-pin, ceramic dual-in-line and offers 5 user-selectable output ranges (0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V) and 2 input coding options (straight binary or two's complement). Units require ±15V and +5V supplies and consume 975mW of power.

DACHK is functionally laser trimmed for linearity, gain and offset, eliminating the need for external trimming potentiometers. Units are available for two operating temperature ranges (0°C to +70°C, and −55°C to +125°C), and each unit guarantees 12-bit monotonicity over its entire range. For military/aerospace or harsh environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-PRF-38534.

Model Number	Coding	Specified Temp. Range
DACHK	Straight Binary	0°C to +70°C
DACHKH	Straight Binary	−55°C to +125°C
DACHKH/B	Straight Binary	−55°C to +125°C
DACHKH/B CH	Straight Binary	−55°C to +125°C
DACHK-2	Two's Complement	0°C to +70°C
DACHK-2H	Two's Complement	−55°C to +125°C
DACHK-2H/B	Two's Complement	−55°C to +125°C
DACHK-2H/BCH	Two's Complement	−55°C to +125°C

DACHK 12-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
DACHK, DACHK-2	0°C to +70°C
DACHKH, H/B; DACHK-2H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 22)	0 to +18 Volts
Negative Supply (−Vcc, Pin 14)	0 to −18 Volts
Logic Supply (+Vdd, Pin 13)	−0.5 to +7 Volts
Register Enable (Pin 16)	−0.5 to +5.5 Volts
Digital Inputs (Pins 1-12)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — DACHK-2H/BCH

Standard Part is specified for 0°C to +70°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

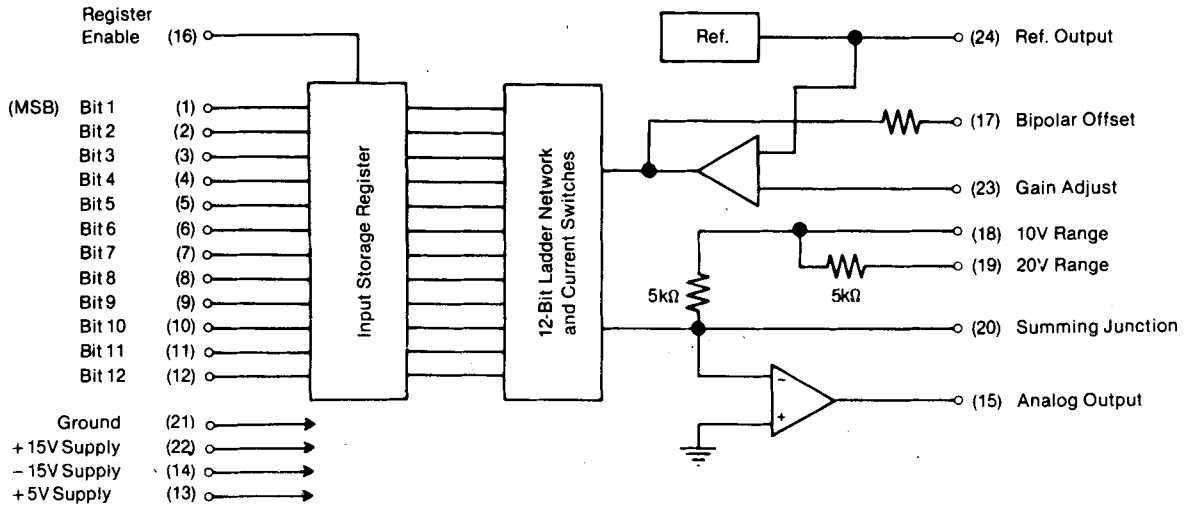
SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Input Currents: Data Inputs: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V) Register Enable: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)		+20 −0.4 +60 −1.2		µA mA µA mA
Logic Coding (Note 2): DACHK: Unipolar Ranges Bipolar Ranges DACHK-2: Bipolar Ranges		Straight Binary Offset Binary Two's Complement		
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar Bipolar		0 to +5, 0 to +10 ±2.5, ±5, ±10		Volts Volts
Output Current	±5			mA
Output Impedance		0.05		Ω
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error		± ¼	± ½	LSB
Differential Linearity Error		± ½		LSB
Temperature Range for Guaranteed Monotonicity: DACHK, DACHK-2 DACHKH, H/B; DACHK-2H, H/B	 0 −55		 +70 +125	 °C °C
Unipolar Offset Error (Notes 4, 5)		±0.1		%FSR
Bipolar Offset Error (Notes 4, 6)		±0.1		%FSR
Gain Error (Notes 4, 7)		±0.1		%
DRIFT SPECIFICATIONS (Note 8)				
Integral Linearity Drift Unipolar Offset Drift Bipolar Offset Drift Gain Drift		±2 ±3 ±7 ±15	 ±5 ±10 ±20	ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ± ½ LSB: 20V Step 10V Step 1 LSB		4 3 0.8		µsec µsec µsec
Slew Rate		±20		V/µsec
POWER SUPPLIES				
Power Supply Range: +15V Supply −15V Supply +5V Supply	+14.55 −14.55 +4.75	+15 −15 +5	+15.45 −15.45 +5.25	Volts Volts Volts
Power Supply Rejection: +15V Supply −15V Supply		±0.002 ±0.002		%FSR/%Supply %FSR/%Supply
Current Drain: +15V Supply −15V Supply +5V Supply		+20 −35 +30		mA mA mA
Power Consumption		975		mW

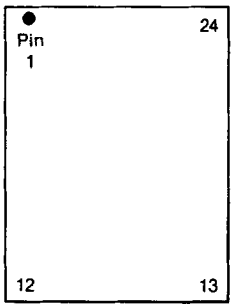
SPECIFICATION NOTES:

1. Unless otherwise indicated, listed specifications apply for all DACHK and DACHK-2 models.
2. DACHK is available with either binary input coding (DACHK, DACHKH, and DACHKH/B) or two's complement input coding (DACHK-2, DACHK-2H and DACHK-2H/B). See Ordering Information.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ±10V output range, FSR is 20V, and 1 LSB is ideally equal to 4.88mV. For the 0 to +10V and ±5V ranges, FSR is 10V, and 1 LSB is ideally equal to 2.44mV. For the 0 to +5V and ±2.5 ranges, FSR is 5V, and 1 LSB is ideally equal to 1.22mV.
4. Initial offset and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Unipolar offset error is defined as the difference between the actual and the ideal output voltage when configured in a unipolar output range with a digital input of 0000 0000 0000.
6. Bipolar offset error is defined as the difference between the actual and the ideal output voltage when configured in a bipolar output range with a digital input of 0000 0000 0000 (1000 0000 0000 for DACHK-2 models).
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 1111 1111 1111 (0111 1111 1111 for DACHK-2 models) output to the 0000 0000 0000 (1000 0000 0000 for DACHK-2 models) output.
8. Drift specifications apply over the 0°C to +70°C temperature range for DACHK and DACHK-2; and over the −55°C to +125°C temperature range for DACHKH, DACHKH/B and DACHK-2H, DACHK-2H/B.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Bit 1 (MSB)	24	Ref. Out (+6.2V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply (+Vcc)
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Register Enable
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply (−Vcc)
12	Bit 12 (LSB)	13	+5V Supply (+Vdd)

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the DACHK. The unit's Ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used.

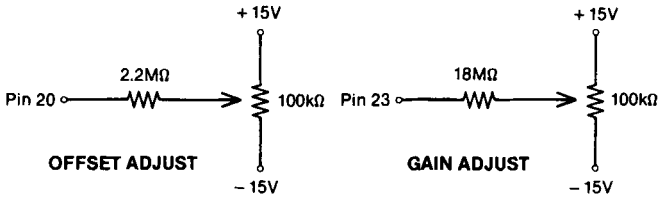
Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

REFERENCE OUTPUT—The DACHK contains an internal +6.2V reference, and the units are actively laser trimmed to operate from this reference. If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 20μA.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS — The DACHK will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be grounded.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "0's" to the digital inputs.* Adjust the potentiometer until the analog output is equal to zero volts for the unipolar output ranges or negative full scale for bipolar output ranges.

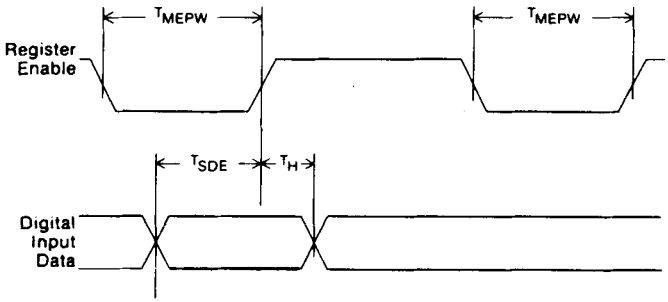
GAIN ADJUSTMENT—Connect the gain potentiometers as shown and apply all "1's" to the digital inputs.** Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Input Logic Coding table.



* "1" and all "0's" for 2's complement ** "0" and all "1's" for 2's complement

REGISTER ENABLE—When the Register Enable (pin 16) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nsec and digital input data must be valid for a minimum of 50nsec prior to Register Enable going high again. See Timing Diagram.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW}	Minimum Enable Pulse Width is 60nsec.
T_{SDE}	Minimum Setup Time Digital Data to Enable is 50nsec.
T_H	Digital Data Hold Time from Register Enable is 0nsec.

INPUT LOGIC CODING

STRAIGHT BINARY			OUTPUT RANGES	
MSB		LSB	0 to +5V	0 to +10V
1111	1111	1111	+4.9988	+9.9976
1100	0000	0000	+3.7500	+7.5000
1000	0000	0000	+2.5000	+5.0000
0100	0000	0000	+1.2500	+2.5000
0000	0000	0001	+0.0012	+0.0024
0000	0000	0000	0.0000	0.0000

OFFSET BINARY			TWO'S COMPLEMENT			OUTPUT RANGES		
MSB		LSB	MSB		LSB	±2.5V	±5V	±10V
1111	1111	1111	0111	1111	1111	+2.4988	+4.9976	+9.9951
1100	0000	0000	0100	0000	0000	+1.2500	+2.5000	+5.0000
1000	0000	0000	0000	0000	0000	0.0000	0.0000	0.0000
0100	0000	0000	1100	0000	0000	−1.2500	−2.5000	−5.0000
0000	0000	0001	1000	0000	0001	−2.4988	−4.9976	−9.9951
0000	0000	0000	1000	0000	0000	−2.5000	−5.0000	−10.0000

CODING NOTES:

1. For unipolar operation, the coding is straight binary.
2. For bipolar operation, the coding is either offset binary or two's complement.
3. For FSR = 20V, 1 LSB = 4.88mV
4. For FSR = 10V, 1 LSB = 2.44mV
5. For FSR = 5V, 1 LSB = 1.22mV

OUTPUT RANGE SELECTION

Pin Connections	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Pin 15 to	18	18	18	18	19
Connect Pin 17 to	21	21	20	20	20
Connect Pin 19 to	20	—	20	—	15