Description

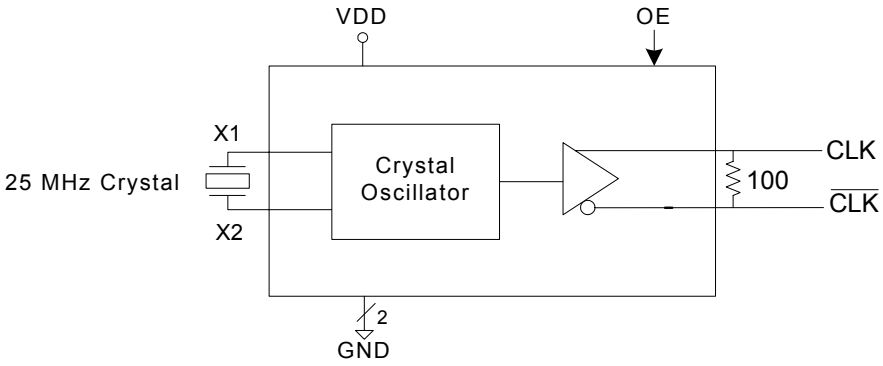
The ICS556-01 generates a high performance, low jitter Low Voltage Differential Signaling (LVDS) clock supporting traditional gigabit ethernet, fibre channel, and other serdes. Using a standard, low cost 25 MHz crystal, the device outputs a single reference (25 MHz) differential (LVDS) output clock with phase jitter below 1 ps.

The operating voltage is 2.5 V to support today's popular interfaces while minimizing power consumption. Off-chip termination using a resistor provides a flexible architecture.

Features

- Packaged in 8-pin TSSOP
- Requires no external components
- Low Phase Jitter: <1 ps from 10 kHz to 10 MHz
- Differential LVDS outputs
- Operating voltage of 2.5 V.
- Advanced, low power, sub-micron CMOS process

Block Diagram



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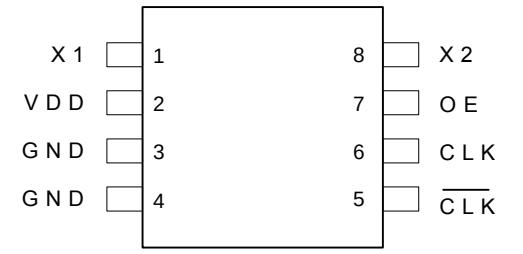
Pin Assignment



8 Pin (173mil) TSSOP or SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection.
2	VDD	Power	Power supply. Connect to 2.5 V.
3	GND	Power	Connect to ground.
4	GND	Power	Connect to ground.
5	$\overline{CLK}$	Output	Inverting differential clock output.
6	CLK	Power	Differential clock output.
7	OE	Input	Output Enable. Internal pull-up resistor.
8	X2	Input	Crystal connection.

External Component Selection

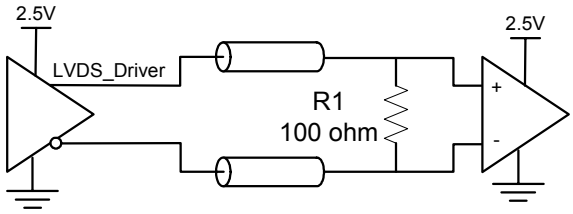
The ICS556-01 requires a minimum number of external components for proper operation. A 100Ω termination resistor between CLK and $\overline{CLK}$ is provided on-chip.

Decoupling Capacitors

A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 2 and 3 as close to the ICS556-01 as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

LVDS Driver Termination

A general LVDS interface is shown in Figure 2. In a 100 differential transmission line environment, LVDS drivers require a matched load termination of 100 across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.



100 Ohm Differential Transmission Line

FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

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Quartz Crystal

The ICS556-01 25 MHz LVDS Clock utilizes an external crystal to generate a low phase noise output. To assure the best system performance and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The crystal specified for use with the ICS556-01 is designed to have zero frequency error when the total of on-chip plus stray capacitance is 5 pF.

Recommended Crystal Parameters:

Initial Accuracy of 25° C±20 ppm
Temperature Stability±20 ppm
Load Capacitance5 pf
Shunt Capacitance, C02 pF Max
Equivalent Series Resistance80 Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS556-01. There should be no via’s between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

The value (in pF) of these crystal caps should equal (C_L - 12 pF)*2. In this equation, C_L =crystal load capacitance in pF. Example: or a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF [(16-12) x 2] = 8.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS556-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+2.375		+2.625	V
Reference crystal parameters	Refer to page 3			

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DC Electrical Characteristics

VDD=2.5 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Output High Voltage	V_{OH}	Note 1	1.375			V
Output Low Voltage	V_{OL}	Note 1			1.125	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, OE = 1		5.3		mA
		No load, OE = 0		1.7		mA

Note 1: Outputs terminated with 50Ω to VDD/2

AC Electrical Characteristics

VDD = 2.5 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Frequency			25		MHz
Output Frequency			25		MHz
Differential Output Voltages (V_{OD})		250	350	450	mV
Δ V_{OD}	V_{OD} Magnitude Change	-40	0	40	mV
Offset Voltage (V_{OS})		1.125	1.25	1.375	V
Δ V_{OS}	V_{OS} Magnitude Change		3	25	mV
Differential Output Short Circuit Current (I_{OSD})			-3.5		mA
Output Short Circuit Current (I_{OS})			-3.5		mA
Output Rise Time	20% to 80%, no load		0.8	1.2	ns
Output Fall Time	20% to 80%, no load		0.8	1.2	ns
Output Clock Duty Cycle	Measured at 1.25 V, C_L=5 pF	45	50	55	%
Maximum Output Jitter (p-p)	C_L=5 pF		40		ps
Phase Jitter (RMS)	Phase Noise integrated from 10 kHz to 10 MHz		1.8	2.5	ps

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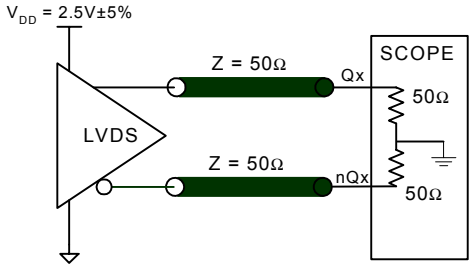
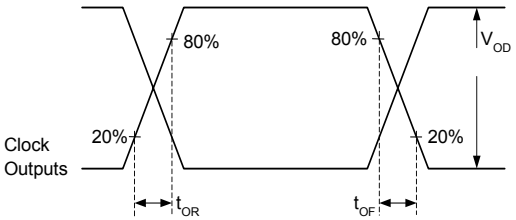
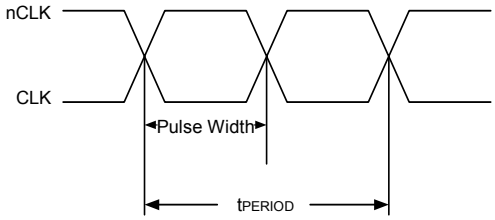
Parameter Measurement Information



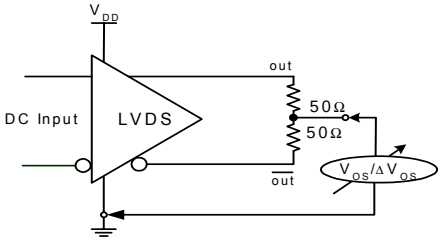
2.5V OUTPUT LOAD AC TEST CIRCUIT



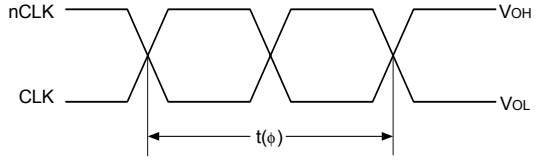
OUTPUT RISE/FALL TIME



tPW & tPERIOD

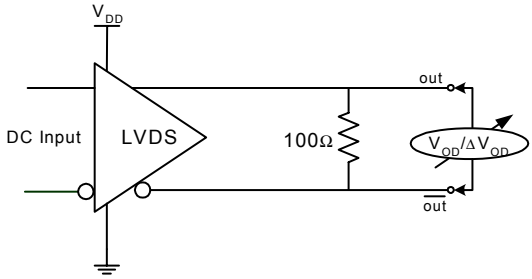


V_{OS} SETUP

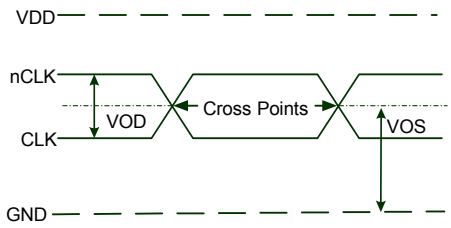


$t_{jit(\phi)} = |t_{(\phi)} - t_{(\phi)mean}|$ = Phase Jitter

PHASE JITTER



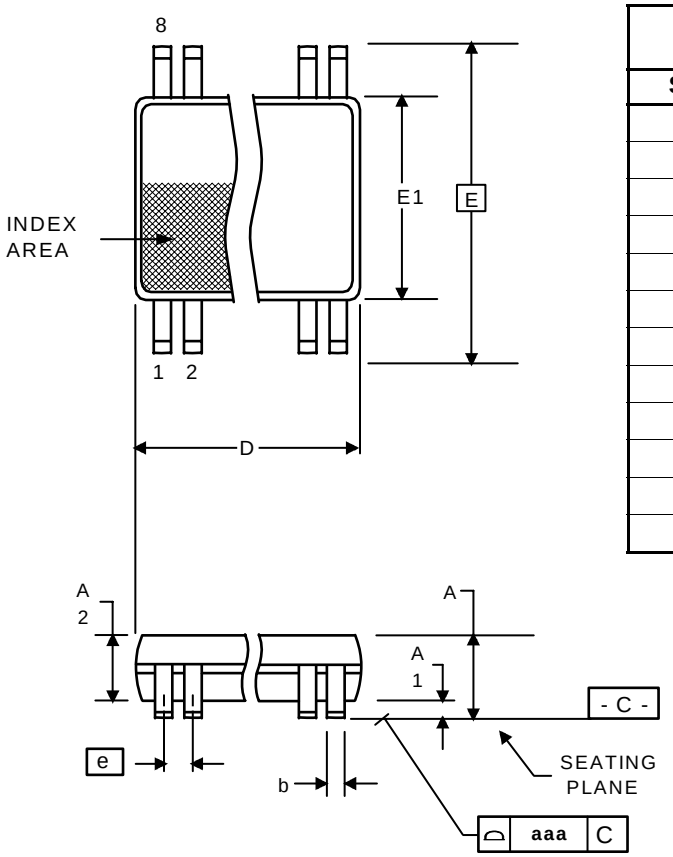
V_{OD} SETUP



DIFFERENTIAL INPUT LEVEL

Package Outline and Package Dimensions (8-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	2.90	3.10	0.114	0.122
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
556G-01	556G-01	Tubes	8-pin TSSOP	0 to +70° C
556G-01T	556G-01	Tape and Reel	8-pin TSSOP	0 to +70° C