VN2406 SERIES
N-Channel Enhancement-Mode MOS Transistors

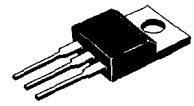
Siliconix incorporated

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2406D	240	6	1.12	TO-220
VN2406L	240	6	0.22	TO-92
VN2406M	240	6	0.25	TO-237

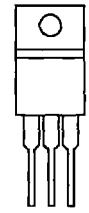
Performance Curves: VNDB24

TO-220

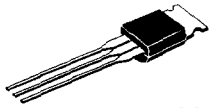


1 GATE
2 & TAB-DRAIN
3 SOURCE

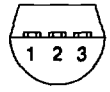
FRONT VIEW



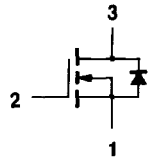
TO-237



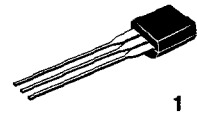
BOTTOM VIEW



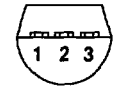
1 SOURCE
2 GATE
3 & TAB-DRAIN



TO-92 (TO-226AA)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN2406D	LIMITS VN2406L	LIMITS VN2406M	UNITS
Drain-Source Voltage		V_{DS}	240	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	1.12	0.17	0.19	A
	T_A = 100°C		0.7	0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	3	1.7	2	
Power Dissipation	T_A = 25°C	P_D	20	0.8	1	W
	T_A = 100°C		8	0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN2406D	LIMITS VN2406L	LIMITS VN2406M	UNITS
Junction-to-Ambient	R_{thJA}	6.25	156	125	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	270	240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	5		6	
		T_J = 125°C	10.8		14.8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		20	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω	3		8	ns
	t_r		2		8	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	13		18	
	t_f		9		12	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

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