SN74CBT3244 OCTAL FET BUS SWITCH

SCDS001I - NOVEMBER 1992 - REVISED MAY 2000

 Functionally Equivalent to QS3244 Standard '244-Type Pinout 	DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)				
 5-Ω Switch Connection Between Two Ports 					
TTL-Compatible Input Levels					
 Package Options Include Plastic 	2B4 🛛 3 18 🛛 1B1				
Small-Outline (DW), Shrink Small-Outline	1A2 4 17 2A4				
(DB, DBQ), Thin Very Small-Outline (DGV),	2B3 🛛 5 16 🖸 1B2				
and Thin Shrink Small-Outline (PW)	1A3 🛛 6 🛛 15 🗍 2A3				
Packages	2B2 🛛 7 🛛 14 🖸 1B3				
-	1A4 🛛 8 13 🗍 2A2				
description	2B1 🛛 9 12 🗋 1B4				
The SN74CBT3244 provides eight bits of	GND [10 11] 2A1				

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

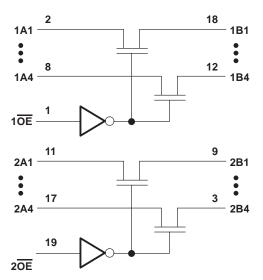
The device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBT3244 is characterized for operation from 0°C to 70 °C.

FUNCTION TABLE (each 4-bit bus switch)

	FUNCTION			
L	A port = B port			
Н	Disconnect			

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range, V _I (see Note 1) Continuous channel current Clamp current, I _K (V _{I/O} < 0) Package thermal impedance, θ_{JA} (see Note 2):	-0.5 V to 7 V -0.5 V to 7 V -0.5 V to 7 V 128 mA -50 mA DB package 70°C/W DBQ package 68°C/W DGV package 92°C/W DW package 58°C/W PW package 83°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TEST CONDITIONS				typ‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	II = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±5	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			50	μΑ
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				3		pF
C _{io(OFF}	=)	V _O = 3 V or 0,	OE = VCC			6		pF
			$V_1 = 0$	l _l = 64 mA		5	7	
ron¶		$V_{CC} = 4.5 V$	VI = 0	I _I = 30 mA		5	7	Ω
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



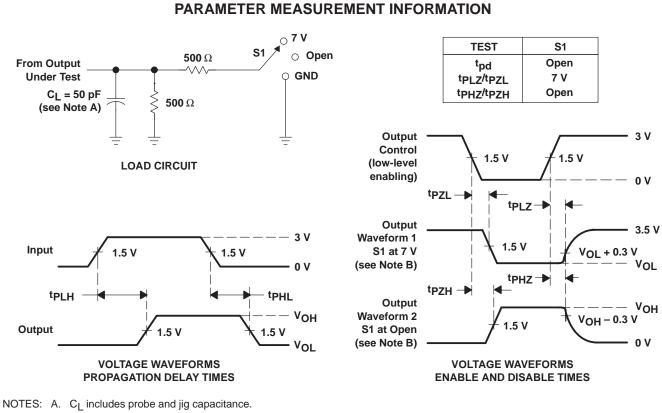
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd} †	A or B	B or A		0.25	ns
t _{en}	ŌE	A or B	1	8.9	ns
^t dis	OE	A or B	1	7.4	ns

[†] This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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SN74CBT3244, Octal FET Bus Switch

Device Status: Active

- > Description
- Features
- > Datasheets
- > Pricing/Samples/Availability
- Application Notes
- Related Documents
- Training

Parameter Name	SN74CBT3244
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
No. of Bits	8
ron(max) (ohms)	7
tpd(max) (ns)	0.25

Description

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Features

- Functionally Equivalent to QS3244
- Standard '244-Type Pinout
- 5- **Ω** Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

To view the following documents, <u>Acrobat Reader 3.x</u> is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: <u>scds001i.pdf</u> (59 KB) Full datasheet in Zipped PostScript: <u>scds001i.psz</u> (59 KB)

Pricing/Samples/Availability

Orderable Device	Package	<u>Pins</u>	Temp (°C)	<u>Status</u>	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN74CBT3244DBLE	<u>DB</u>	20	0 TO 70	OBSOLETE			
SN74CBT3244DBQR	DBQ	20	0 TO 70	ACTIVE	1.00	2500	Check stock or order
SN74CBT3244DBR	DB	20	0 TO 70	ACTIVE	0.84	2000	Check stock or order
SN74CBT3244DGVR	DGV	20	0 TO 70	ACTIVE	1.00	2000	Check stock or order
SN74CBT3244DW	DW	20	0 TO 70	ACTIVE	1.00	25	Check stock or order
SN74CBT3244DWR	DW	20	0 TO 70	ACTIVE	0.87	2000	Check stock or order
SN74CBT3244PWLE	<u>PW</u>	20	0 TO 70	OBSOLETE			
SN74CBT3244PWR	<u>PW</u>	20	0 TO 70	ACTIVE	0.84	2000	Check stock or order

Application Reports

View Application Reports for Digital Logic

- <u>5-V To 3.3-V Translation With The SN74CBTD3384</u> (SCDA003B Updated: 03/01/1997)
- Flexible Voltage-Level Translation With CBT Family Devices (SCDA006 Updated: 07/20/1999)
- Implications Of Slow Or Floating CMOS Inputs (SCBA004C Updated: 02/01/1998)
- Low-Voltage Bus-Switch Technology And Applications (SCDA005 Updated: 12/01/1997)
- Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices (SCEA005 Updated: 12/01/1997)
- <u>SN74CBTS3384 Bus Switches Provide Fast Connection And Ensure Isolation</u> (SCDA002A Updated: 08/01/1996)
- <u>TI Logic Solutions for Memory Interleaving With the Intel440BX Chipset</u> (SCCA001 Updated: 04/08/1999)
- Texas Instruments Crossbar Switches (SCDA001A Updated: 06/01/1995)
- <u>Texas Instruments Solution for Undershoot Protection for Bus Switches</u> (SCDA007 Updated: 04/13/2000)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB Updated: 05/01/1996)

Related Documents

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 284 KB Updated: 07/28/2000)
- More Power In Less Space Technical Article (SCAU001A, 850 KB Updated: 03/01/1996)

Table Data Updated on: 8/31/2000

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