High Speed CMOS 8-bit Bus Interface LatchTransceivers

QS54/74FCT543T
QS54/74FCT544T

QS54/74FCT2543T
QS54/74FCT2544T

FEATURES/BENEFITS

- Pin and function compatible to the 74F543/4 74FCT543/4 and 74FCT543T/4T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 543T/4T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 4.6ns tPD for D
- Iol = 64 mA Com., 48mA Mil.

FCT-T 2543T/4T

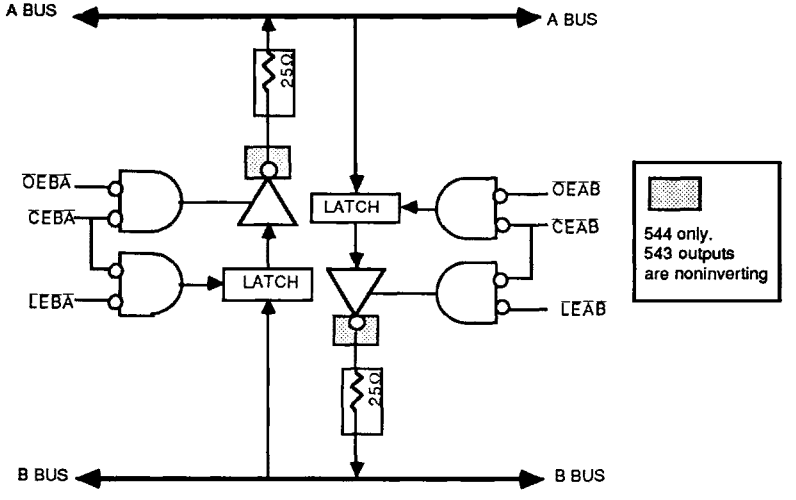
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and C speed grades with 4.6ns tPD for D
- Iol = 12mA Com.

4

DESCRIPTION

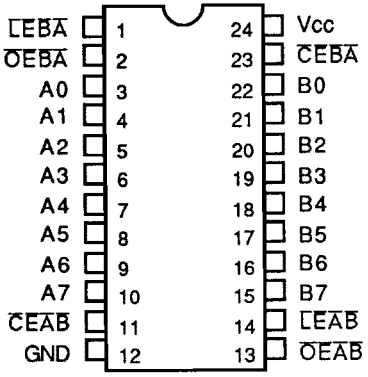
The QSFCT543T/4T and QSFCT543T/4T are 8-bit high-speed CMOS TTL-compatible latched bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2543/4 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2543 series parts can replace the 543 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

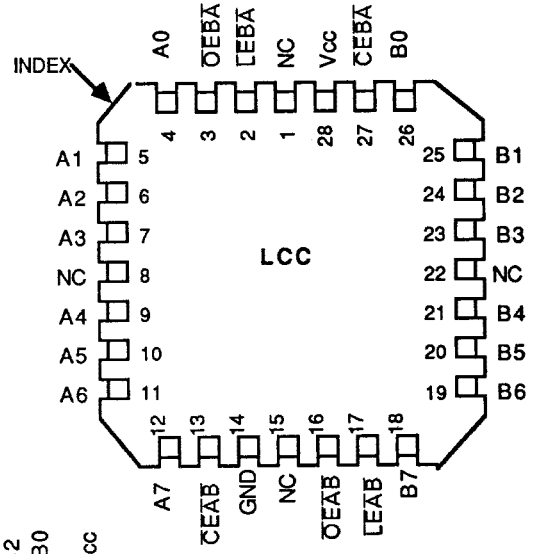
FUNCTIONAL BLOCK DIAGRAM

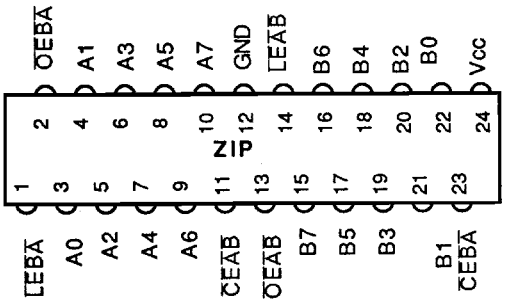


PINOUTS

PDIP, SOIC, QSOP







ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
A1-A8	I/O	A Bus
B1-B8	I/O	B Bus
$\overline{CEAB}$	I	Chip Select, A to B
$\overline{CEBA}$	I	Chip Select, B to A
$\overline{LEAB}$	I	Latch Enable, A to B
$\overline{LEBA}$	I	Latch Enable, B to A
$\overline{OEAB}$	I	Output Enable, A to B
$\overline{OEBA}$	I	Output Enable, B to A

FUNCTION TABLES - QSFCT543/4, 2543/4

Inputs						Outputs		Function	
$\overline{CEAB}$	$\overline{CEBA}$	$\overline{LEAB}$	$\overline{LEBA}$	$\overline{OEAB}$	$\overline{OEBA}$	A1-8	B1-8	543/2543	544/2544
H	H	-	-	-	-	Z	Z	Disabled, Hold	Disabled, Hold
-	-	-	-	H	H	Z	Z	Disabled	Disabled
-	-	H	H	-	-	NC	NC	Hold	Hold
-	-	L	H	-	-	-	-	A->B Latch Open	A->B Latch Open
-	-	H	L	-	-	-	-	B->A Latch Open	B->A Latch Open
-	-	-	-	L	H	-	-	A Latch -> B Bus	A Latch->$\overline{B}$ Bus
-	-	-	-	H	L	-	-	B Latch -> A Bus	B Latch ->$\overline{A}$ Bus

H = HIGH
L = LOW
NC = No Change
Z = High Impedance
- = Don't care

4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
---------	4	4	5	7	pF
---------	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX (25Ω)	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Parameter		543/4T, 2543/4T		543/4AT, 2543/4AT		543/4CT, 2543/4CT		543/4DT, 2543/4DT		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPHLB, tPLHB	Bus to Bus delaY,(Transparent) (1)	Com	2.5	8.5	2.5	6.5	2.5	5.5	2	4.6	ns
		Mil	2.5	10	2.5	7.5					
tPHLL, tPLHL	Latch enable to data delay (1)	Com	2.5	12.5	2.5	8	2.5	7	2.5	5.3	
		Mil	2.5	14	2.5	9					
tPZH, tPZL	Output enable time (1)	Com	2	12	2	9	2	8	1.5	6.2	
		Mil	2	14	2	10					
tPLZ, tPHZ (2)	Output disable time (2)	Com	2	9	2	7.5	2	6.5	2	6	
		Mil	2	13	2	8.5					
tS	Setup time bus to $\overline{CE}$	Com	3		2		2		2		
		Mil	3		2		2		2		
tH	Hold time bus to $\overline{CE}$	Com	2		2		2		2		
		Mil	2		2		2		2		
tW	Pulse width low $\overline{CE}$	Com	5		5		5		5		
		Mil	5		5		5		5		

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.

4