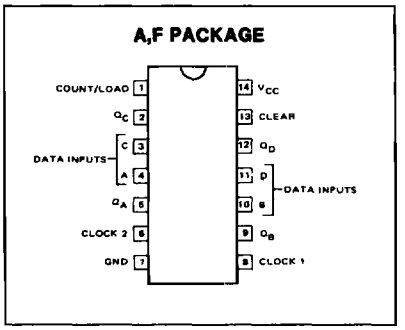
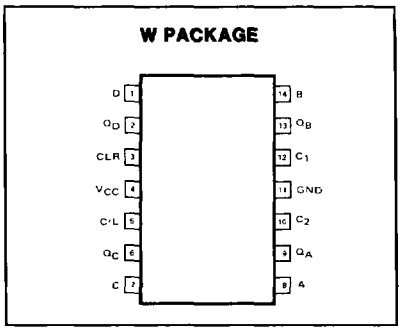
SPEED/PACKAGE AVAILABILITY

54	F,W	74	A
54LS	F,W	74LS	A
54S	F,W	74S	A

PIN CONFIGURATION





DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter S54/N74LS196. This counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

*During the count operation, transfer of information to the outputs occurs on the negative-*going edge of the clock pulse. This counter features a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

(54/74—Refer to 8290 Data Sheet, 54/74S—Refer to 82S90 Data Sheet)

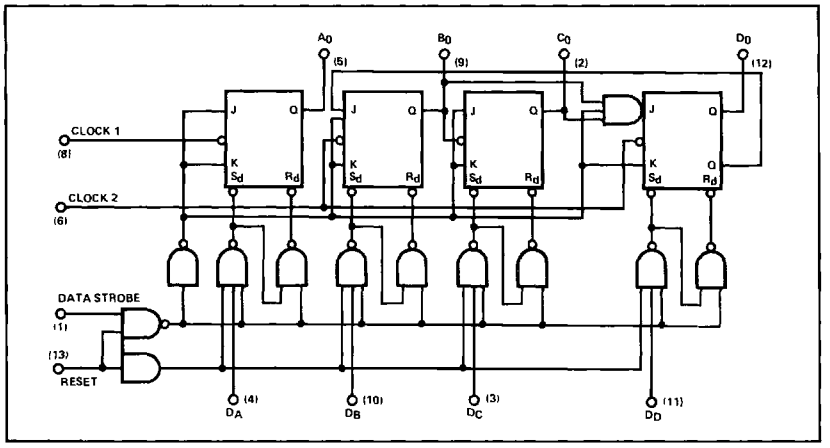
PARAMETER[1]		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	54/74LS MIN	54/74LS TYP	54/74LS MAX	UNIT
f_{Clock}		Clock 1	Q_A		30	40		MHz
		Clock 2	Q_A		15			
t_w	Input pulse-width				20			
		Clock 1			30			ns
		Clock 2						
		Clear			15			
		Load			20			
t_{Hold}	*Input hold time*							
		High level			$t_{w(Load)}\downarrow$			
		Low level			$t_{w(Load)}\downarrow$			
t_{Setup}	Input setup time							
		High level			10↓			ns
		Low level			15↓			ns
t_{Enable} (Note 1)	Count enable time				20↓			ns
				C_L = 15pF				
t_{PLH}		Clock 1	Q_A	R_L = 2kΩ		8	15	
t_{PHL}						13	20	ns
t_{PLH}		Clock 2	Q_B			16	24	
t_{PHL}						22	33	ns
t_{PLH}		Clock 2	Q_C			38	57	
t_{PHL}						41	62	ns
t_{PLH}		Clock 2	Q_D			12	18	
t_{PHL}						30	45	ns
t_{PLH}		A,B,C,D	Q_A, Q_B, Q_C, Q_D			20	30	
t_{PHL}						29	44	ns
t_{PLH}		Load	Any			27	41	
t_{PHL}						30	45	ns
t_{PHL}		Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

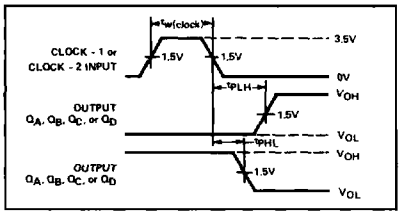
NOTE:

1. Count enable time is the internal immediately preceding the negative – going edge of the clock pulse during which internal the count/load and clear inputs must be high to ensure counting.

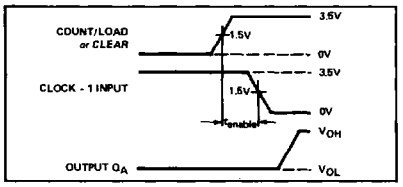
LOGIC DIAGRAM



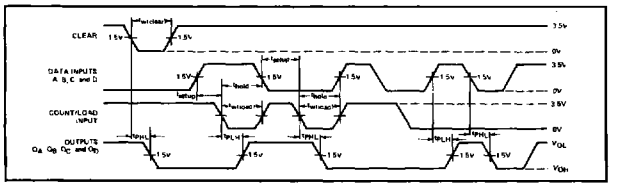
PARAMETER MEASUREMENT INFORMATION



CLOCK-MODE VOLTAGE WAVEFORMS



CLOCK ENABLE TIME VOLTAGE WAVEFORMS



CLEAR AND LOAD VOLTAGE WAVEFORMS

NOTES:

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, and unless specified, t_f ≤ 15 ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Unless otherwise specified, Q_A is connected to clock 2.

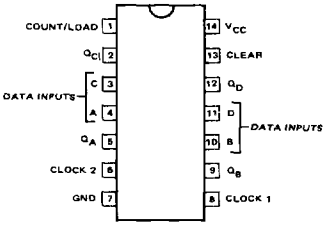
LOGIC

SPEED/PACKAGE AVAILABILITY

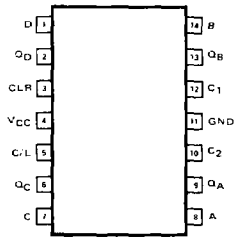
54	F,W	74	A
54LS	F,W	74LS	A
		74S	A

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter S54/N74LS197. These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

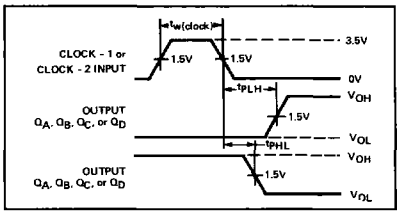
These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

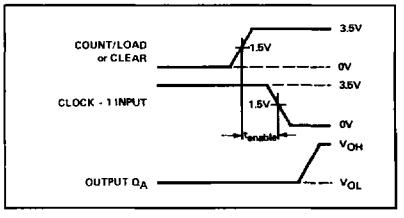
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	Clock 1	Q_A	C_L = 15pF, R_L = 2kΩ	30	40		MHz
	Clock 2	Q_A		15			
t_{PLH}	Clock 1	Q_A			8	15	ns
t_{PHL}					14	21	
t_{PLH}	Clock 2	Q_B			12	19	ns
t_{PHL}					23	35	
t_{PLH}	Clock 2	Q_C			34	51	ns
t_{PHL}					42	63	
t_{PLH}	Clock 2	Q_D			55	78	ns
t_{PHL}					63	95	
t_{PLH}	A,B,C,D	Q_A, Q_B, Q_C, Q_D			18	27	ns
t_{PHL}					29	44	
t_{PLH}	Load	Any			26	39	ns
t_{PHL}					30	45	
t_{PHL}	Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency
t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

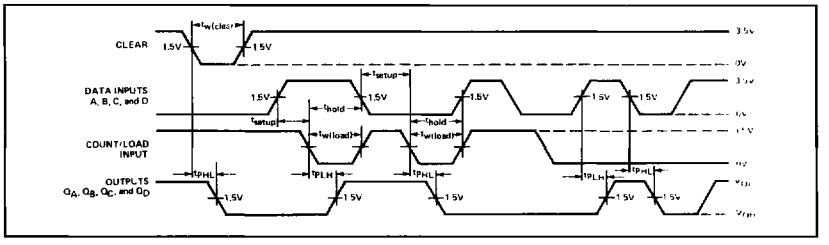
PARAMETER MEASUREMENT INFORMATION



CLOCK MODE

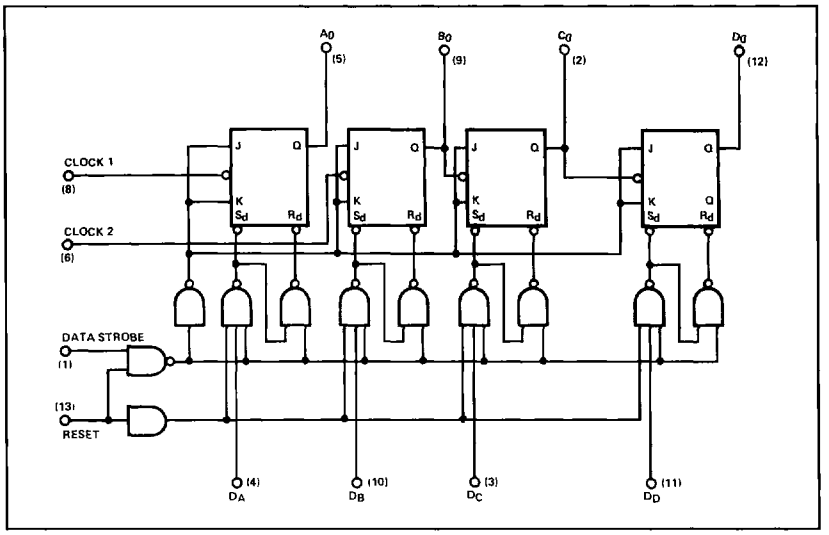


CLOCK ENABLE



CLEAR AND LOAD

LOGIC DIAGRAM



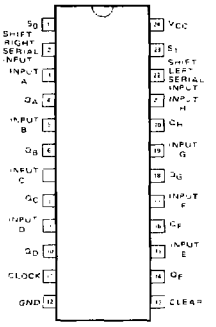
LOGIC

SPEED/PACKAGE AVAILABILITY

54 F,Q 74 N

PIN CONFIGURATION

F,N,Q PACKAGE



TRUTH TABLE

INPUTS							OUTPUTS				
	MODE			SERIAL		PARALLEL					
CLEAR	S_1	S_0	CLOCK	LEFT	RIGHT	A...H	Q_A	Q_B	...	Q_G	Q_H
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a...h	a	b		g	h
H	L	H	↑	X	H	X	H	Q_{An}		Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}		Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}

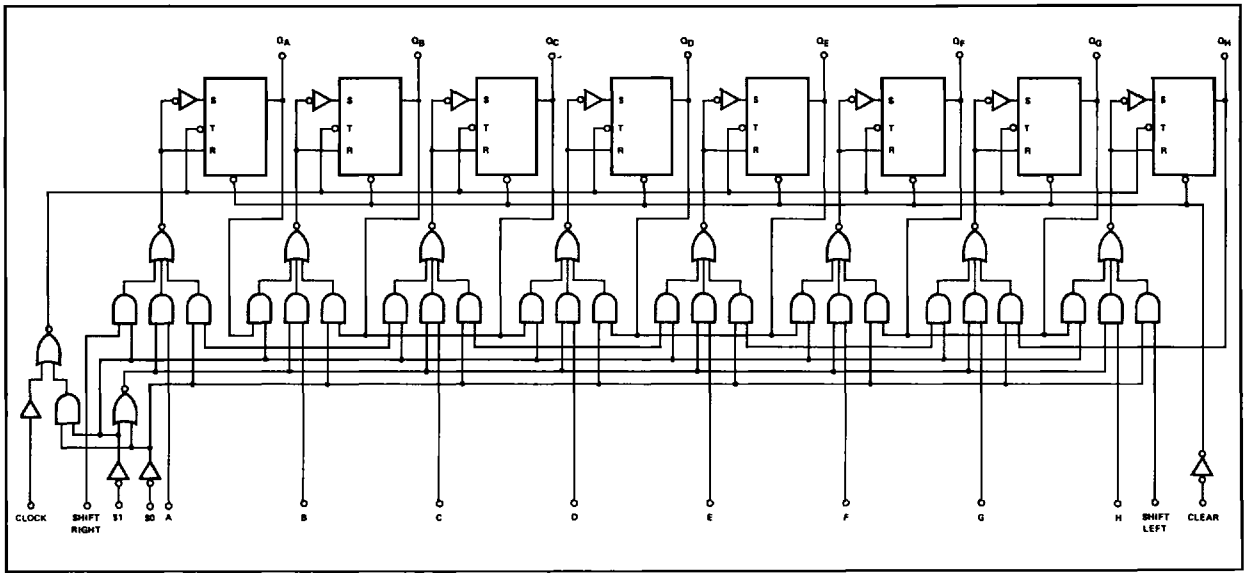
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

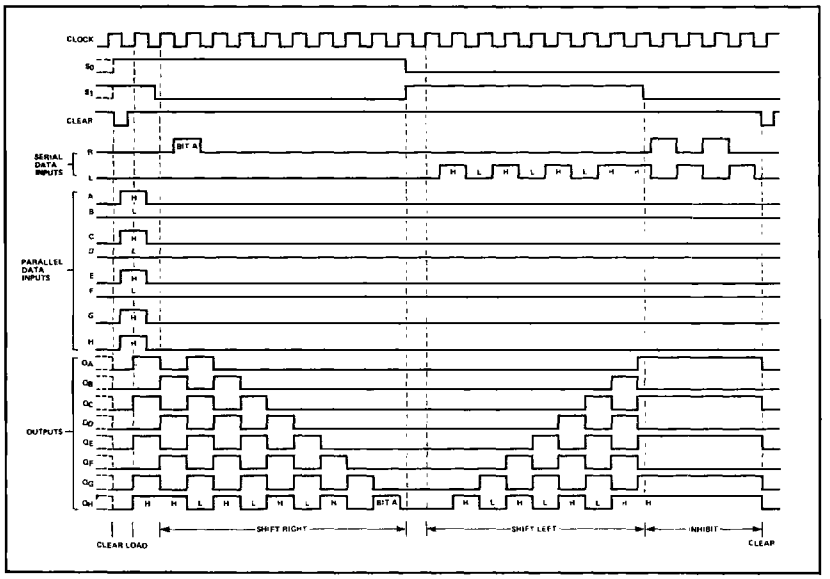
TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			25	35		MHz
t_w	Width of pulse			20			ns
t_{Setup}	Input setup time			30			
	Mode control						
	Data			20			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Clock		8	17	26	ns
t_{PLH}	High-to-low			8	20	30	
t_{PHL}	High-to-low	Clear			23	35	

Load circuit and typical waveforms are shown at the front of section.

BLOCK DIAGRAM



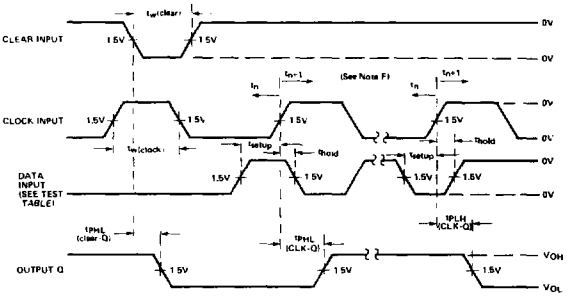
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT & CLEAR SEQUENCES



PARAMETER MEASUREMENT INFORMATION

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_n+1
B	4.5V	4.5V	Q_B at t_n+1
C	4.5V	4.5V	Q_C at t_n+1
D	4.5V	4.5V	Q_D at t_n+1
E	4.5V	4.5V	Q_E at t_n+1
F	4.5V	4.5V	Q_F at t_n+1
G	4.5V	4.5V	Q_G at t_n+1
H	4.5V	4.5V	Q_H at t_n+1
L Serial Input	4.5V	0V	Q_A at t_n+8
R Serial Input	0V	4.5V	Q_H at t_n+8



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional text.
   t_n+1 = *bit time after one clocking transition*
   t_n+8 = bit time after eight clocking transitions
Load circuit shown at front of section.