SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

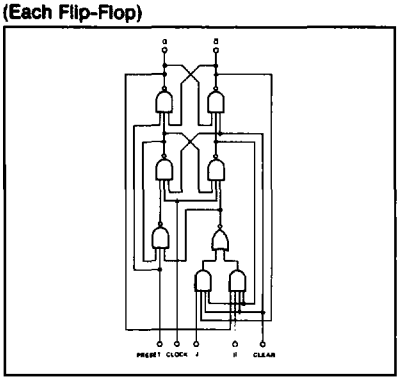
DESCRIPTION

A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

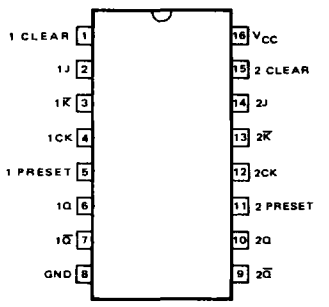
FUNCTIONAL BLOCK DIAGRAM

(Each Flip-Flop)



PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: each output changes to the complement of its previous level on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	33		25	33		MHz
$t_{w\ (Clock)}$	Width of clock pulse			20			25			ns
$t_{w\ (Preset)}$	Width of preset pulse			20			25			ns
$t_{w\ (CLear)}$	Width of clear pulse			20			25			ns
t_{Setup}	Input setup time			10↑			20↑			ns
t_{Hold}	Input hold time			6↑			5↑			ns
Propagation delay time										
t_{PLH}	Low-to-high	Clock	Q,$\overline{Q}$	4	10	16				ns
t_{PHL}	High-to-low			9	18	28				
t_{PLH}	Low-to-high	Preset	Q		10	15				
t_{PHL}	High-to-low	Preset	$\overline{Q}$		23	35				
t_{PLH}	Low-to-high	Clear	$\overline{Q}$		10	15				
t_{PHL}	High-to-low	Clear	Q		17	25				
t_{PLH}	Low-to-high	CLR, PRE or CLK (as appropriate)						8	25	
t_{PHL}	High-to-low							16	40	

Load circuit and typical waveforms are shown at the front of section.

LOGIC

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP 54/74112

(Separate clock, preset and clear inputs)

SPEED/PACKAGE AVAILABILITY

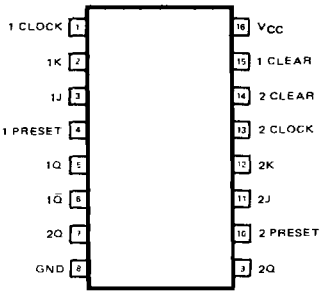
54LS F,W 74LS B,F
54S F,W 74S B,F

DESCRIPTION

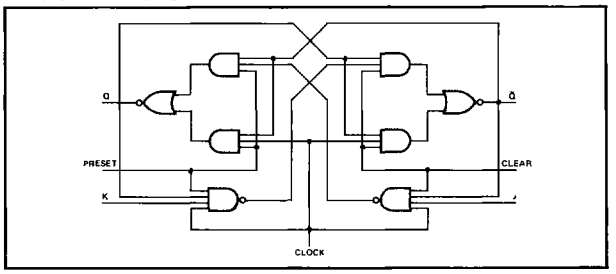
The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

B,F,W PACKAGE



BLOCK DIAGRAM



FUNCTIONAL TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			30	45		80	125		MHz
$t_{w(Clock)}$ Width of clock pulse			20						ns
Clock high						6			
Clock low						6.5			
$t_{w(Preset)}$ Width of preset pulse			25			8			ns
$t_{w(Clear)}$ Width of clear pulse			25			8			ns
t_{Setup} Input setup time			20↓			3↓			ns
t_{Hold} Input hold time			0↓			0↓			ns
Propagation delay time									
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)			11	20	2	4	7	ns
t_{PHL} High-to-low				15	30	2	5	7	

Load circuit and typical waveforms are shown at the front of section.