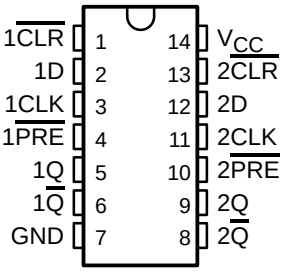
- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 10 ns at 5 V**

description/ordering information

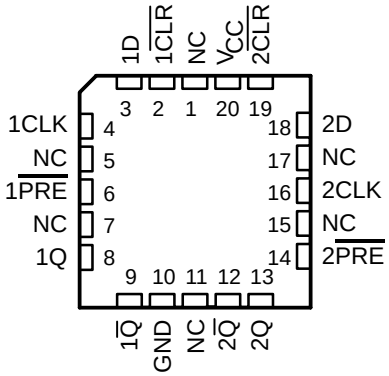
The 'AC74 devices are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

SN54AC74 . . . J OR W PACKAGE
SN74AC74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AC74N	SN74AC74N
	SOIC – D	Tube	SN74AC74D	AC74
		Tape and reel	SN74AC74DR	
	SOP – NS	Tape and reel	SN74AC74NSR	AC74
	SSOP – DB	Tape and reel	SN74AC74DBR	AC74
	TSSOP – PW	Tape and reel	SN74AC74PWR	AC74
–55°C to 125°C	CDIP – J	Tube	SNJ54AC74J	SNJ54AC74J
	CFP – W	Tube	SNJ54AC74W	SNJ54AC74W
	LCCC – FK	Tube	SNJ54AC74FK	SNJ54AC74FK

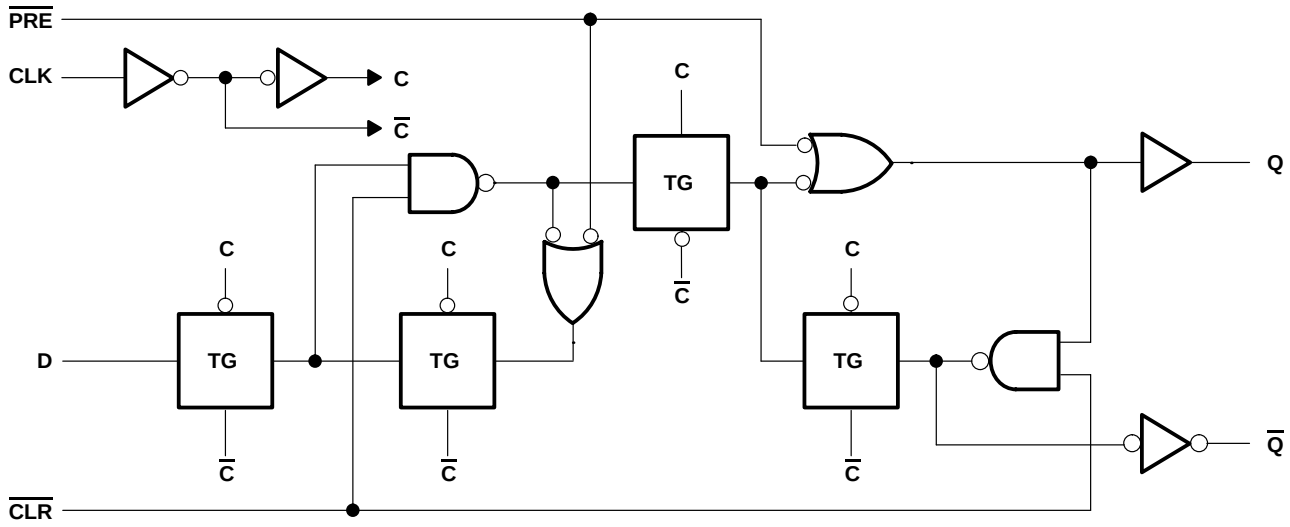
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is unstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5 V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		–12		–12	mA
		V_{CC} = 4.5 V		–24		–24	
		V_{CC} = 5.5 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AC74		SN74AC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	3 V	2.9	4.49		2.9		2.9		V
			4.5 V	4.4	5.49		4.4		4.4		
			5.5 V	5.4	5.49		5.4		5.4		
		I_{OH} = –12 mA	3 V	2.56			2.4		2.46		
		I_{OH} = –24 mA	4.5 V	3.86			3.7		3.76		
			5.5 V	4.86			4.7		4.76		
		I_{OH} = –50 mA†	5.5 V				3.85				
		I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			5.5 V		0.001	0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Data pins	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
	Control pins					±0.1		±1		±1	
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		40		20	μA
C_i		$V_I = V_{CC}$ or GND	5 V		3						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.5		8		7		ns
		CLK	5.5		8		7		
t_{su}	Setup time, data before CLK↑	Data	4		5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	140	0	140	0	140	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5		5.5		5		ns
		CLK	4.5		5.5		5		
t_{su}	Setup time, data before CLK↑	Data	3		4		3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.5	8	12	1	13	2.5	13	ns
t_{PHL}			4	10.5	12	1	14	3.5	13.5	
t_{PLH}	CLK	Q or $\overline{Q}$	4.5	8	13.5	1	17.5	4	16	ns
t_{PHL}			3.5	8	14	1	13.5	3.5	14.5	

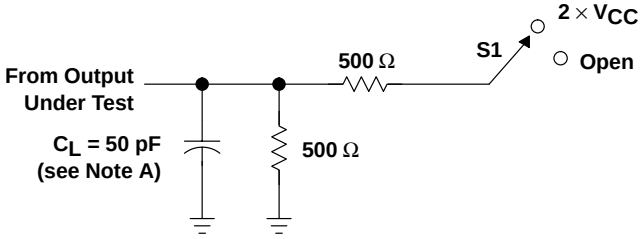
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.5	6	9	1	9.5	2	10	ns
t_{PHL}			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	6	10	1	12	3	10.5	ns
t_{PHL}			2.5	6	10	1	10	2.5	10.5	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

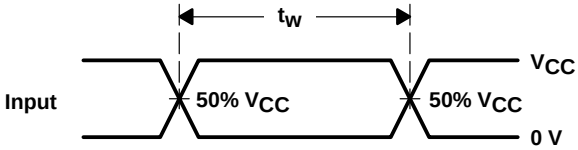
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	45	pF

PARAMETER MEASUREMENT INFORMATION

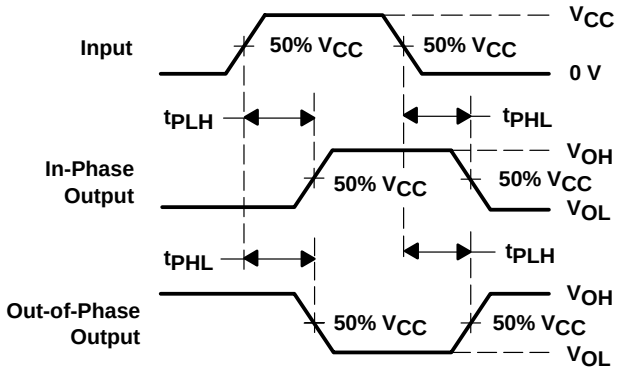


TEST	S1
t_{PLH}/t_{PHL}	Open

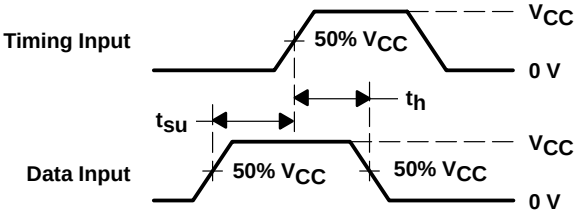
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

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Dallas, Texas 75265

SN74AC74, Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54AC74	SN74AC74
Voltage Nodes (V)	5, 3.3	5, 3.3
Vcc range (V)	2.0 to 6.0	2.0 to 6.0
Input Level	CMOS	CMOS
Output Level	CMOS	CMOS
Output Drive (mA)		-24/24
Output	3S	3S
No. of Bits	2	2
Static Current		0.02
th (ns)		0.5
tpd max (ns)		10.5
tsu (ns)		3

FEATURES

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- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 10 ns at 5 V

DESCRIPTION

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The ’AC74 devices are dual positive-edge-triggered D-type flip-flops.

A low level at the preset (PRE)\ or clear (CLR)\ input sets or resets the outputs, regardless of the levels of the other inputs. When PRE\ and CLR\ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74ac74.pdf (103 KB,Rev.D) (Updated: 09/19/2002)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74AC74D	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74AC74DBR	SSOP (DB)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74AC74DR	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74AC74N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74AC74PWR	TSSOP (PW)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74AC74D	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.20	50	N/A*		8 WKS	Avnet | AMERICA	>1k	BUY NOW
										DigiKey | AMERICA	707	BUY NOW
SN74AC74DBLE	OBSOLETE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74AC74DBR	ACTIVE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU | 0.20	2000	N/A*	4000 | 03 Oct	8 WKS			
SN74AC74DR	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.20	2500	N/A*		8 WKS	DigiKey | AMERICA	>1k	BUY NOW
SN74AC74N	ACTIVE	PDIP (N) | 14	-40 TO 85	View Contents	1KU | 0.20	25	N/A*		6 WKS	Avnet | AMERICA	448	BUY NOW
										DigiKey | AMERICA	336	BUY NOW
SN74AC74NSR	ACTIVE	SOP (NS) | 14		View Contents	1KU | 0.24	2000	N/A*		8 WKS			

SN74AC74PWLE	OBSOLETE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74AC74PWR	ACTIVE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU | 0.20	2000	N/A*		8 WKS	DigiKey | AMERICA	>1k	BUY NOW

Table Data Updated on: 9/26/2002