

## IS63C1024

### 128K x 8 HIGH-SPEED CMOS STATIC RAM 5V REVOLUTIONARY PINOUT

ADVANCE INFORMATION  
FEBRUARY 1999

#### FEATURES

- High-speed access times:  
10, 12 and 15 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- $\overline{CE}$  power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- 2V data retention (optional)
- Packages available:
  - 32-pin 300-mil SOJ
  - 32-PIN 400-mil SOJ
  - 32-pin TSOP (Type 2)

#### DESCRIPTION

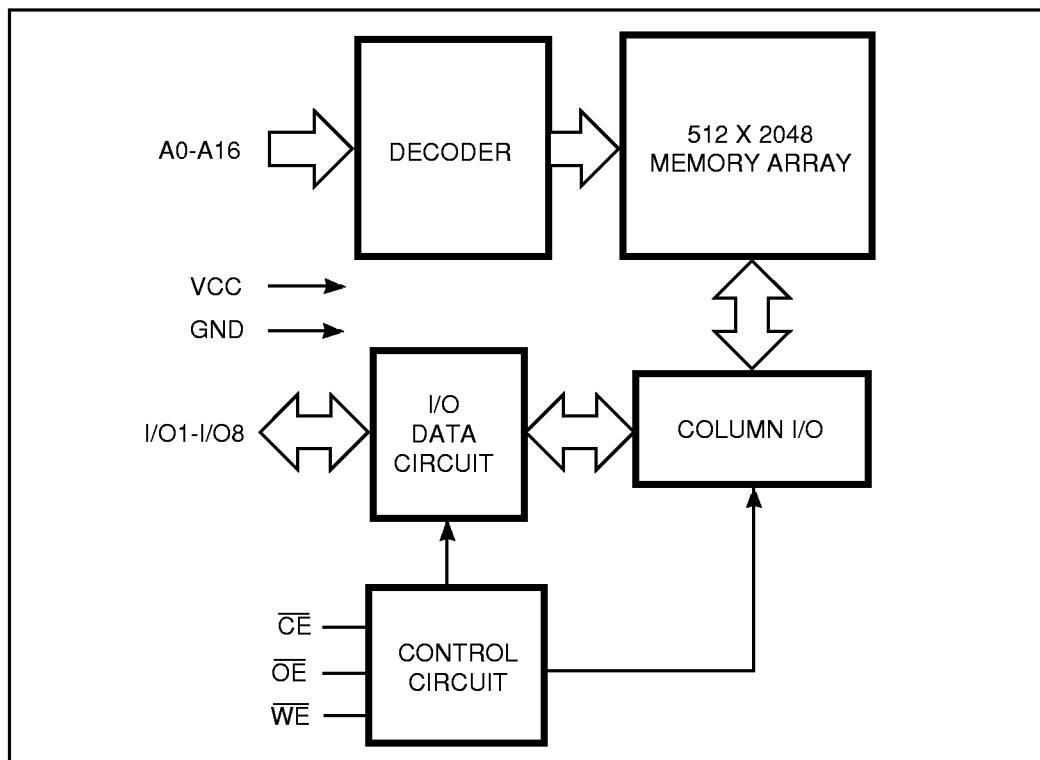
The *ISSI* IS63C1024 is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The IS63C1024 is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

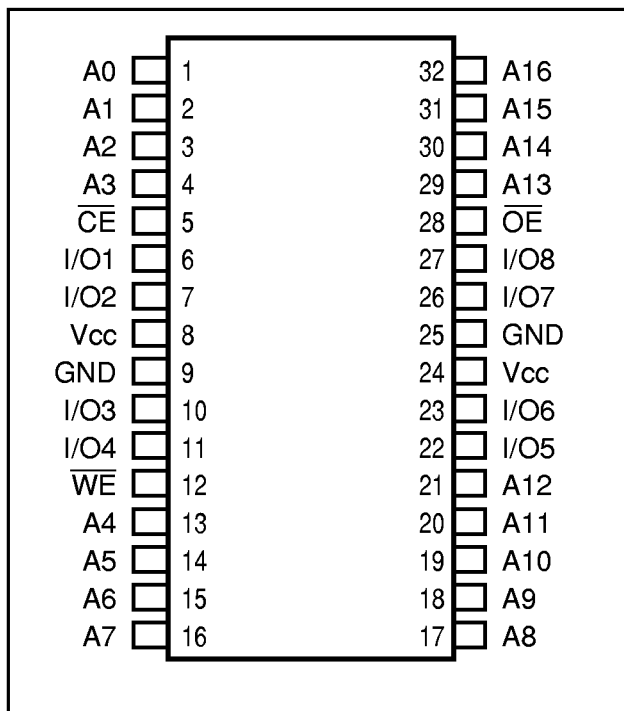
The IS63C1024 operates from a single 5V power supply and all inputs are TTL-compatible.

The IS63C1024 is available in 32-pin 300-mil SOJ, 400-mil SOJ, and TSOP (Type II) packages.

#### FUNCTIONAL BLOCK DIAGRAM



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**PIN CONFIGURATION****32-Pin SOJ and TSOP (Type II)****PIN DESCRIPTIONS**

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O1-I/O8	Bidirectional Ports
Vcc	Power
GND	Ground

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA		2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>			-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Com. Ind.	-1 -5	1 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled	Com. Ind.	-1 -5	1 5	μA

## Notes:

1. V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns		-12 ns		-15 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE}$ = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = Max.	Com.	—	100	—	90	—	80	mA
			Ind.	—	110	—	100	—	90	
I <sub>CC2</sub>	Static Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE}$ = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	60	—	60	—	60	mA
			Ind.	—	70	—	70	—	70	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	15	—	15	—	15	mA
			Ind.	—	25	—	25	—	25	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CE} \leq V_{CC} - 0.2V$ , V <sub>IN</sub> > V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	2	—	2	—	2	mA
			Ind.	—	5	—	5	—	5	

## Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

## Notes:

1. Tested initially and after any design or process changes that may affect these parameters.  
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	10	—	12	—	15	—	ns
$t_{AA}$	Address Access Time	—	10	—	12	—	15	ns
$t_{OHA}$	Output Hold Time	3	—	3	—	3	—	ns
$t_{ACE}$	$\overline{CE}$ Access Time	—	10	—	12	—	15	ns
$t_{DOE}$	$\overline{OE}$ Access Time	—	5	—	6	—	7	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	5	0	6	0	7	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	5	0	6	0	7	ns
$t_{PU}$	Power Up Time	0	—	0	—	0	—	ns
$t_{PD}$	Power Down Time	—	10	—	12	—	15	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

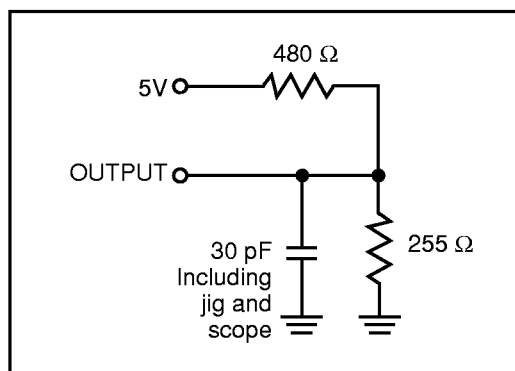
**AC TEST LOADS**

Figure 1.

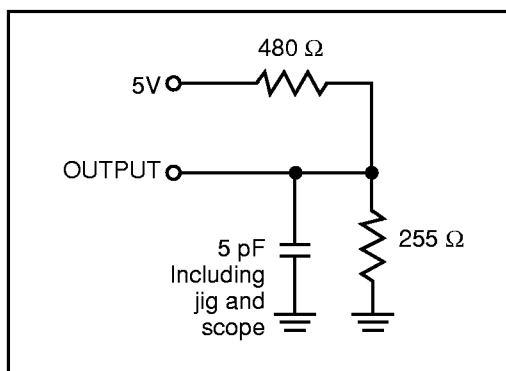
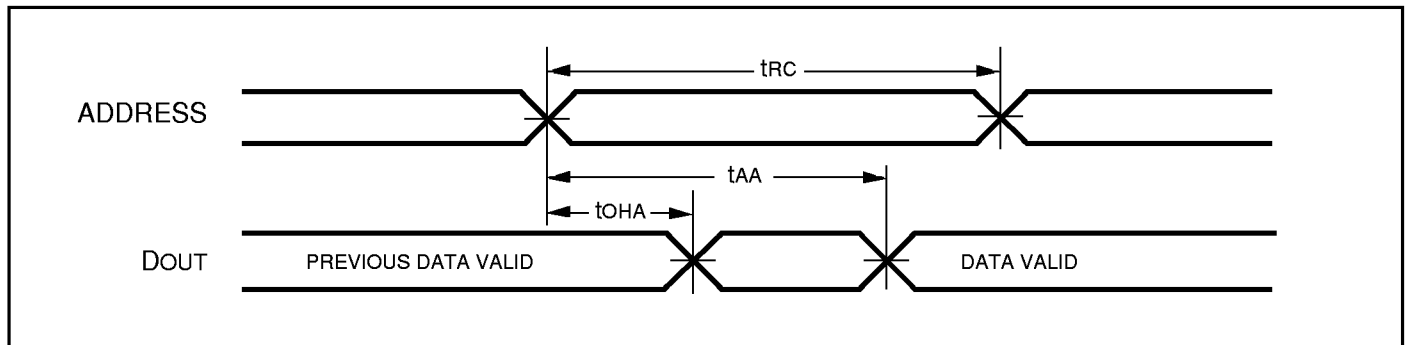
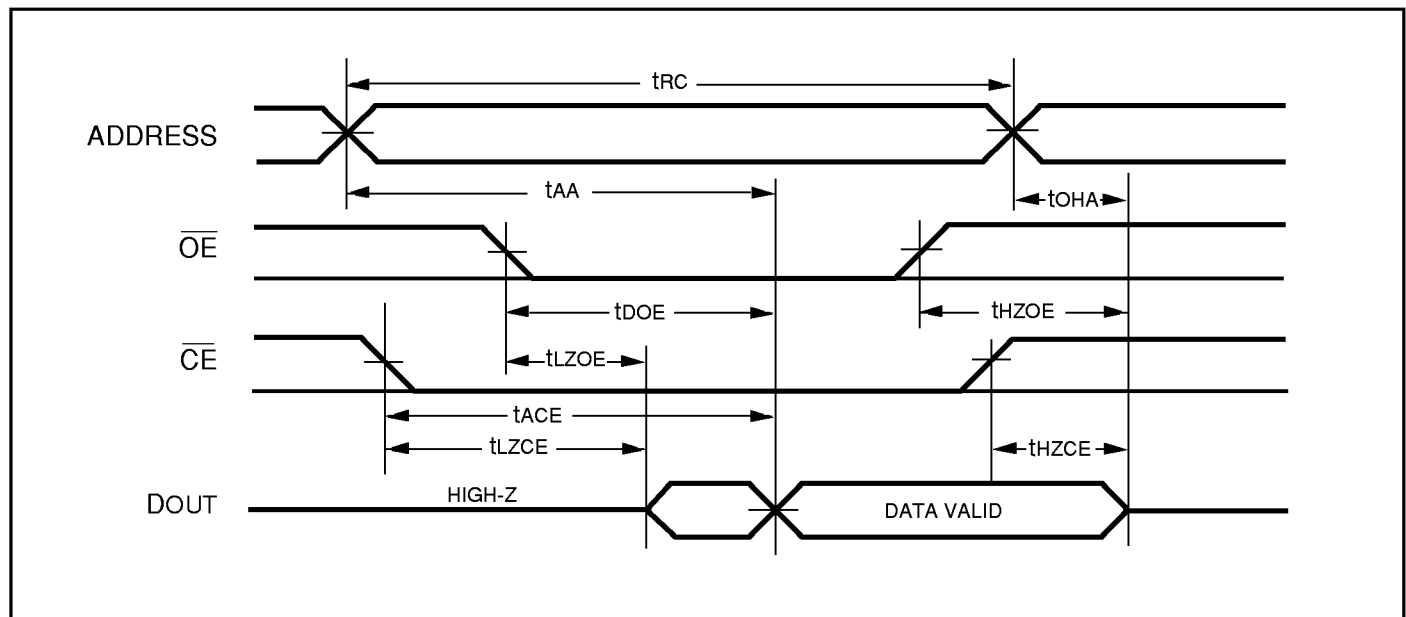


Figure 2.

## AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>READ CYCLE NO. 2<sup>(1,3)</sup>**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range)

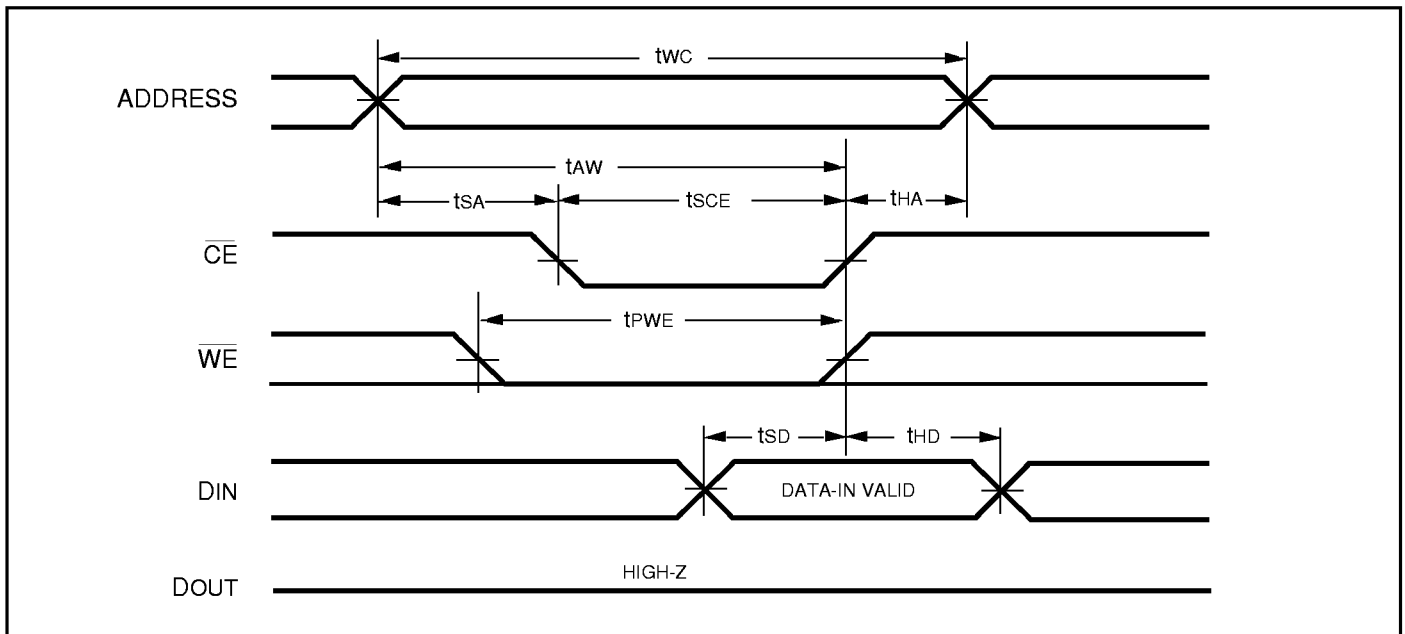
Symbol	Parameter	-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	10	—	12	—	15	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	8	—	9	—	10	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	8	—	9	—	10	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = High)	8	—	9	—	10	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = Low)	10	—	12	—	15	—	ns
t <sub>SD</sub>	Data Setup to Write End	6	—	6	—	7	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE<sup>(2)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	0	5	0	6	0	7	ns
t <sub>LZWE<sup>(2)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	ns

**Notes:**

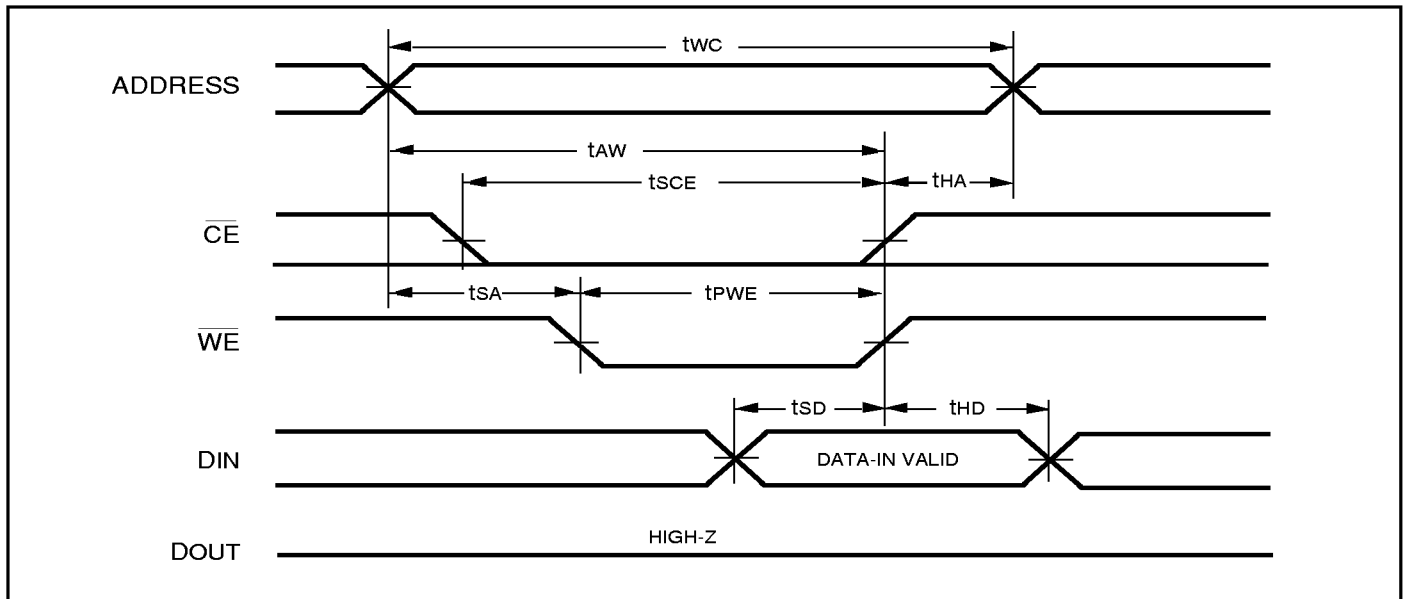
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**



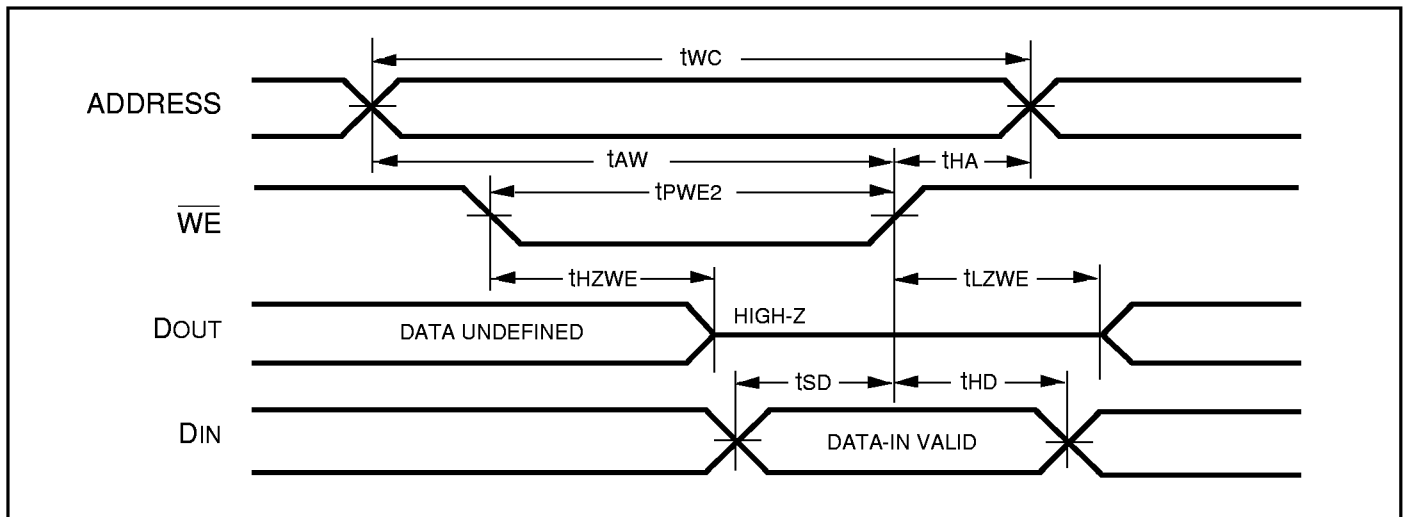
**WRITE CYCLE NO. 2 ( $\overline{CE}$  Controlled)<sup>(1,2)</sup>**



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

**WRITE CYCLE NO. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  is LOW,  $\overline{CE}$  is LOW,  $\overline{WE}$  Terminates Write)**



**ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
10	IS63C1024-10T	TSOP (Type II)
10	IS63C1024-10J	300-mil Plastic SOJ
10	IS63C1024-10K	400-mil Plastic SOJ
12	IS63C1024-12T	TSOP (Type II)
12	IS63C1024-12J	300-mil Plastic SOJ
12	IS63C1024-12K	400-mil Plastic SOJ
15	IS63C1024-15T	TSOP (Type II)
15	IS63C1024-15J	300-mil Plastic SOJ
15	IS63C1024-15K	400-mil Plastic SOJ

**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
10	IS63C1024-10TI	TSOP (Type II)
10	IS63C1024-10JI	300-mil Plastic SOJ
10	IS63C1024-10KI	400-mil Plastic SOJ
12	IS63C1024-12TI	TSOP (Type II)
12	IS63C1024-12JI	300-mil Plastic SOJ
12	IS63C1024-12KI	400-mil Plastic SOJ
15	IS63C1024-15TI	TSOP (Type II)
15	IS63C1024-15JI	300-mil Plastic SOJ
15	IS63C1024-15KI	400-mil Plastic SOJ

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