National Semiconductor

December 1994

54F/74F821
10-Bit D-Type Flip-Flop

General Description

The 'F821 is a 10-bit D-type flip-flop with TRI-STATE® true outputs arranged in a broadside pinout. The 'F821 is functionally and pin compatible with the AMD's Am29821.

Features

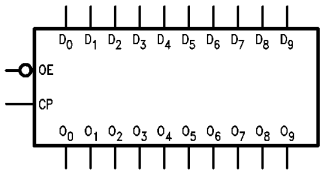
- TRI-STATE Outputs
- Direct replacement for AMD's Am29821

Commercial	Military	Package Number	Package Description
74F821SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F821SDM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F821SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
	54F821FM (Note 2)	W24C	24-Lead Cerpack
	54F821LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

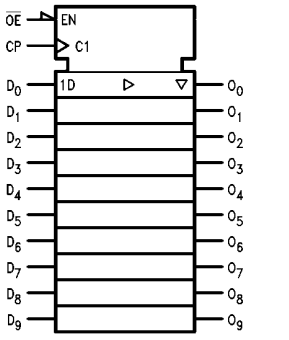
Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

Logic Symbols



TL/F/9595–1

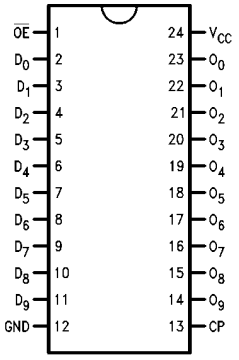
IEEE/IEC



TL/F/9595–5

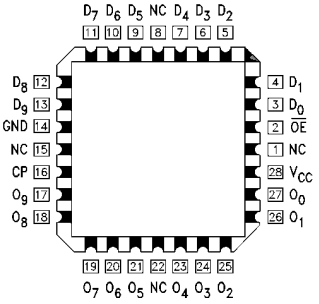
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9595–2

Pin Assignment for LCC



TL/F/9595–3

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RRD-B30M75/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_9	Data Inputs	1.0/1.0	20 μA/$-$0.6 mA
$\overline{OE}$	Output Enable TRI-STATE Input	1.0/1.0	20 μA/$-$0.6 mA
CP	Clock Input	1.0/1.0	20 μA/$-$0.6 mA
O_0-O_9	TRI-STATE Outputs	150/40 (33.3)	$-$3.0 mA/24 mA (20 mA)

Functional Description

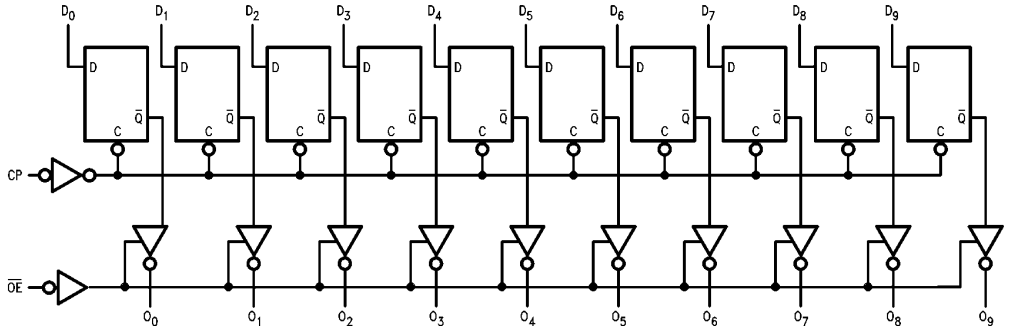
The 'F821 consists of ten D-type edge-triggered flip-flops. This device has TRI-STATE true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the content of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	CP	D	$\overline{Q}$	O	
H	H	X	NC	Z	Hold
H	L	X	NC	Z	Hold
H	⌐⌐	L	H	Z	Load
H	⌐⌐	H	L	Z	Load
L	⌐⌐	L	H	L	Data Available
L	⌐⌐	H	L	H	Data Available
L	H	X	NC	NC	No Change in Data
L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
⌐⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/9595–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCZ}	Power Supply Current			78	100	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

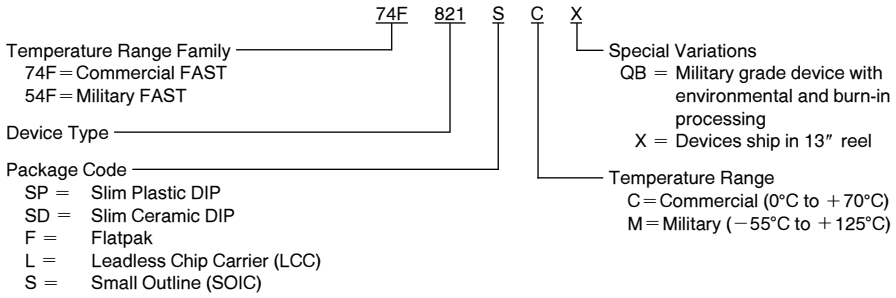
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	150		60		70		MHz
t_{PLH}	Propagation Delay	2.0	6.4	9.5	2.0	10.5	2.0	10.5	ns
t_{PHL}	CP to O_n	2.0	6.2	9.5	2.0	10.5	2.0	10.5	
t_{PZH}	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns
t_{PZL}	$\overline{OE}$ to O_n	2.0	6.3	10.5	2.0	13.0	2.0	11.5	
t_{PHZ}	Output Disable Time	1.5	3.4	7.0	1.0	7.5	1.5	7.5	
t_{PLZ}	$\overline{OE}$ to O_n	1.5	3.5	7.0	1.0	7.5	1.5	7.5	

AC Operating Requirements

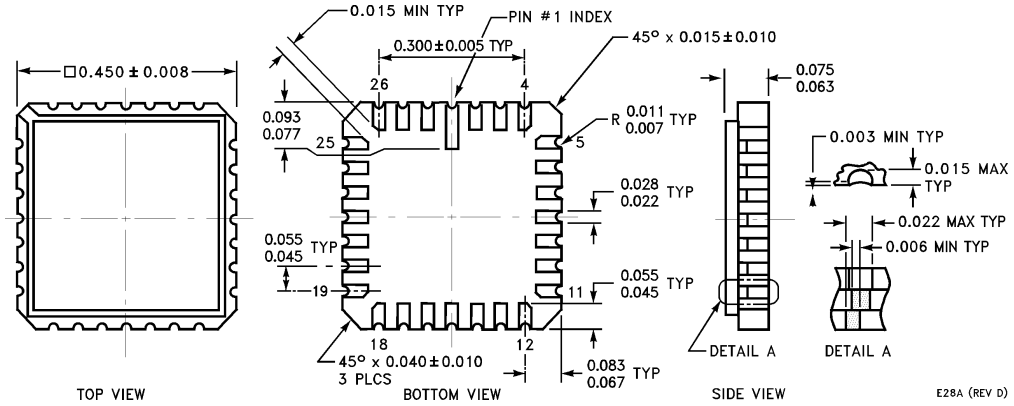
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
$t_s(L)$	D_n to CP	2.5		4.0		3.0		
$t_h(H)$	Hold Time, HIGH or LOW	2.5		2.5		2.5		
$t_h(L)$	D_n to CP	2.5		2.5		2.5		
$t_w(H)$	CP Pulse Width	5.0		6.0		6.0		ns
$t_w(L)$	HIGH or LOW	5.0		6.0		6.0		

Ordering Information

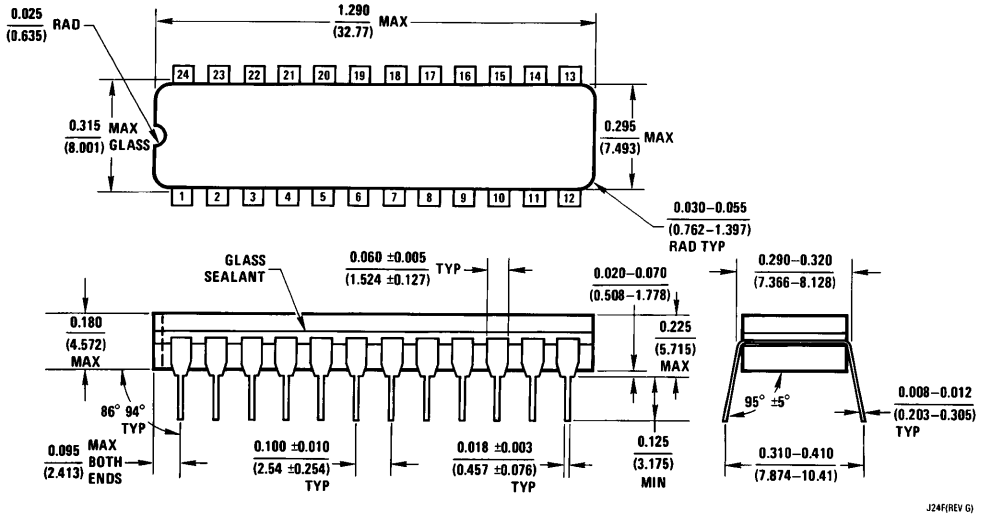
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

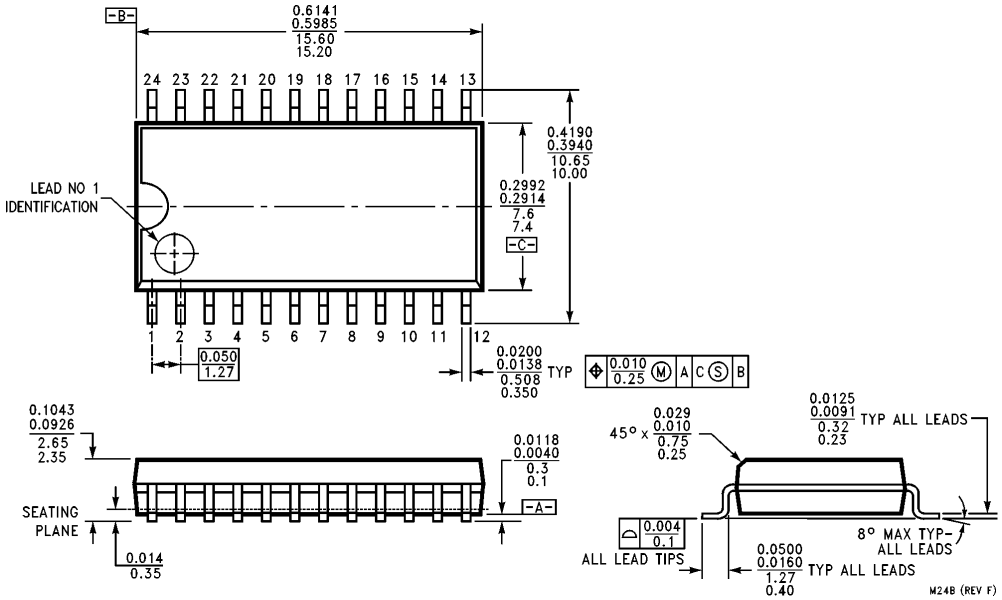


28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

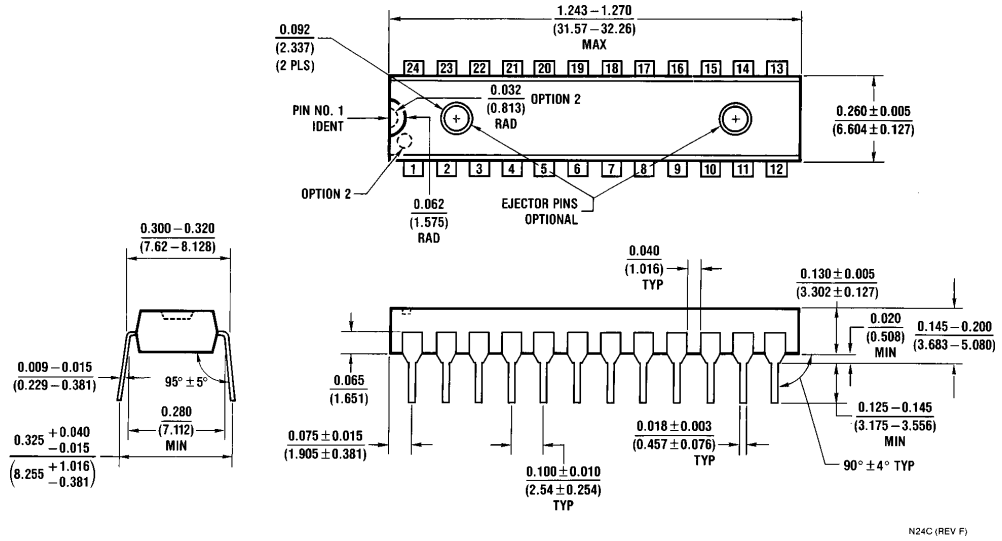


24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)

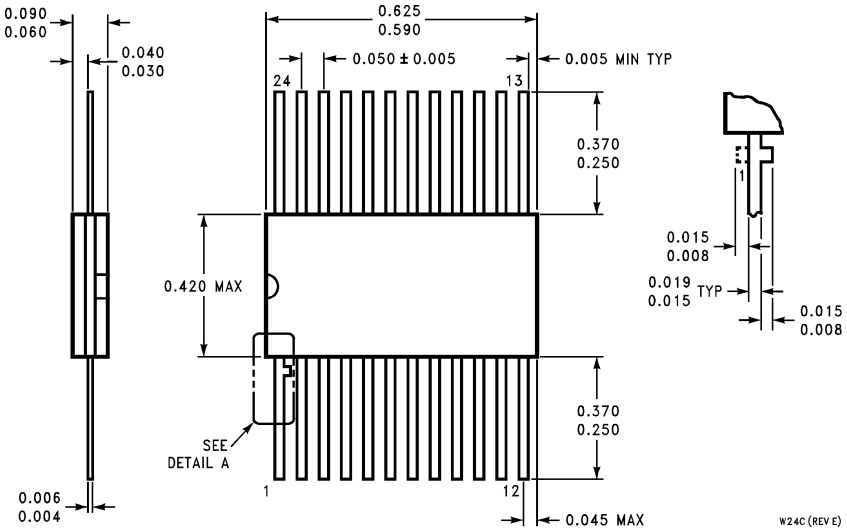


24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B



24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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54F821 10-Bit D Flip-Flop

Contents

General Description

The 'F821 is a 10-bit D-type flip-flop with TRI-STATE® true outputs arranged in a broadside pinout. The 'F821 is functionally and pin compatible with the AMD's Am29821.

Features

- TRI-STATE Outputs
- Direct replacement for AMD's Am29821

Datasheet

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
54F821 10-Bit D-Type Flip-Flop	153 Kbytes	9-Dec-97	View Online	Download	Receive via Email

Please use Adobe Acrobat to view PDF file(s).
If you have trouble printing, see Printing Problems.

Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	# pins		SPICE	IBIS		Quantity	$US each		
5962-89438013A	LCC	28	Full production	N/A	N/A	.	50+	$20.0000	tray of 25	[logo]¢Z¢S¢4¢A 54F821 LMQB /Q¢M$E 5962-89438013A
5962-8943801LA	Cerdip	24	Full production	N/A	N/A	.	50+	$7.5000	tube of 15	[logo]¢Z¢S¢4¢A$E 54F821SDMQB /Q¢M 5962-8943801LA

[Information as of 1-Sep-2000]
