HARRIS Semiconductor

CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T

January 1998

Fast CMOS 16-Bit Latched Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices Are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16543T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162543T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162H543T**
  - **Bus Hold Retains Last Active Bus State During Three-State**
  - **Eliminates the Need for External Pull-Up Resistors**

Description

These devices are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($_X\overline{CEAB}$) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With $_X\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $_X\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $_X\overline{CEAB}$ and $_X\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $_X\overline{CEBA}$, $_X\overline{LEBA}$, and $_X\overline{OEBA}$ inputs.

The CD74FCT16543T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162543T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H543T has “Bus Hold” which retains the input’s last state whenever the input goes to high impedance preventing “floating” inputs and eliminating the need for pull-up/down resistors.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543TSM	-40 to 85	56 Ld SSOP	M56.300-P

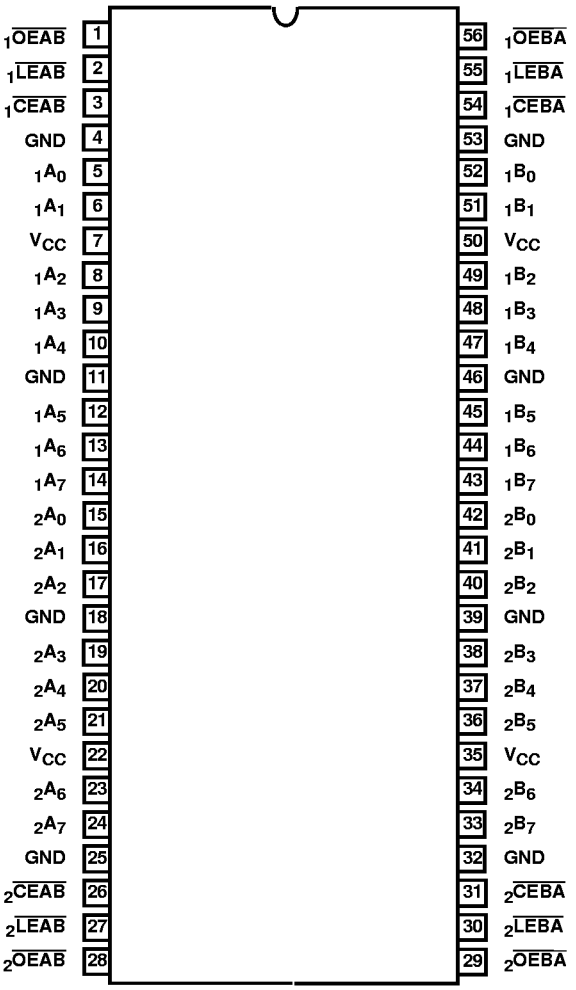
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

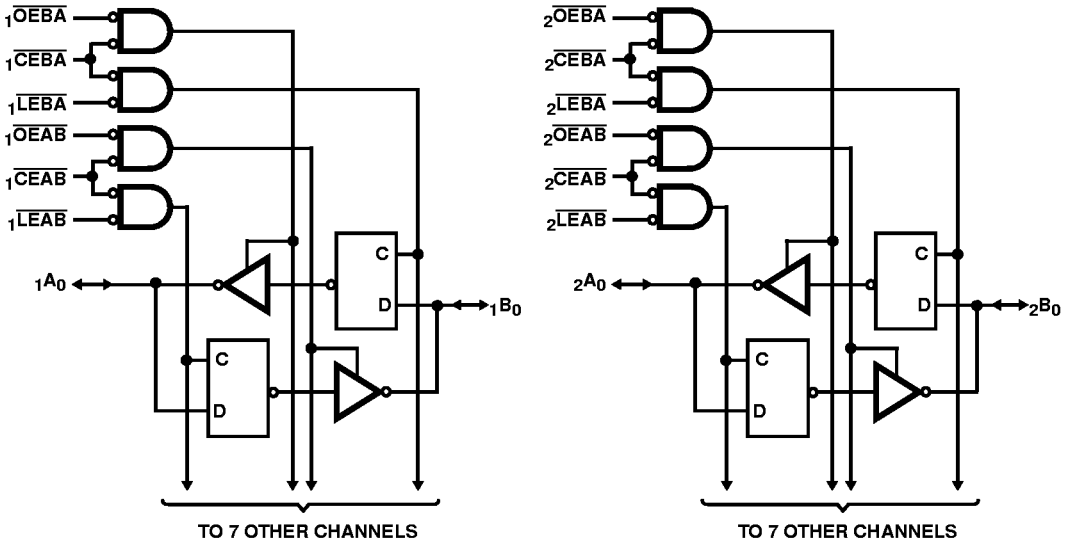
File Number **4187.2**

Pinout

CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$_X\overline{CEAB}$	$_X\overline{LEAB}$	$_X\overline{OEAB}$	$_XA_X$ TO $_XB_X$	$_XB_X$
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using $_X\overline{CEBA}$, $_X\overline{LEBA}$, and $_X\overline{OEBA}$.
2. Before xLEAB LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$_X\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$_X\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$_X\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$_X\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$_X\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$_XA_X$	A-to-B Data Inputs or B-to-A Three-State Outputs
$_XB_X$	B-to-A Data Inputs or A-to-B Three-State Outputs (Note 4)
GND	Ground
V_{CC}	Power

NOTE:

4. For the CD74FCT162H543T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} ($^oC/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 9) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 9) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 9) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 9) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 9) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 10)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 8), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
CD74FCT16543T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162543T, CD74FCT162H543T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 8)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 8)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 11)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 11)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 12)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 13)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{CEAB}$ and $\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 15)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 14)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 14)	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 14)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 14)	mA

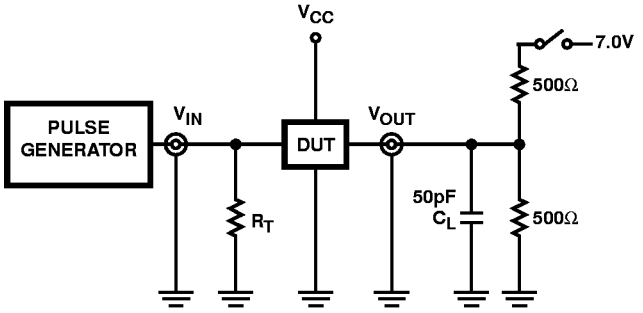
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Transparent Mode $_XA_X$ to $_XB_X$ or $_XB_X$ to $_XA_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
Propagation Delay $_X\overline{LEBA}$ to $_XA_X$ $_X\overline{LEAB}$ to $_XB_X$	t_{PLH}, t_{PHL}		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
Output Enable Time $_X\overline{OEBA}$ or $_X\overline{OEAB}$ to $_XA_X$ or $_XB_X$	t_{PZH}, t_{PZL}		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
Output Disable Time (Note 18) $_X\overline{OEBA}$ or $_X\overline{OEAB}$ to $_XA_X$ or $_XB_X$	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
Setup Time HIGH or LOW, $_XA_X$ or $_XB_X$ to $_X\overline{LEAB}$ or $_X\overline{LEBA}$	t_{SU}		3.0	-	2.0	-	2.0	-	2.0	-	1.0	-	ns
Hold Time HIGH or LOW, $_XA_X$ or $_XB_X$ to $_X\overline{LEAB}$ or $_X\overline{LEBA}$	t_H		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
$_X\overline{LEAB}$ or $_X\overline{LEBA}$ Pulse Width LOW (Note 18)	t_W		5.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. Pins with Bus Hold are identified in the pin description.
10. This specification does not apply to bi-directional functionalities with Bus Hold.
11. This parameter is determined by device characterization but is not production tested.
12. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
14. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
15. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

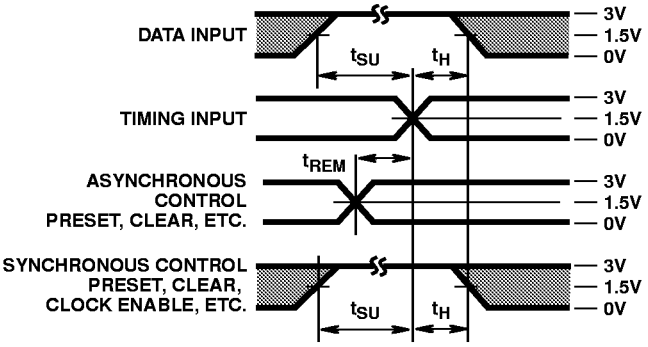


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

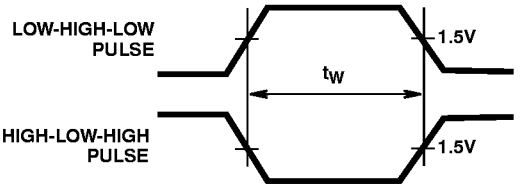


FIGURE 3. PULSE WIDTH

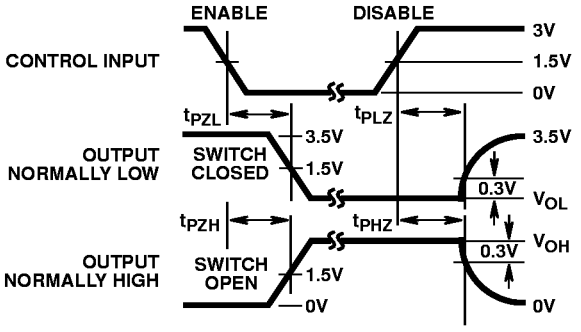


FIGURE 4. ENABLE AND DISABLE TIMING

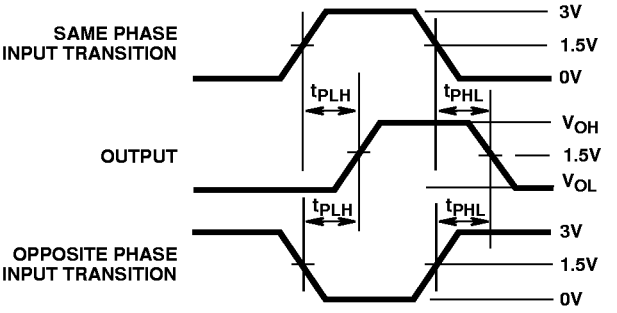


FIGURE 5. PROPAGATION DELAY