DATA SHEET

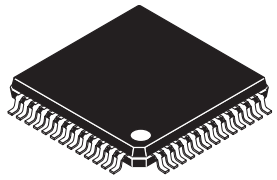
Low Voltage PLL Clock Driver

MPC973

The MPC973 is a 3.3 V compatible, PLL based clock driver device targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550 ps the MPC973 is ideally suited for most synchronous systems. The device offer twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with PowerPC™ and Pentium™ Microprocessors
- LQFP Packaging
- 3.3 V V_{CC}
- ± 100ps Typical Cycle–to–Cycle Jitter

LOW VOLTAGE PLL CLOCK DRIVER



SCALE 2:1

FA SUFFIX
52–LEAD LQFP PACKAGE
CASE 848D-03

The MPC973 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The Power–On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power–up to ensure synchronization between the QFB output and the other outputs. The internal power–on reset is designed to provide this function, but with power–up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The MPC973 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of “green” class machines. The MPC973 allows for the enabling of each output independently via a serial input port. When disabled or “frozen” the outputs will be locked in the “LOW” state, however the internal state machines will continue to run. Therefore when “unfrozen” the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the “LOW” state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC973 have internal pull–up resistors.

The MPC973 is fully 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50 Ω transmission lines. For series terminated lines each MPC973 output can drive two 50 Ω lines in parallel thus effectively doubling the fanout of the device.

The MPC973 can consume significant power in some configurations. Users are encouraged to review Application Note AN1545/D in the Advanced Clock Drivers Device Data book (DL207/D) for a discussion on the thermal issues with the MPC family of clock drivers.

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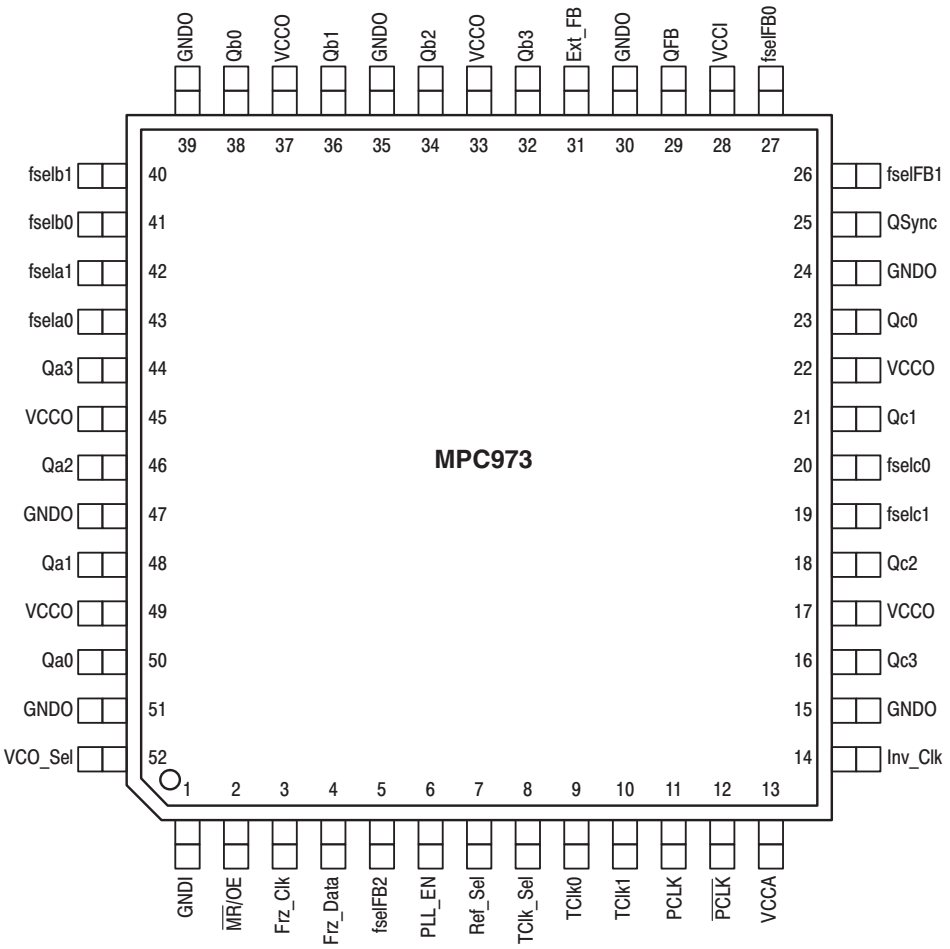


All inputs have internal pull–up resistors (appr. 50 K) except for the xtal1 and xtal2 pins.

Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

FUNCTION TABLE 2

*fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

* If the fselFB2 is 1, it may be necessary to apply a reset after power up to ensure synchronization between QFB and the other inputs.

FUNCTION TABLE 3

Control Pin	Logic ‘0’	Logic ‘1’
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	Xtal (PECL)
TCLK_Sel	TCLK0	TCLK1
PLL_En	Bypass PLL	Enable PLL
MR/OE	Master Reset/Output Hi–Z	Enable Outputs
Inv_Clk	Non–Inverted Qc2, Qc3	Inverted Qc2, Qc3

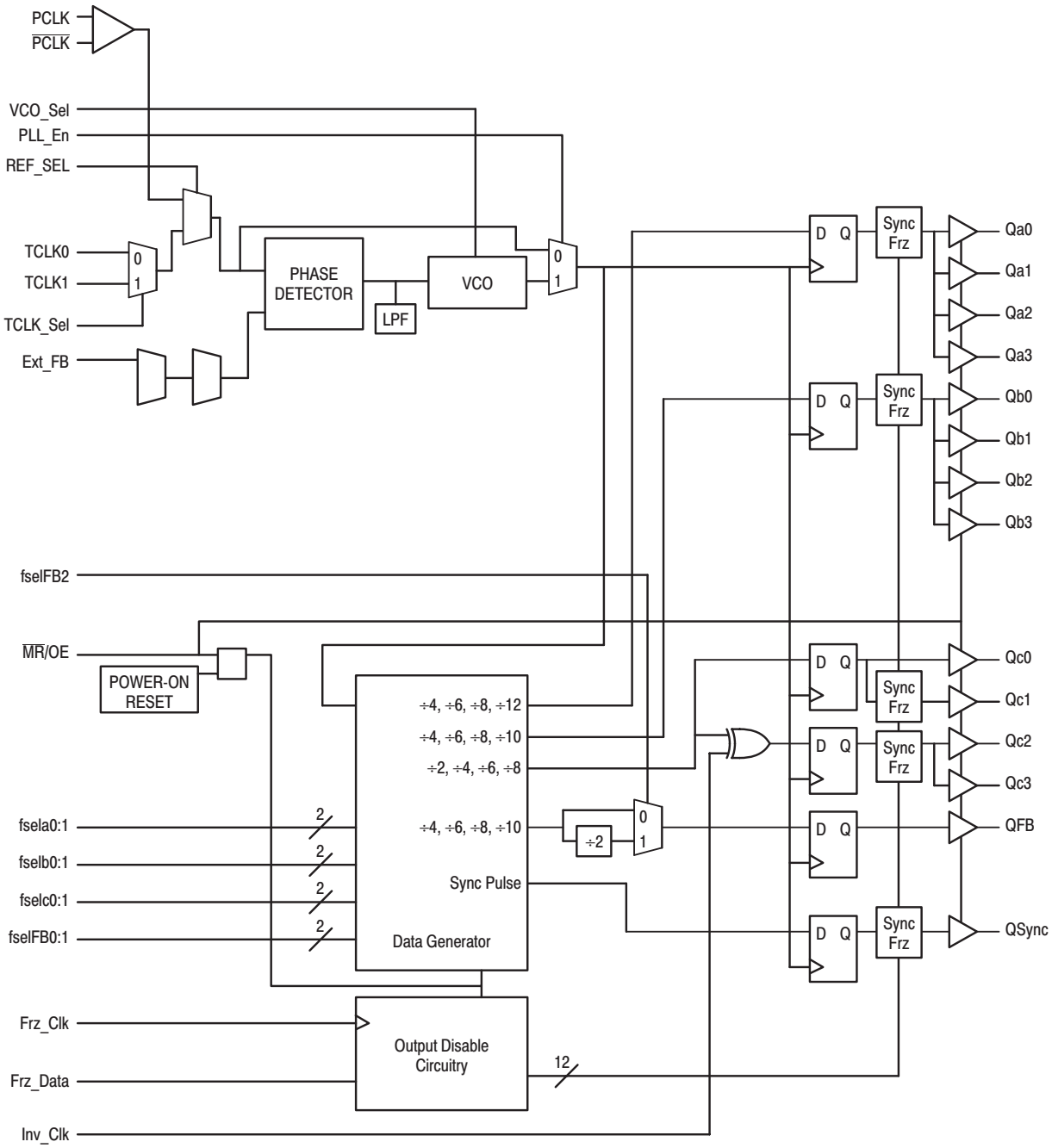


Figure 2. Logic Diagram

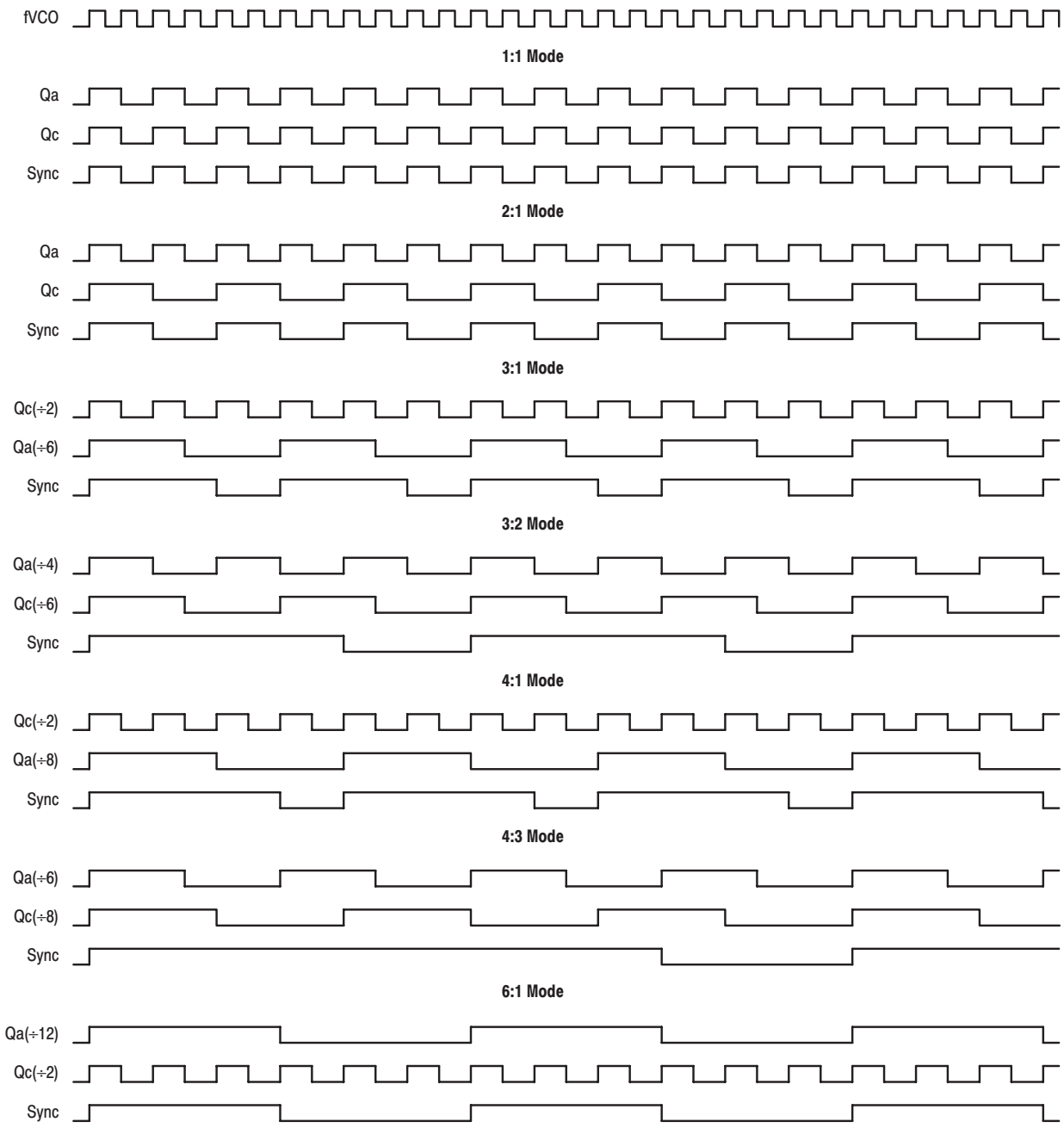


Figure 3. Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS (Note 4.; T_A = 0° to 70°C; V_{CC} = 3.3 V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{CCA}	Analog V_{CC} Voltage		2.935		V_{CC}	V	
V_{IH}	Input HIGH Voltage		2.0		3.6	V	
V_{IL}	Input LOW Voltage				0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PCLK	300		1000	mV	
V_{CMR}	Common Mode Range	PCLK	V_{CC}–2.0		V_{CC}–0.6		Note 1.
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20 mA (Note 2.)
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA (Note 2.)
I_{IN}	Input Current				±120	µA	Note 3.
I_{CC}	Maximum Quiescent Supply Current			190	215	mA	All VCC PIns
I_{CCA}	Analog V_{CC} Current			15	20	mA	
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			25		pF	Per Output

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the V_{CMR} range and the input lies within the V_{PP} specification.
2. The MPC973 outputs can drive series or parallel terminated 50 Ω (or 50 Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.
4. Special thermal handling may be required in some configurations.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0° to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 5.	100 Note 5.	MHz	Note 5.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

5. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0° to 70°C; V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		0.15		1.2	ns	0.8 to 2.0V, Note 6.
t_{pw}	Output Duty Cycle		$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	Note 6.
t_{pd}	SYNC to Feedback Propagation Delay	TCLK0 TCLK1 PCLK	–70 –130 –225	130 70 –25	330 270 175	ps	Notes 6., 7.; QFB = ÷8
t_{os}	Output-to-Output Skew				550	ps	Note 6.
f_{VCO}	VCO Lock Range		200		480	MHz	
f_{max}	Maximum Output Frequency	Q (÷2) Q (÷4) Q (÷6) Q (÷8)			125 120 80 60	MHz	Note 6.
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±100		ps	Note 6.
t_{PLZ}, t_{PHZ}	Output Disable Time		2		8	ns	Note 6.
t_{PZL}, t_{PZH}	Output ENable TIme		2		10	ns	Note 6.
t_{lock}	Maximum PLL Lock Time				10	ms	
f_{MAX}	Maximum Frz_Clk Frequency				20	MHz	

6. 50Ω transmission line terminated into $V_{CC}/2$.
7. t_{pd} is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Programming the MPC973

The MPC973 is the most flexible frequency programming device in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three banks the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to ÷10, the Qa outputs to ÷6 and the Qc outputs to ÷4. With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra ÷2 to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC973 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference frequency was equal to the lowest output frequency the feedback output would be set in the ÷10 mode. If the input needed to be half the lowest frequency output the fselFB2 input could be asserted to halve the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100 MHz. If one was also constrained because the only reference frequency available was 50MHz the setup in figure 8 could be used. The MPC973 provides the 100, 66 and 40MHz outputs all synthesized from the 50 MHz source. With its multitude of divide ratio capabilities the MPC973 can generate almost any frequency from a standard, common frequency already present in a design. Figures 9 and 10 illustrate a few more examples of possible MPC973 configurations.

The MPC973 has one more programming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output–output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC973 or a second PLL device to generate early or late clocks for a specific design. Figure 11 illustrates the use of two MPC973's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

Using the MPC973 as a Zero Delay Buffer

The external feedback of the MPC973 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the MPC973 is a function of the configuration used.

When used as a zero delay buffer the MPC973 will likely be in a nested clock tree application. For these applications the MPC973 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC973 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To calculate the overall uncertainty between the input reference clock and the output clocks the following approach should be used. Figure 4 through 7 contains performance information to assist in calculating the overall uncertainty. Data presented in Figures 4 through 7 is representative data but is not guaranteed under all conditions. Since the overall skew performance is a function of the input reference frequency all of the graphs provide relavent data with respect to the input reference frequency.

The overall uncertainty can be broken down into three parts; the static phase offset variation (Tpd), the I/O phase jitter and the output skew. If we assume that we have a 75 MHz reference clock, from the graphs we can pull the following information for static phase offset (SPO) and I/O jitter: the SPO variation will be 300 ps (–100 ps to +200 ps assuming a TCLK is used) and the I/O jitter will be ±105 ps (assuming a VCO/6 configuration and a ±3 sigma for min and max). The nominal delay from Figure 5 is 50 ps so that the propagation delay between the reference clock and the feedback clock is 50 ps ±255 ps.

Figure 4 can now be used to establish the uncertainty between the reference clock and all of the outputs for the MPC973. Figure 4 provides the skew of the MC973 outputs with respect to the feedback output. From Figure 4, if all of the outputs are used the propagation delay of the device will range from –555 ps (50 ps – 255 ps – 350 ps) to +705 ps (50 ps + 255 ps + 400 ps) for a total uncertainty of 1.26 ns. This 1.26ns uncertainty would hold true if multiple 973's are used in parallel in the application given that the skew between the reference clock for the devices were zero. Notice from the data in Figure 4 that if a subset of the outputs were used significant reductions in uncertainty could be obtained.

SYNC Output Description

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC973 is designed to specifically address this need. The MPC973 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

1. Programmable Output Frequency Relationships (VCO_Sel='1')

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

2. Programmable Output Frequency Relationships (VCO_Sel='1')

fselFB2	fselFB1	fselFB0	QFB
0	0	0	VCO/4
0	0	1	VCO/6
0	1	0	VCO/8
0	1	1	VCO/10
1	0	0	VCO/8
1	0	1	VCO/12
1	1	0	VCO/16
1	1	1	VCO/20

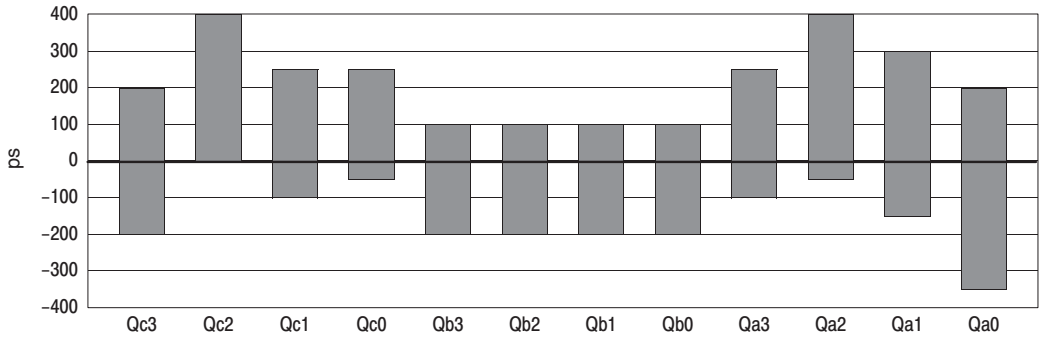


Figure 4. Typical Skews Relative to QFB

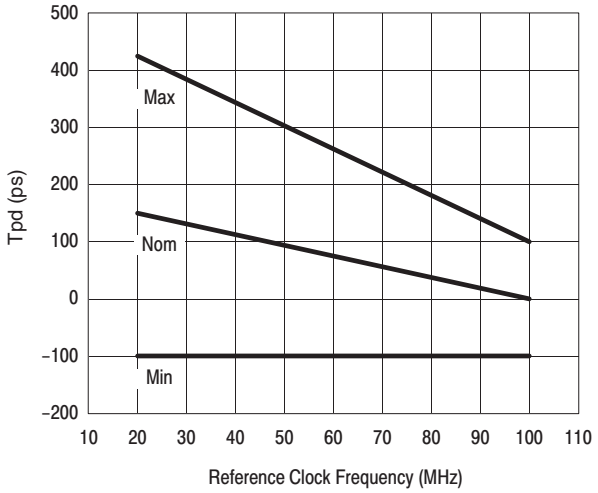


Figure 5. Typical Static Phase Offset versus Reference Frequency
T_{pd} versus TCLK

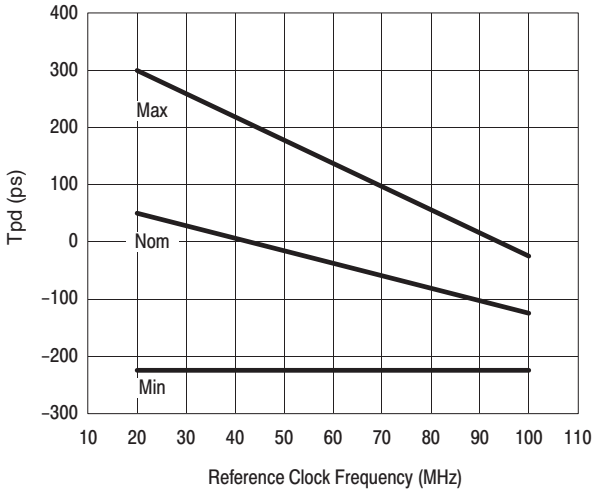


Figure 6. Typical Static Phase Offset versus Reference Frequency
T_{pd} versus PCLK

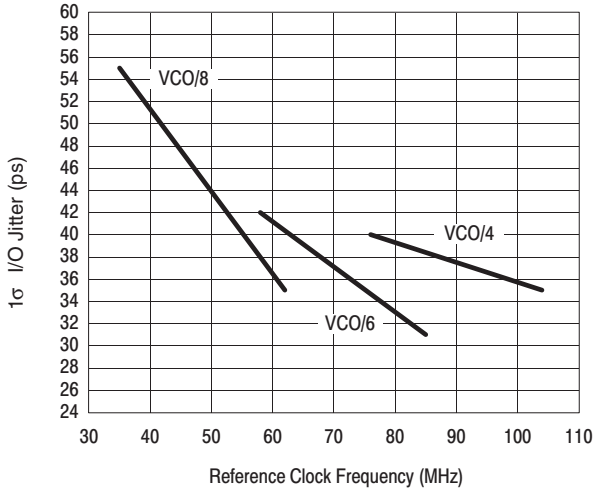


Figure 7. Typical Phase Jitter versus Reference Frequency
I/O Jitter

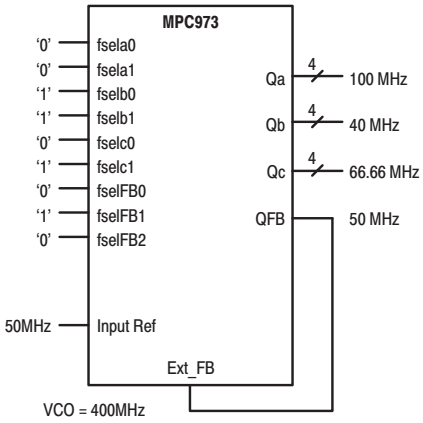


Figure 8. Programming Configuration Example

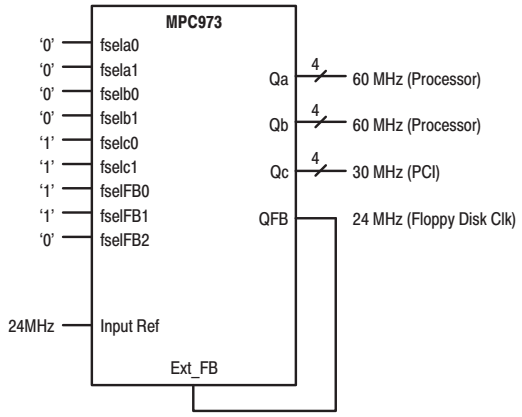


Figure 9. Generating Pentium Clocks from Floppy Clock

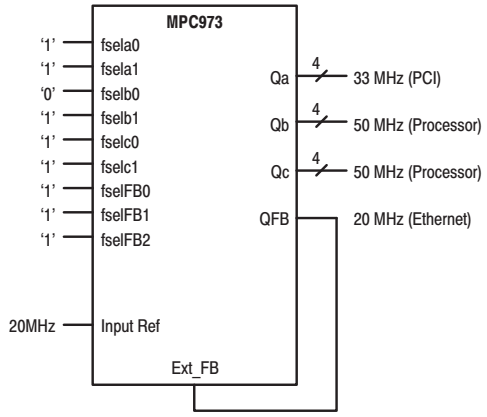


Figure 10. Generating MPC604 Clocks from Ethernet Clocks

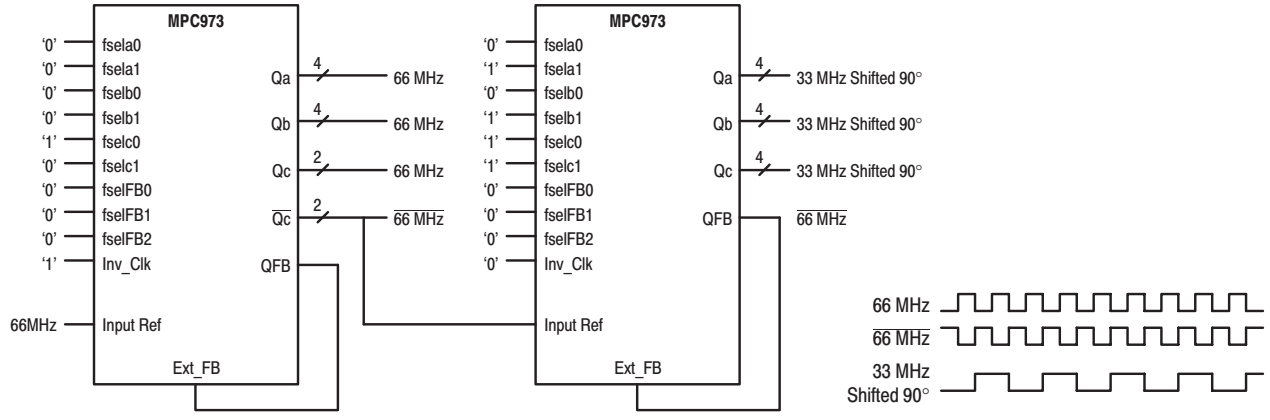


Figure 11. Phase Delay Using Multiple MPC973's

Recommended External Reset Timing

For MPC973 applications requiring synchronization of the output clock to the input clock and if fselFB2 = 1, the assertion of the $\overline{MR}$ is recommended. The timing of asserting $\overline{MR}$ should be as shown in Figure 12. The power supply should be at or above the minimum specified voltage and the reference clock input (refclk) should be present a minimum of t1 prior to the reset pulse being applied to the $\overline{MR}$ pin.

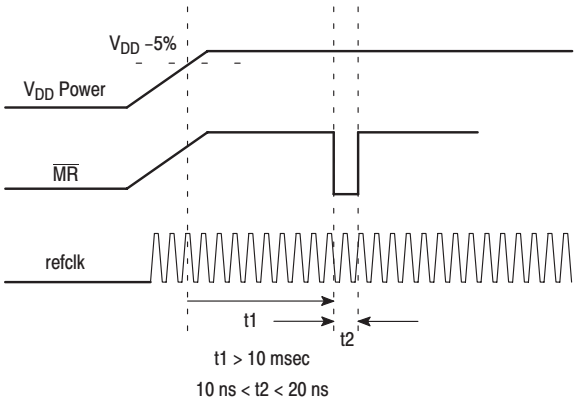


Figure 12. Assertion of $\overline{MR}$

Power Supply Filtering

The MPC973 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC973 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC973.

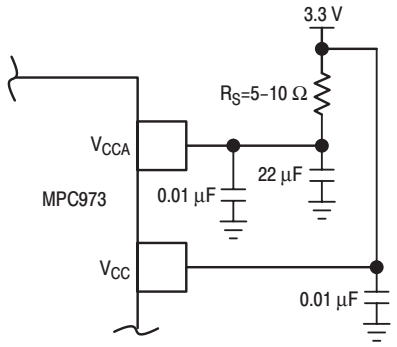


Figure 13. Power Supply Filter

Figure 13 illustrates a typical power supply filter scheme. The MPC973 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC973. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 2.935 V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 13 must have a resistance of 5–10 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC973 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC973 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC973 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 14 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC973 clock driver is effectively doubled due to its capability to drive multiple lines.

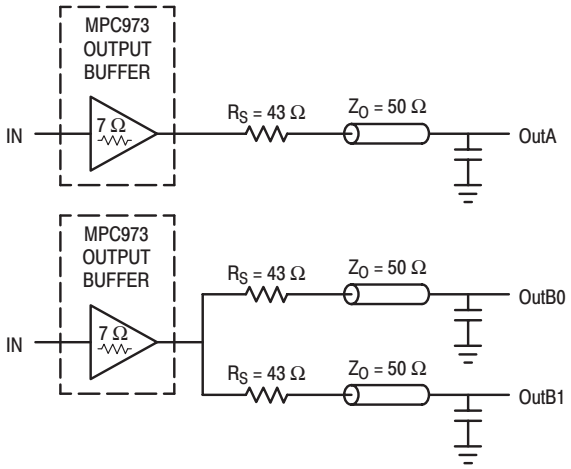


Figure 14. Single versus Dual Transmission Lines

The waveform plots of Figure 15 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC973 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used

exclusively to maintain the tight output–to–output skew of the MPC973. The output waveform in Figure 15 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40 V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 15 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

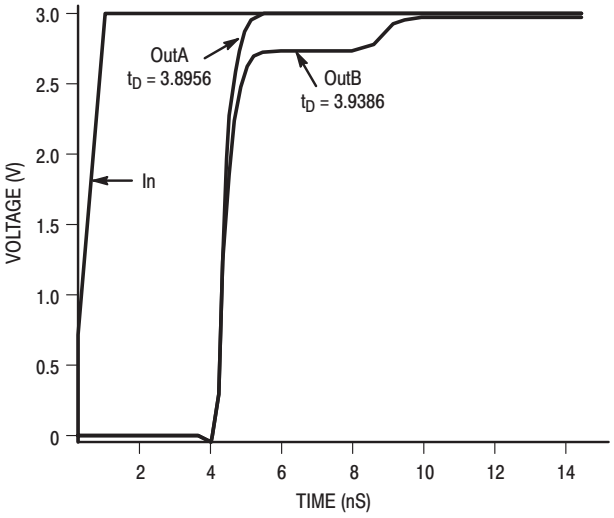
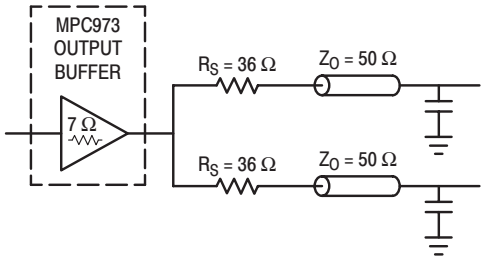


Figure 15. Single versus Dual Waveforms



7 Ω + 36 Ω || 36 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 16. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

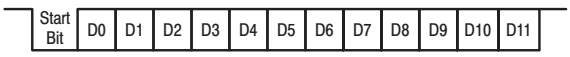
With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC973 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC973 clock outputs may be frozen (stopped in the logic ‘0’ state):

The freeze mechanism allows serial loading of the 12–bit Serial Input Register, this register contains one program–mable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may program an output clock to freeze by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The freeze logic will never force a newly–frozen clock to a logic ‘0’ state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC973 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.

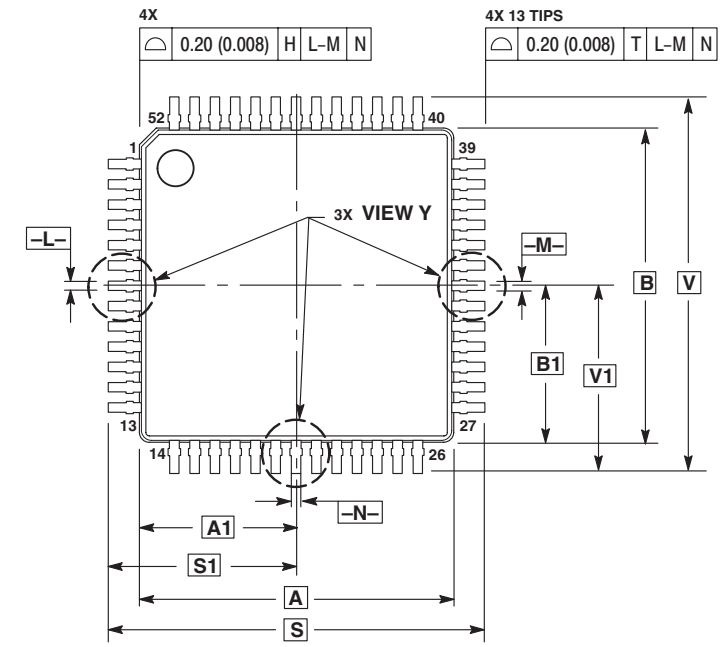


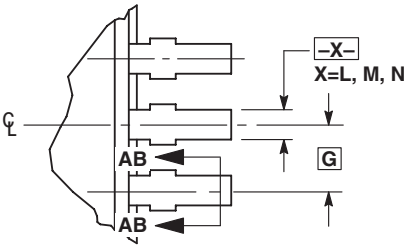
D0–D3 are the control bits for Qa0–Qa3, respectively
D4–D7 are the control bits for Qb0–Qb3, respectively
D8–D10 are the control bits for Qc1–Qc3, respectively
D11 is the control bit for QSync

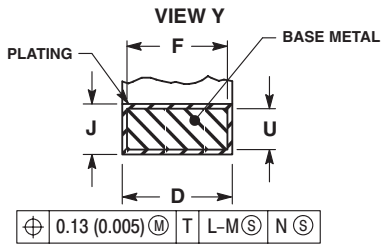
Figure 17. Freeze Data Input Protocol

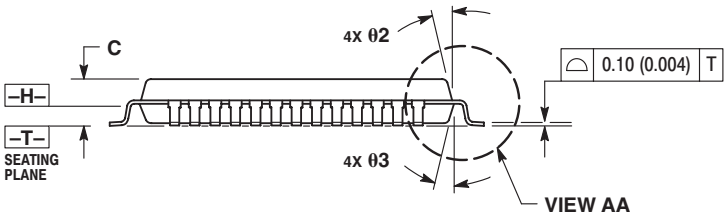
OUTLINE DIMENSIONS

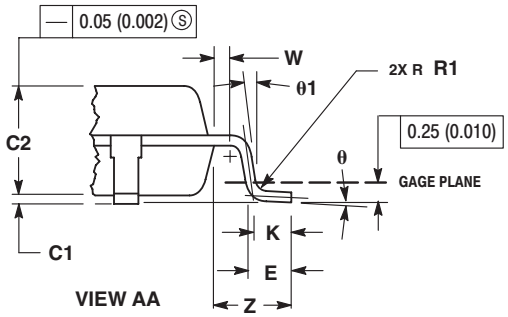
FA SUFFIX
LQFP PACKAGE
CASE 848D–03
ISSUE D











SECTION AB–AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	---	0°	---
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

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