

OBJECTIVE SPECIFICATIONS

Features

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

74AHCT: -40°C to $+85^{\circ}\text{C}$
54AHCT: -55°C to $+125^{\circ}\text{C}$

Quad 2-Input Exclusive-OR Gates

Description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = AB + A\bar{B}$.

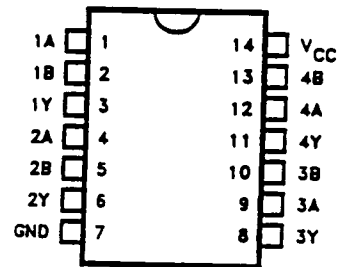
Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Function Table
(Each Gate)

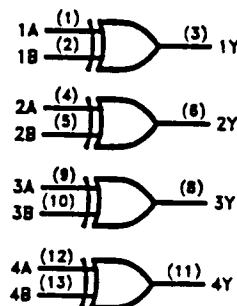
Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Pin Configuration



0017-1

Logic Diagram



0017-2

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)..... ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$)..... ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$)..... ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins..... ± 125 mA
 Storage Temperature Range, T_{STG} -65°C to +150°C
 Power Dissipation Per Package, P_D *.....500 mW

*Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range 74AHCT: -40°C to +85°C
 54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Sym	Parameter	Test Conditions	$T_A = 25^\circ C$			Unit	
			Typ	74AHCT $T_A = -40^\circ C$ to $+85^\circ C$	54AHCT $T_A = -55^\circ C$ to $+125^\circ C$		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu A$ $I_O = -4 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu A$ $I_O = 4 mA$ $I_O = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		2.0	20.0	40.0	μA

AC Electrical Characteristics (Input $t_r, t_f \leq 2$ ns), AHCT86

Sym	Parameter	Conditions •	$T_A = 25^\circ\text{C}$	74AHCT	54AHCT	Unit	
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A or B to Y (Other Input Low)	$C_L = 50$ pF	7	11	13	ns	
t_{PHL}			7	11	13		
t_{PLH}	Maximum Propagation Delay, A or B to Y (Other Input High)		8	13	15	ns	
t_{PHL}			8	13	15		
C_{IN}	Maximum Input Capacitance			5			pF
C_{PD}	Power Dissipation Capacitance*		(per gate)	15			pF

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

• For AC switching test circuits and timing waveforms see section 2.