National Semiconductor

ADVANCED INFORMATION

54F/74F620 • 54F/74F623
Inverting Octal Bus Transceiver with TRI-STATE® Outputs

General Description

The 'F623 is an octal transceiver featuring non-inverting TRI-STATE bus compatible outputs in both send and receive directions. The outputs are capable of sinking 64 mA and sourcing up to 15 mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

These octal bus transceivers are designed for asynchronous two-way data flow between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

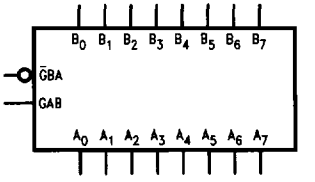
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (sixteen in all) will remain at their last states.

Features

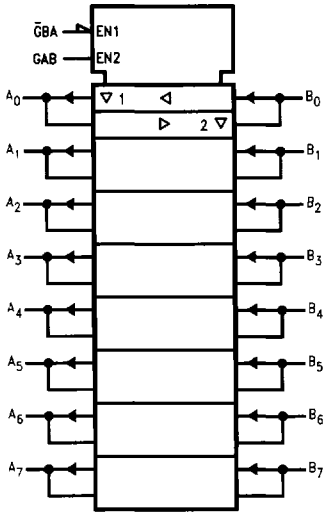
- Octal bidirectional bus interface
- TRI-STATE buffer outputs sink 64 mA
- 15 mA source current
- 'F620 inverting option of 'F623

Logic Symbols



TL/F/9577–3

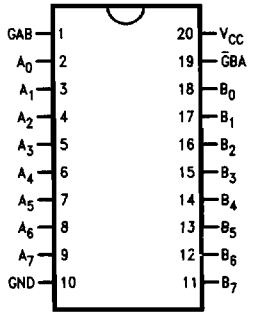
IEEE/IEC
'F623



TL/F/9577–6

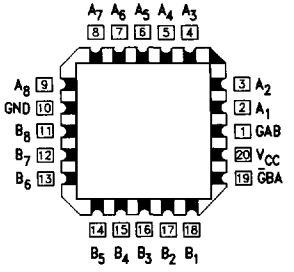
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9577–1

Pin Assignment for LCC



TL/F/9577–2

4

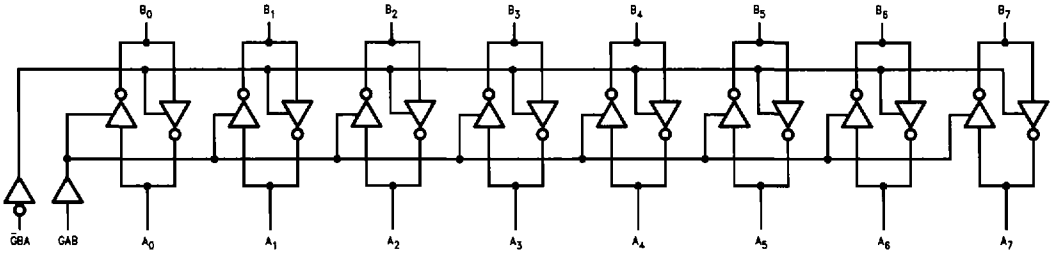
Function Table

Enable Inputs		Operation	
$\overline{G}BA$	GAB	'F620	'F623
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
H	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	$\overline{B}$ Data to A Bus, A Data to B Bus	B Data to A Bus, $\overline{A}$ Data to B Bus

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Logic Diagram

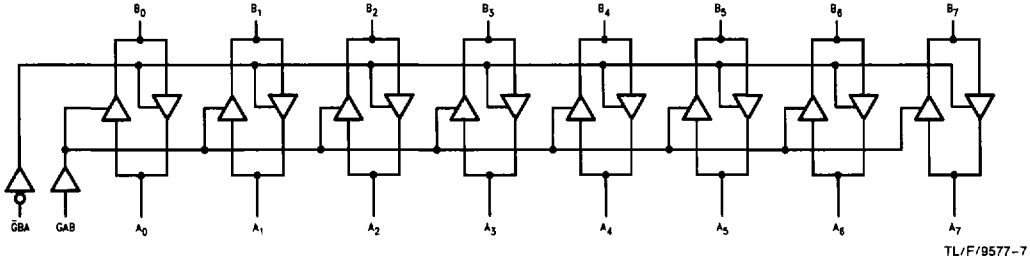
'F620



TL/F/9577–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'F623



TL/F/9577–7

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.