Precision, Single-Supply SPST Analog Switch

Features

- Low On-Resistance (33-ohm typ.) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors in Sample-and-Holds. Charge Injection, 2pC typ.
- Single-Supply Operation (+2.5V to +16V)
- Improved Second Sources for MAX323/MAX324/MAX325
- On-Resistance Matching Between Channels, <2-ohm
- On-Resistance Flatness, <6-ohm max.
- Low Off-Channel Leakage, <5nA @ +85°C
- TTL/CMOS Logic Compatible
- Fast Switching Speed, t_{ON} <150ns eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Dynamic Range
- Low Power Consumption, <5mW
- Packaging (Pb-free & Green available):
  - 8-pin SOIC (W)
  - 8-pin MOSP (U)
  - 8-pin PDIP (P)

Applications

- Audio Switching and Routing
- Portable Instruments
- Data Acquisition Systems
- Sample-and-Holds
- Telecommunication Systems
- Battery-Powered Systems

Switches shown for logic "0" input

PS323	
Logic	**Switch**
0	OFF
1	ON

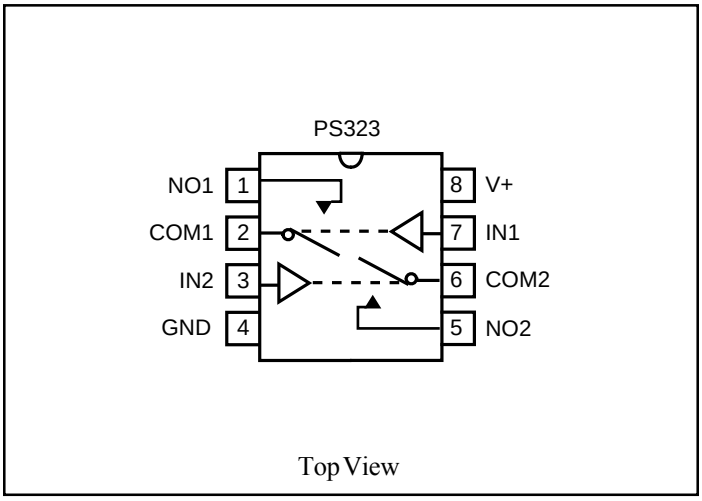
Description

The PS323 is a improved high-precision, medium- voltage analog switches designed to operate with single power supplies. The decive is a dual, single-pole single-throw (SPST), normally open (NO) switch. The switch conducts current equally well in either direction when on. In the off state, each switch blocks voltages up to the power-supply rail.

With a +5V power supply, PS323 guarantees <60-ohm On-Resistance. On-Resistance matching between channels is within 2-ohm. On-Resistance flatness is less than 6-ohm over the specified range. All three devices guarantee low leakage currents (<100 pA @ 25°C, <10nA @ +85°C) and fast switching speeds (t_{ON} <150ns). Break-before-make switching action protects against momentary crosstalk (PS325).

For single-supply operation below 5V, PI5A317/318/319 are also recommended.

Block Diagram, Pin Configuration, and Truth Table



Top View

Absolute Maximum Ratings

Voltages Referenced to GND .....
V+ ..... -0.3V to +17V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (1) ..... –2V to (V+) +2V
or 30mA, whichever occurs first
Current (any terminal) 30mA
Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA
ESD per Method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation
Plastic DIP (derate 6mW/°C above +70°C) 500mW
Narrow SO (derate 6mW/°C above +70°C) 450mW
MSOP (derate 4mW/°C above +70°C) 330mW
Storage Temperature ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA maximum.

Caution: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +5V Supply

(V+ = 5V +10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range (3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = +3.5V I_{COM} = 1mA,	25		20	35	ohm
			Full		30	60	
On-Resistance Match Between Channels (4)	ΔR_{ON}	V_{NO} or V_{NC} = +3V, I_{COM} = 1mA, V+ = 5V,	25		0.8	2	
			Full			4	
On-Resisatance Flatness (5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1V, 2V, 3V	25		2	6	
			Full			8	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	25	–0.1	–0.01	0.1	nA
			Full	–5		5	
COM Off Leakage Current (6)	$I_{COM(OFF)}$	V+ = 5.5V V_{COM} = 4.5V V_{NO} or V_{NC} = 1V	25	–0.1	–0.01	0.1	
			Full	–5		5	
COM On Leakage Current (6)	$I_{COM(ON)}$	V+ = 5.5V V_{COM} = 5V V_{NO} or V_{NC} = 5V	25	–0.2	–0.04	0.2	
			Full	–10		10	

Electrical Specifications - Single +5V Supply (continued) (V+ = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V	Full	–0.5	0.005	0.5	µA
Input Current with Input Voltage High	I_{INL}	V_{IN} = 2.4V, all others = 2.4V		–0.5	0.005	0.5	
Logic High Input Voltage	V_{INH}			2.4			V
Logic Low Input Voltage	V_{INL}					0.8	
Dynamic							
Turn-On Time (3)	t_{ON}	V_{NO} or V_{NC} = 3V, Figure 2	25		30	75	ns
			Full		60	150	
Turn-Off Time (3)	t_{OFF}		25		25	50	
			Full		50	100	
Break-Before-Make Time Delay (3)	t_D	PS325 only, RL = 300ohm, CL = 35pF, Figure 3	25	2	5		
Charge Injection (3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 4			1	5	pC
Off Isolation(7)	OIRR	R_L = 500ohm, C_L = 5pF, f = 1MHz, Figure 5			–72		dB
Crosstalk	X_{TALK}	R_L = 500ohm, C_L = 5pF, f = 1MHz, Figure 6			–85		
NC or NO Off Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 7			9		pF
COM Off Capacitance	$C_{COM(OFF)}$				9		
COM Off Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 8			22		
Supply							
Power-Supply Range	V+			2.7		16	V
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	–1		1	µA

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $DR_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of ON-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})]. See Figure 5.

Electrical Specifications - Single +3.3V Supply

(V+ = 3.3V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 3V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1.5V	25		40	70	ohm
			Full		50	80	
Dynamic							
Turn-On Time(3)	t_{ON}	V_{NO} or V_{NC} = 1.5V, Figure 2	25		50	125	ns
			Full		100	250	
Turn-Off Time(3)	t_{OFF}		25		30	75	
			Full		60	150	
Break-Before-Make Time Delay(3)	t_D	PS325 only	25	2	5		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 4	25		1	5	pC
Supply							
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off	Full	–1	0.01	1	µA

Electrical Specifications - Single +12V Supply

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 10.8V I_{COM} = 1mA, V_{NO} or V_{NC} = 10V	25		15	25	ohm
			Full		20	40	
Dynamic							
Turn-On Time(3)	t_{ON}	V_{NO} or V_{NC} = 1.5V, Figure 2	25		25	50	ns
			Full		50	100	
Turn-Off Time(3)	t_{OFF}		25		20	40	
			Full		40	75	
Break-Before-Make Time Delay(3)	t_D	PS325 only	25	2	5		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 4	25		1	5	pC
Supply							
Positive Supply Current	I+	V+ = 13V, V_{IN} = 0V or V+, all channels on or off	Full	–1	0.01	1	µA

Application Information

The PS323 dual analog switch precisely switches inputs with a single 2.7V to 12V supply, low On-Resistance (30-ohm) and high speed operation (tON = 85ns, tOFF = 25ns). The devices are suited to portable battery powered equipment due to a low supply voltage (2.7V), low power consumption (5mW), and low leakage currents (0.1nA). High frequency applications benefit from the high bandwidth, high off isolation, and low crosstalk.

Proper Power Supply Sequencing & Over-voltage Protection

With any CMOS device, proper power supply sequencing is needed to protect the device from excessive input currents, which may permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 9 below). To prevent forward biasing of these diodes, V+ must be applied before any input signals, and input signals must swing between V+ and GND. If these conditions cannot be guaranteed, then one of two suggested protection methods must be employed. Protect the logic inputs by adding a 1k-ohm resistor in series with the input (see Figure 9). The resistor limits the currents below the threshold that can cause permanent damage to sub-micro Amp levels. This reduced input current produces an insignificant voltage drop during normal operation. A series resistor is not desirable, but small-signal diodes can be added in series with the supply pins to provide over-voltage protection for the IC. The diodes limit the analog signal from 1V below V+ to 1V above GND. The leakage current will remain low, but the switch resistance may increase at low supply voltages.

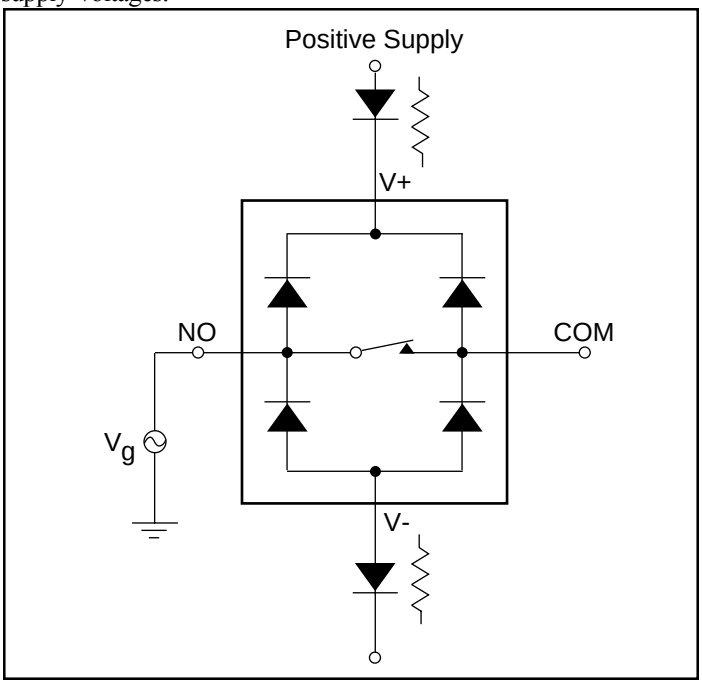


Figure 1. Overvoltage Protection

Power-Supply Considerations

The PS32X construction is typical of most CMOS analog switches, except that they have voltage supply pins: V+ and GND. These pins power the internal CMOS switches and set the analog voltage limits. Unlike switches with a 12V maximum supply voltage, the PS32X series is made from a 17V-supply voltage technology that provides room for 10-20% tolerance on 12V supplies. This technology gives room for overshoot and noise spikes. While the minimum recommended supply voltage is 2.7V, it is important to note that the input signal-range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specifications for details. V+ and GND also power the internal logic drivers (turn the switch on & off). These switches can be operated with bipolar supplies if the voltage range from V- (at the GND pin) to V+ does not exceed a total of 12V.

Logic-Level Thresholds

The switch logic is TTL compatible (0.8V & 2.4V) over a supply range of 3V to 11V. At 12V the VIH level is about 2.5V. This is below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use logic drive that provides a VOH greater than 3V. The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Signal Passing/Isolation

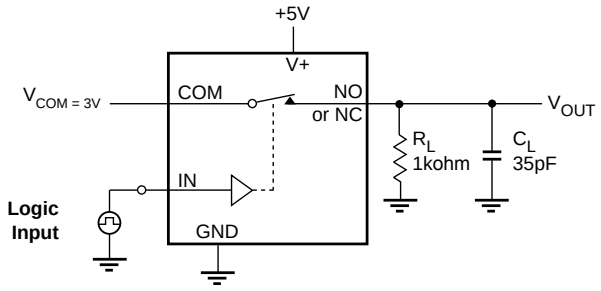
In 50-ohm systems, signal response is flat even past 300MHz. An OFF switch is like a capacitor and passes high frequencies with low attenuation, resulting in signal passing from the switch input to output. OFF Isolation is the resistance to passing signals while the switch is OFF, while Crosstalk indicates the amount of signal noise that crosses over from one switch to another. The OFF Isolation is about 50dB in 50Ohm systems. Larger load impedances reduce Off Isolation and Crosstalk due to the voltage divider action of the switch OFF impedance and the load.

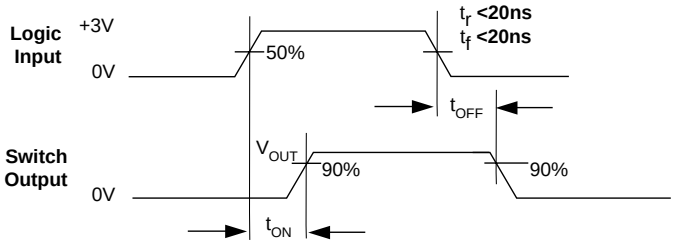
Leakage Current

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Most of the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Either V+ or GND and the analog signal bias each diode. Hence, leakage currents will vary as the signal varies. The difference in the diode leakage currents to the V+ and GND pins creates the analog signal-path leakage current. Also, analog leakage currents flow between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or GND.

Test Circuits/Timing Diagrams



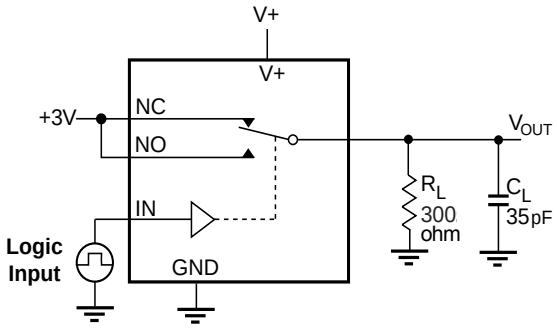


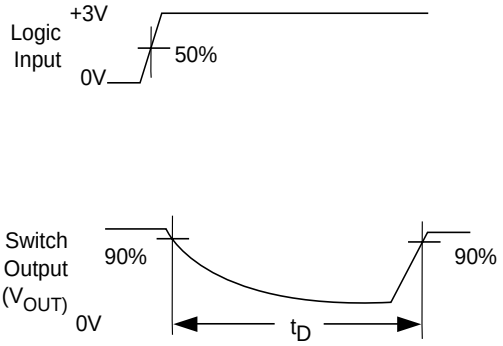
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC

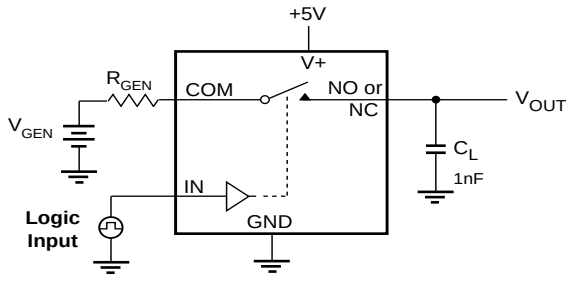
Figure 2. Switching Time

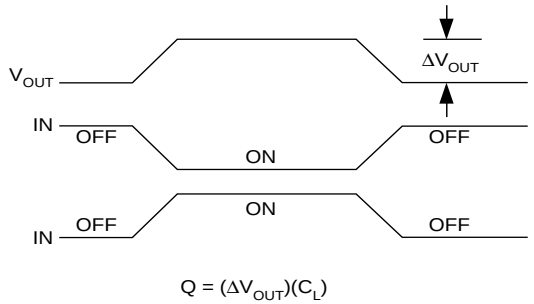




C_L INCLUDES FIXTURE AND STRAY CAPACITANCE.

Figure 3. Break-Before-Make Interval (PS325 only)





$$Q = (\Delta V_{OUT})(C_L)$$

IN POLARITY DEPENDS ON NO OR NC SWITCH FUNCTION

Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

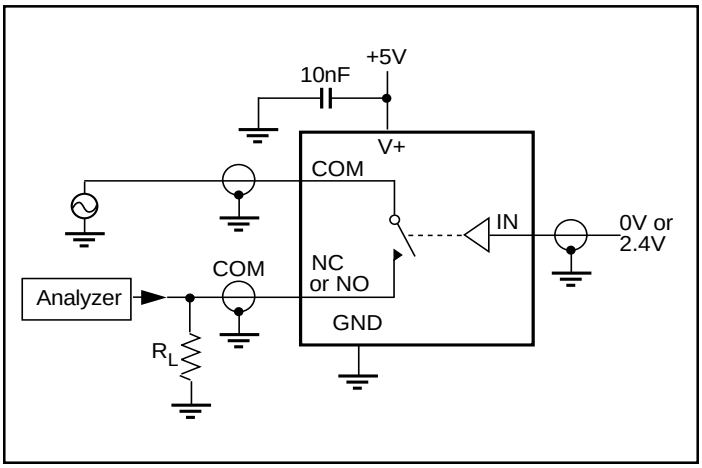


Figure 5. Off Isolation

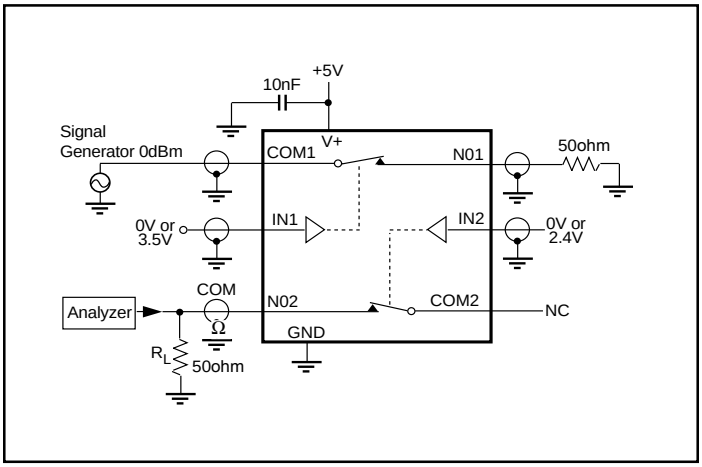


Figure 6. Crosstalk

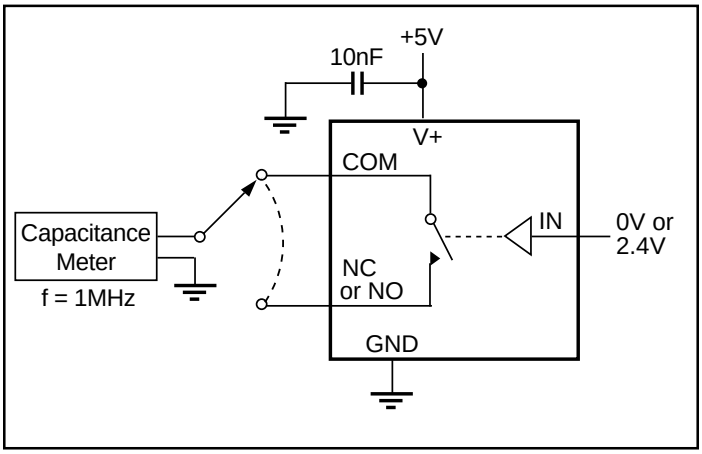


Figure 7. Channel-Off Capacitance

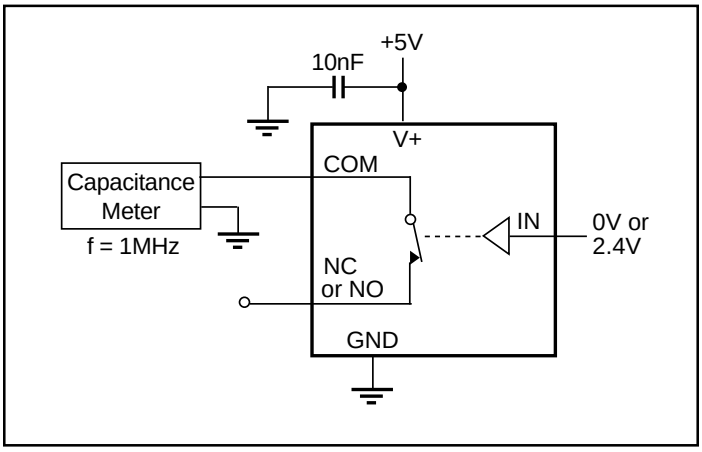


Figure 8. Channel-On Capacitance

Typical Performance Curves (TA = 25°C unless otherwise noted)

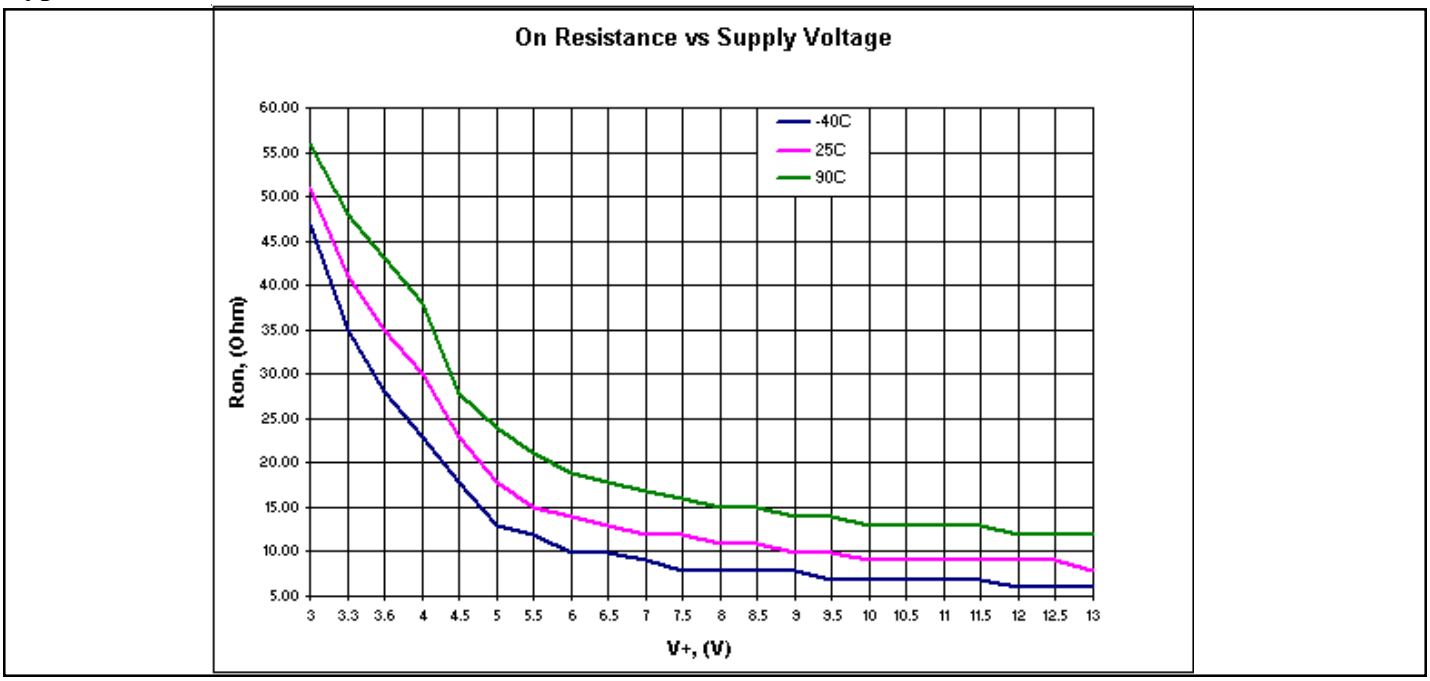


Figure 9. On Resistance vs. Supply Voltage

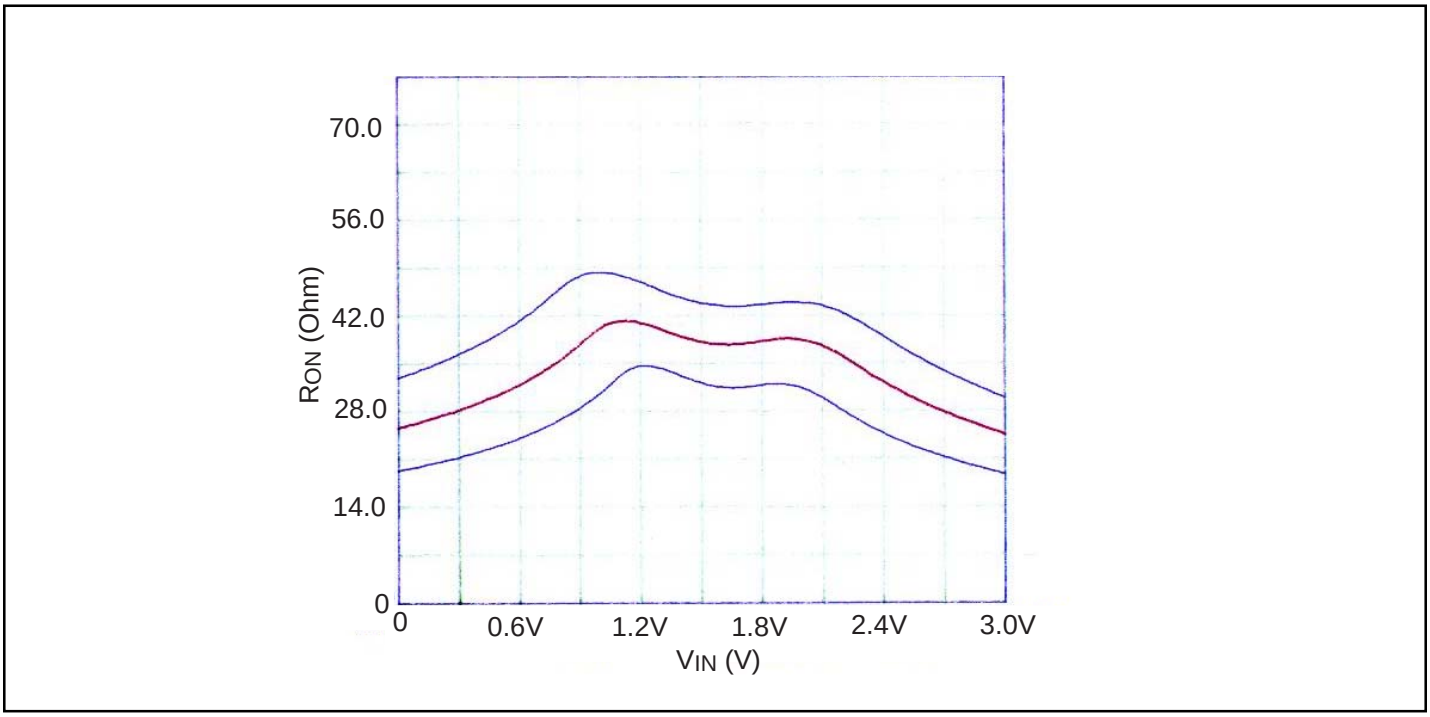


Figure 10. On Resistance vs. Switch Voltage, V_{CC} = 3.3V

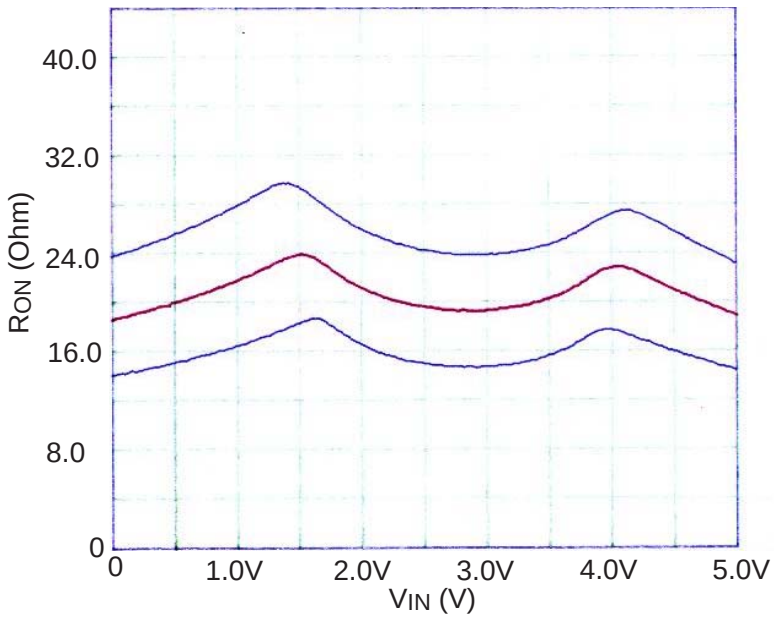


Figure 11. On Resistance vs. Switch Voltage, V_{CC} = 5V

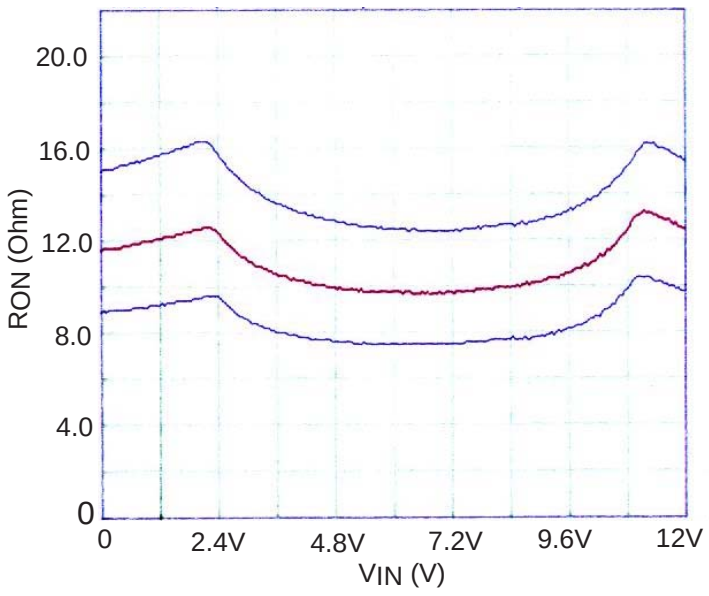


Figure 12. On Resistance vs. Switch Voltage, V_{CC} = 12V

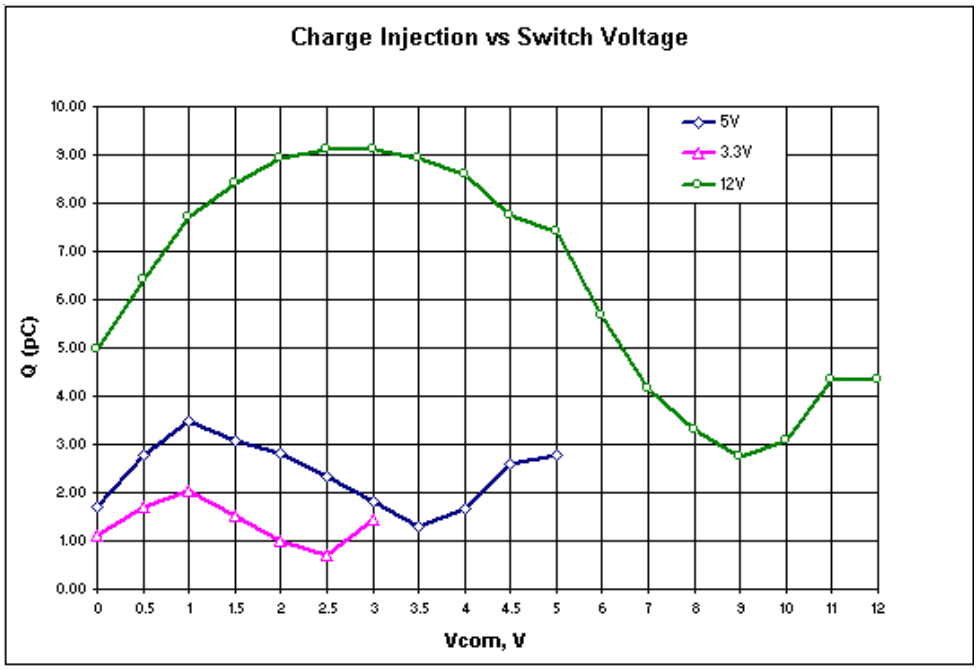


Figure 13. Charge Injection vs. Switch Voltage

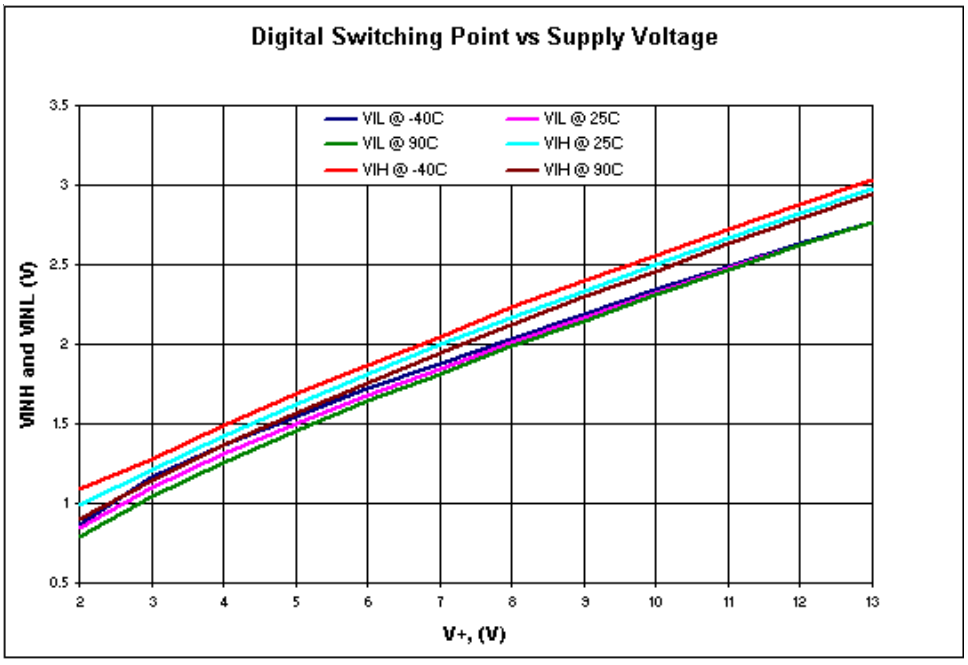
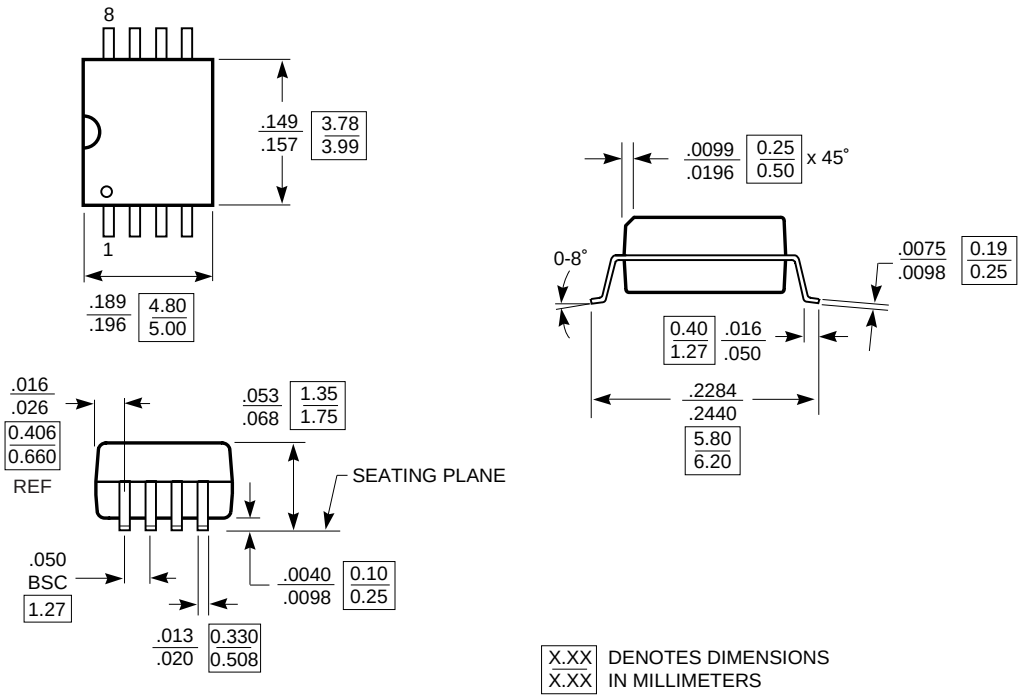
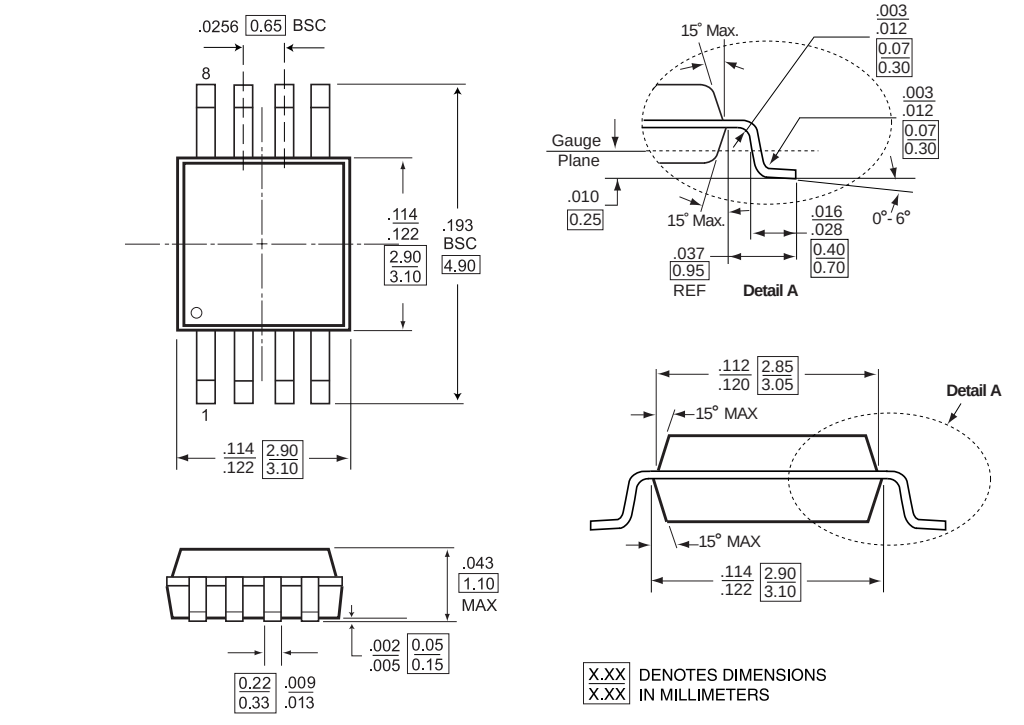


Figure 14. Digital Switching point vs. Supply Voltage

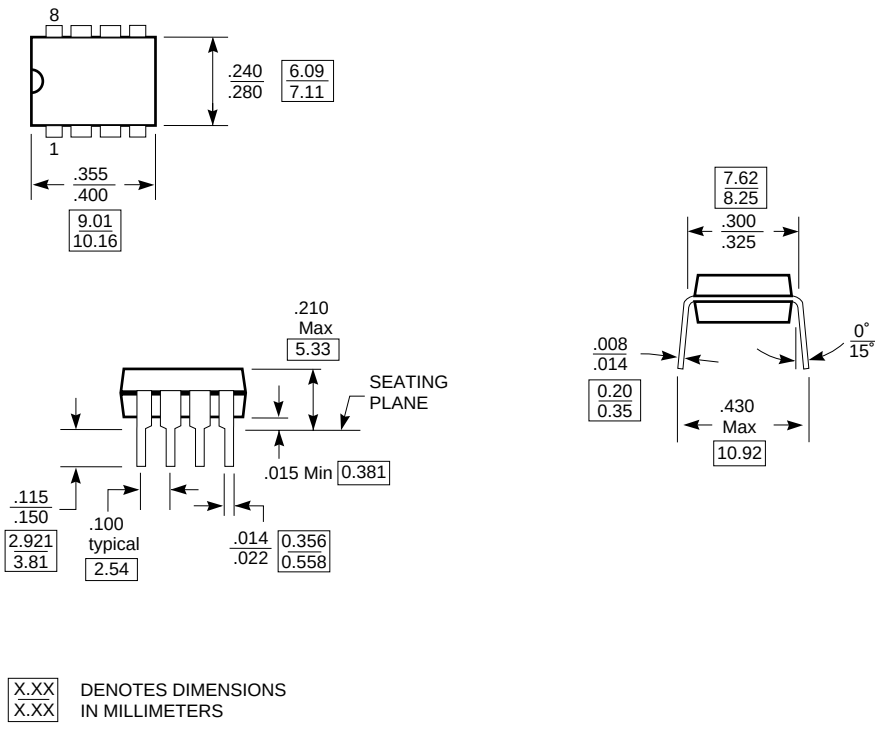
Packaging Mechanical: 8-pin SOIC (W)



Packaging Mechanical: 8-pin MSOP (U)



Packaging Mechanical: 8-pin PDIP (P)



Ordering Information

Ordering Code	Package Code	Package Type
PS323CSA	W	8-pin SOIC
PS323CSAE	W	Pb-free & Green, 8-pin SOIC
PS323CUA	U	8-pin MSOP
PS323CUAE	U	Pb-free & Green, 8-pin MSOP
PS323CPA	P	8-pin PDIP
PS323CPAE	P	Pb-free & Green, 8-pin PDIP
PS323ESA	W	8-pin SOIC
PS323ESAE	W	Pb-free & Green, 8-pin SOIC
PS323EUA	U	8-pin MSOP
PS323EUAE	U	Pb-free & Green, 8-pin MSOP
PS323EPA	P	8-pin PDIP
PS323EPAE	P	Pb-free & Green, 8-pin PDIP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/