

# SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
  - SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs
  - SN74ALS876A, SN74AS876 Have Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

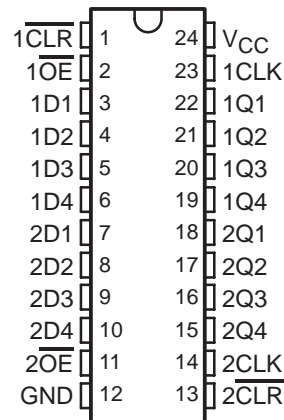
## description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

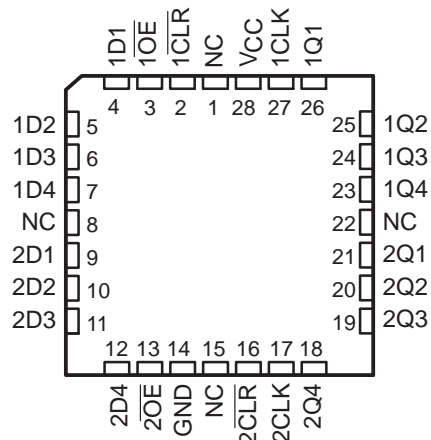
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear ( $\overline{\text{CLR}}$ ) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset ( $\overline{\text{PRE}}$ ) inputs and inverting  $\overline{\text{Q}}$  outputs; taking  $\overline{\text{PRE}}$  low causes the four  $\overline{\text{Q}}$  or Q outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS874B . . . JT PACKAGE  
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE  
(TOP VIEW)

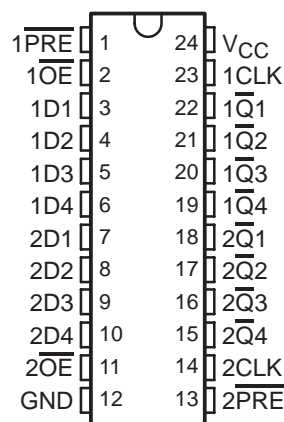


SN54ALS874B . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE  
(TOP VIEW)



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## Function Tables

SN54ALS874B, SN74ALS874B, SN74AS874  
(each flip-flop)

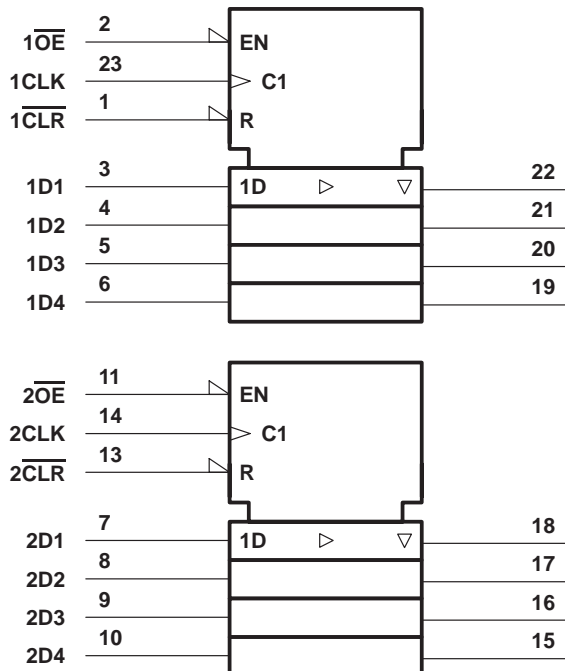
INPUTS				OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	CLK	D	
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	$Q_0$
H	X	X	X	Z

SN74ALS876A, SN74AS876  
(each flip-flop)

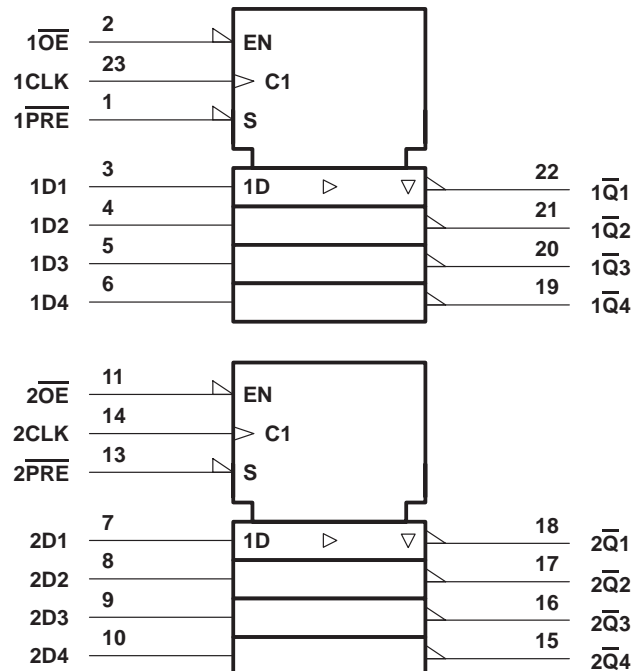
INPUTS				OUTPUT $\overline{Q}$
$\overline{OE}$	$\overline{PRE}$	CLK	D	
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q_0}$
H	X	X	X	Z

## logic symbols†

SN54ALS874B, SN74ALS874B, SN74AS874



SN74ALS876A, SN74AS876

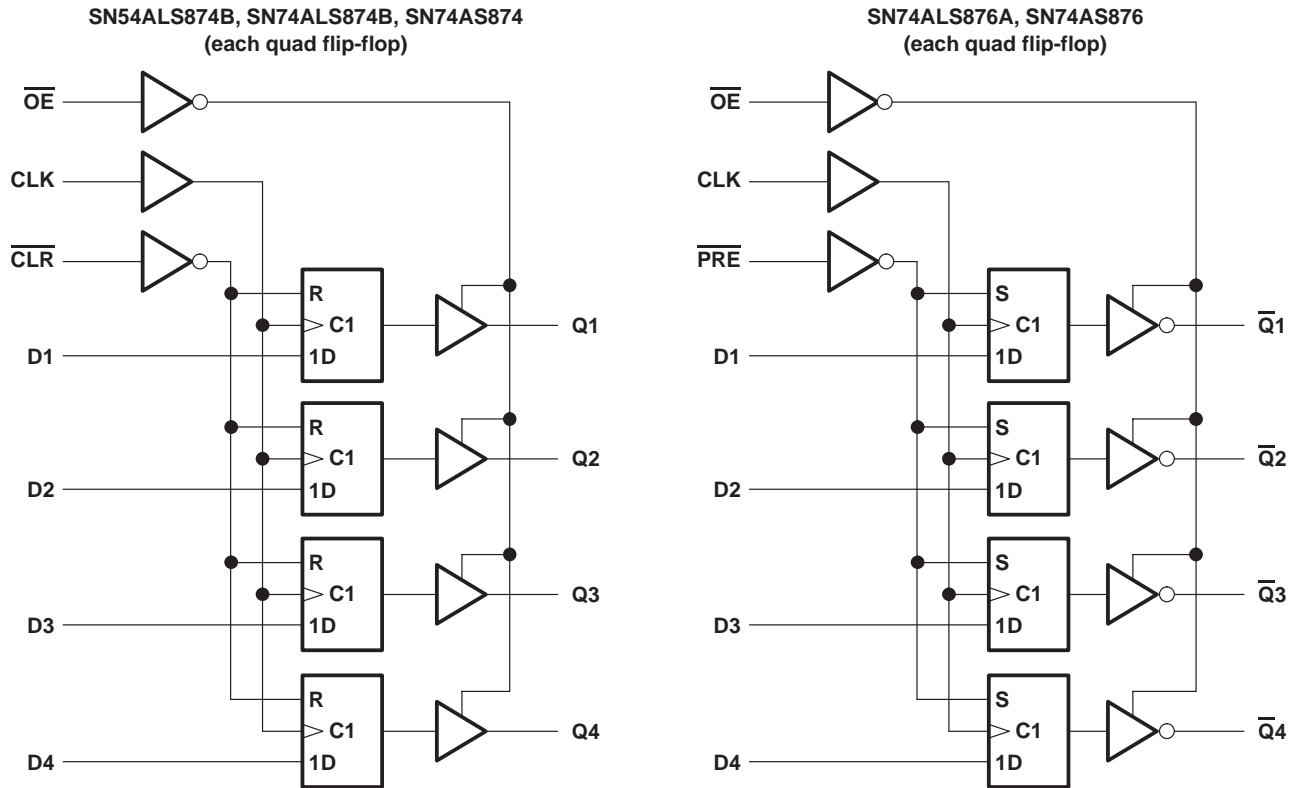


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

# SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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## logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS874B .....	–55°C to 125°C
SN74ALS874B, SN74ALS876A .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**recommended operating conditions**

		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V <sub>IH</sub>	High-level input voltage	2			2			V		
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V		
I <sub>OH</sub>	High-level output current			-1			-2.6	mA		
I <sub>OL</sub>	Low-level output current			12			24	mA		
f <sub>clock</sub>	Clock frequency	0		25	0		30	MHz		
t <sub>w</sub>	Pulse duration	PRE or CLR low		15	10		ns			
		CLK high		20	16.5					
		CLK low		20	16.5					
t <sub>su</sub>	Setup time before CLK↑	Data		15	15		ns			
		PRE or CLR inactive		15	10					
t <sub>h</sub>	Hold time, data after CLK↑	4			0			ns		
T <sub>A</sub>	Operating free-air temperature	-55			125			0	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2			-1.2	V	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA		V <sub>CC</sub> - 2			V <sub>CC</sub> - 2			V	
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA		2.4	3.3					
			I <sub>OH</sub> = -2.6 mA					2.4	3.2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4		
			I <sub>OL</sub> = 24 mA					0.35	0.5		
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		20			20			μA	
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V		-20			-20			μA	
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1			0.1			mA	
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20			20			μA	
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.2			-0.2			mA	
I <sub>O‡</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		-20	-112		-30	-112		mA	
I <sub>CC</sub>	'ALS874B	V <sub>CC</sub> = 5.5 V	Outputs high		14	21		14	21		mA
			Outputs low		19	30		19	30		
			Outputs disabled		20	32		20	32		
	SN74ALS876A	V <sub>CC</sub> = 5.5 V	Outputs high					14	21		
			Outputs low					18	29		
			Outputs disabled					20	31		

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.



**SN54ALS874B, SN74ALS874B, SN74ALS876A  
SN74AS874, SN74AS876  
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS874B		SN74ALS874B		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30		MHz
t <sub>PLH</sub>	CLK	Any Q	4	18	4	14	ns
t <sub>PHL</sub>			4	16	4	14	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Any Q	5	23	5	17	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any Q	4	24	4	18	ns
t <sub>PZL</sub>			4	21	4	18	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any Q	2	15	2	10	ns
t <sub>PLZ</sub>			3	22	3	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS876A		
			MIN	MAX	
f <sub>max</sub>			30		MHz
t <sub>PLH</sub>	CLK	Any $\overline{\text{Q}}$	4	14	ns
t <sub>PHL</sub>			4	14	
t <sub>PHL</sub>	$\overline{\text{PRE}}$	Any $\overline{\text{Q}}$	6	19	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	4	18	ns
t <sub>PZL</sub>			4	18	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	2	10	ns
t <sub>PLZ</sub>			3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage, V <sub>CC</sub> .....	7 V
Input voltage, V <sub>I</sub> .....	7 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS874, SN74AS876 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**recommended operating conditions**

		SN74AS874			SN74AS876			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-15			-15	mA
$I_{OL}$	Low-level output current			48			48	mA
$f_{clock}$	Clock frequency	0		125	0		80	MHz
$t_w$	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low		2		4.5		ns
		CLK high		3		6.2		
		CLK low		4		6.2		
$t_{su}$	Setup time before CLK $\uparrow$	Data		2		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive		4		5		
$t_h$	Hold time, data after CLK $\uparrow$	1			2			ns
$T_A$	Operating free-air temperature	0		70	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN74AS874		SN74AS876		UNIT
				MIN	TYP $\dagger$	MAX	MIN	
$V_{IK}$		$V_{CC} = 4.5$ V,	$I_I = -18$ mA				-1.2	V
$V_{OH}$		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} - 2$				V
		$V_{CC} = 4.5$ V,	$I_{OH} = -15$ mA	2.4	3.3			
$V_{OL}$		$V_{CC} = 4.5$ V,	$I_{OL} = 48$ mA		0.35	0.5		V
$I_{OZH}$		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V				50	$\mu$ A
$I_{OZL}$		$V_{CC} = 5.5$ V,	$V_O = 0.4$ V				-50	$\mu$ A
$I_I$		$V_{CC} = 5.5$ V,	$V_I = 7$ V				0.1	mA
$I_{IH}$		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V				20	$\mu$ A
$I_{IL}$	D	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V				-2	mA
	All others						-0.5	
$I_{O\ddagger}$		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V		-30		-112	mA
$I_{CC}$	SN74AS874	$V_{CC} = 5.5$ V	Outputs high		82	133	mA	
			Outputs low		92	149		
			Outputs disabled		100	160		
	SN74AS876		Outputs high		88	142		
			Outputs low		94	150		
			Outputs disabled		100	160		

$\dagger$  All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^{\circ}$ C.

$\ddagger$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74AS874		
			MIN	MAX	
f <sub>max</sub>			125		MHz
t <sub>PLH</sub>	CLK	Any Q	3	8.5	ns
t <sub>PHL</sub>			4	10.5	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Any Q	4	9.5	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any Q	2	7	ns
t <sub>PZL</sub>			3	10.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any Q	2	6	ns
t <sub>PLZ</sub>			2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74AS876		
			MIN	MAX	
f <sub>max</sub>			80		MHz
t <sub>PLH</sub>	CLK	Any $\overline{\text{Q}}$	3	8.5	ns
t <sub>PHL</sub>			4	10.5	
t <sub>PHL</sub>	$\overline{\text{PRE}}$	Any $\overline{\text{Q}}$	4	9.5	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	2	7	ns
t <sub>PZL</sub>			3	11	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	2	7	ns
t <sub>PLZ</sub>			2	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84010013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84010013A SNJ54ALS 874BFB	<a href="#">Samples</a>
8401001KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	-55 to 125		
8401001LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401001LA SNJ54ALS874BJT	<a href="#">Samples</a>
SN54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS874BJT	<a href="#">Samples</a>
SN74ALS874BDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BDWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS874B	<a href="#">Samples</a>
SN74ALS874BNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS874BNT	<a href="#">Samples</a>
SN74ALS874BNTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS874BNT	<a href="#">Samples</a>
SN74ALS876ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS876A	<a href="#">Samples</a>
SN74ALS876ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS876A	<a href="#">Samples</a>
SN74ALS876ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS876A	<a href="#">Samples</a>
SN74ALS876ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS876ANT	<a href="#">Samples</a>
SN74ALS876ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS876ANT	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS874DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS874	<a href="#">Samples</a>
SN74AS874DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS874	<a href="#">Samples</a>
SN74AS874DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS874	<a href="#">Samples</a>
SN74AS874NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS874NT	<a href="#">Samples</a>
SN74AS874NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS874NT	<a href="#">Samples</a>
SN74AS876NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS876NT	<a href="#">Samples</a>
SN74AS876NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS876NT	<a href="#">Samples</a>
SNJ54ALS874BFK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84010013A SNJ54ALS 874BFK	<a href="#">Samples</a>
SNJ54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401001LA SNJ54ALS874BJT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS874B, SN74ALS874B :**

- Catalog: [SN74ALS874B](#)
- Military: [SN54ALS874B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS874BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS874BDWR	SOIC	DW	24	2000	367.0	367.0	45.0

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

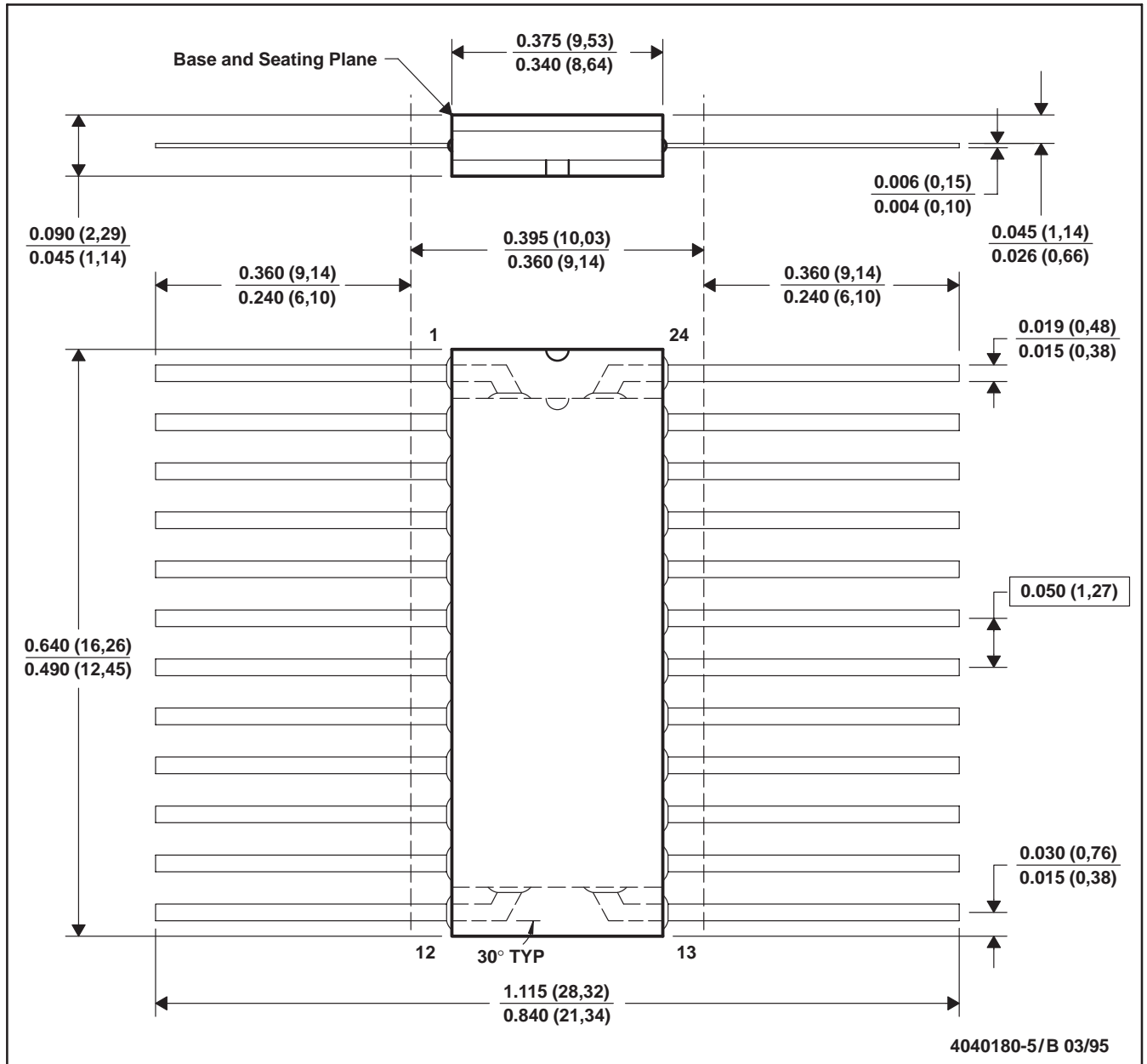
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - Index point is provided on cap for terminal identification only.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

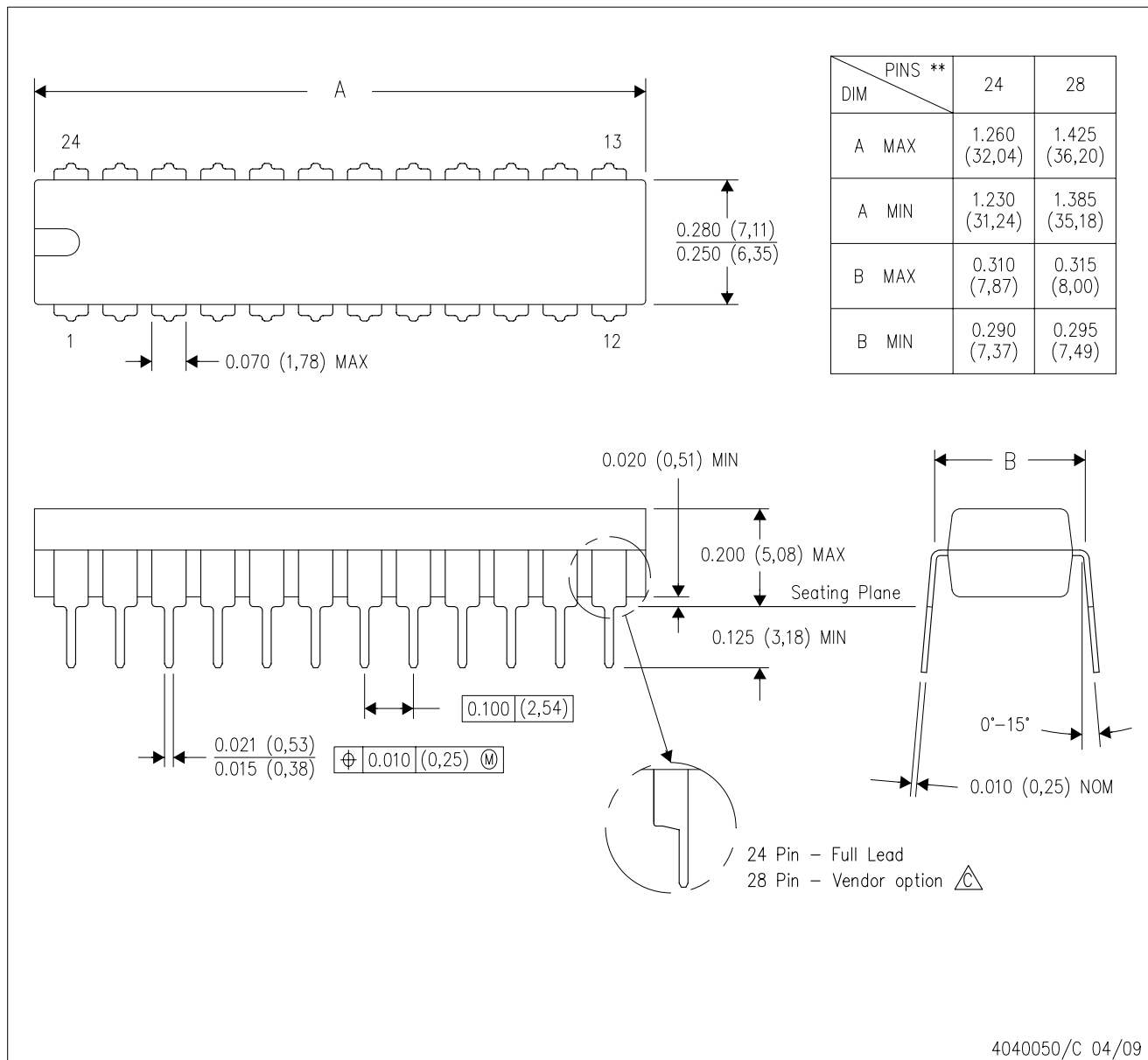
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004




# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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