



# 74F2645

## Octal Bus Transceiver with $25\Omega$ Series Resistors in the Outputs

### General Description

This device is an octal bus transceiver designed for asynchronous two-way data flow between the A and B busses and is functionally equivalent to the 'F645. The  $25\Omega$  series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, have TRI-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive ( $T/\bar{R}$ ) input. The 'F2645 is a low power version of the 'F245 with  $25\Omega$  series resistors in the outputs.

### Features

- $25\Omega$  series resistors in the outputs eliminates the need for external resistors
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Transmit/receive ( $T/\bar{R}$ ) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F2645 is a low power version of the 'F245 with  $25\Omega$  series resistors in the outputs

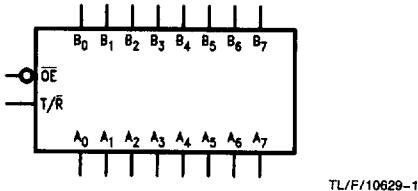
### Ordering Code:

See Section 11

Commercial	Package Number	Package Description
74F2645SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

### Logic Symbol



### Connection Diagram

Pin Assignment for SOIC

$T/\bar{R}$	1	$V_{CC}$
$A_0$	2	$\bar{OE}$
$A_1$	3	$B_0$
$A_2$	4	$B_1$
$A_3$	5	$B_2$
$A_4$	6	$B_3$
$A_5$	7	$B_4$
$A_6$	8	$B_5$
$A_7$	9	$B_6$
GND	10	$B_7$

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### Unit Loading/Fan Out:

See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{OE}$	Output Enable Input (Active LOW)	1.0/1.0	$20\ \mu A/-0.6\ mA$
$T/\bar{R}$	Transmit/Receive Input	1.0/1.0	$20\ \mu A/-0.6\ mA$
$A_0-A_7$	Side A Inputs or TRI-STATE Outputs	3.5/0.667	$70\ \mu A/-0.4\ mA$
	Side B Inputs or TRI-STATE Outputs	750/20	$-15\ mA/12\ mA$
$B_0-B_7$		3.5/0.667	$70\ \mu A/-0.4\ mA$
		750/20	$-15\ mA/12\ mA$

## Functional Description

The output enable ( $\bar{OE}$ ) is active LOW. If the device is disabled ( $\bar{OE}$  HIGH), the outputs are in the high impedance state. The transmit/receive input ( $T/\bar{R}$ ) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When  $T/\bar{R}$  is LOW, B data is sent to the A bus. If  $T/\bar{R}$  is HIGH, A data is sent to the B bus.

## Function Table

Inputs		Outputs
$\bar{OE}$	$T/\bar{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

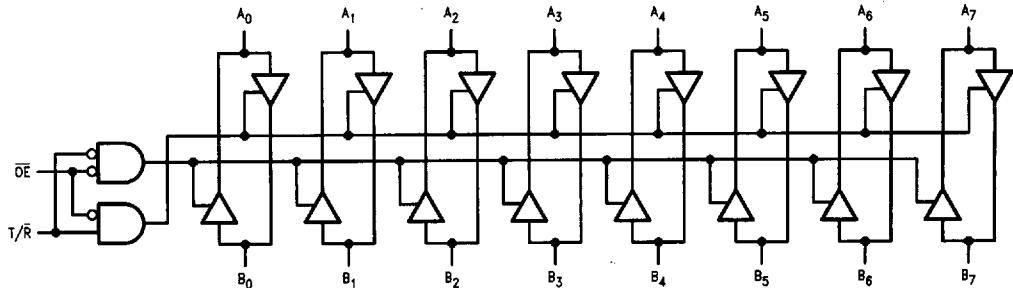
H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance state

## Logic Diagram



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## Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Plastic	-55°C to +175°C -55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output  
in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V  
**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

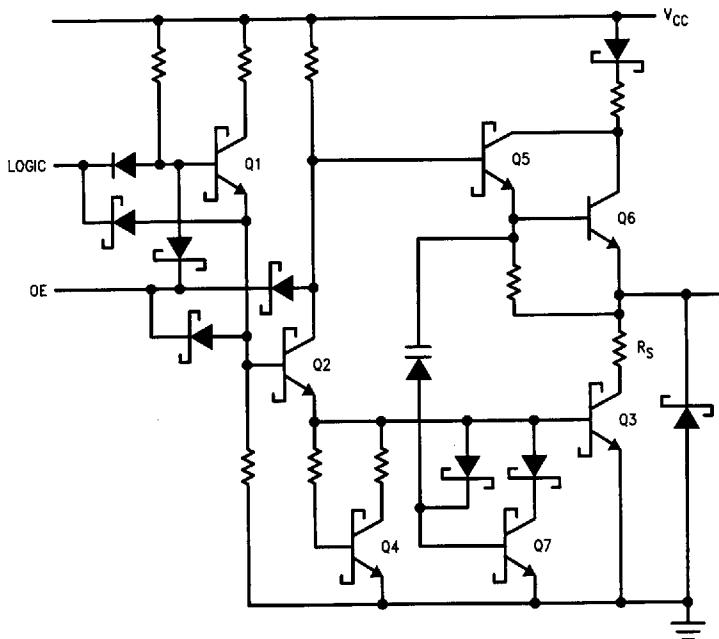
## DC Electrical Characteristics

Symbol	Parameter	74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	74F 10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	74F 10% V <sub>CC</sub>	0.50	0.75	V	Min	I <sub>OL</sub> = 1 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	74F		5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	74F		0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEx</sub>	Output HIGH Leakage Current	74F		50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100	-225		mA	Max	V <sub>OUT</sub> = 0V
I <sub>IZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25
I <sub>CCL</sub>	Power Supply Current ('F2645)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current ('F2645)			95	mA	Max	V <sub>O</sub> = HIGH Z

## 'F2645 AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.		
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$					
		Min	Typ	Max	Min	Max				
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	1.5 2.5	6.0 7.5		1.5 2.5	7.0 8.0	ns	2-3		
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	1.5 2.5	6.0 7.5		1.5 2.5	7.0 8.0	ns	2-3		
$t_{PZH}$ $t_{PZL}$	Enable Time $\bar{OE}$ Input to A Output	2.5 2.5	8.0 8.5		2.0 2.0	9.0 8.5	ns	2-5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\bar{OE}$ Input to A Output	1.5 1.0	7.0 5.5		1.0 1.0	8.0 5.5				
$t_{PZH}$ $t_{PZL}$	Enable Time $\bar{OE}$ Input to B Output	2.5 2.5	7.5 8.5		2.0 2.5	9.5 9.0	ns	2-5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\bar{OE}$ Input to B Output	1.5 1.0	6.5 6.5		1.0 1.0	7.5 6.5				

Basic FAST Circuit Showing Series Resistor Placement



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