# CY25566

# Spread Spectrum Clock Generator

## Features

- **25- to 200-MHz operating frequency range**
- **Wide range of spread selections (9)**
- **Accepts clock or crystal inputs**
- **Provides four clocks**
  - **SSCLK1a**
  - **SSCLK1b**
  - **SSCLK2**
  - **REFOUT**
- **Low-power dissipation**
  - **3.3V = 70 mW (typical @ 40 MHz, no load)**
- **Center spread modulation**
- **Low cycle-to cycle jitter**
- **16-pin SOIC package**

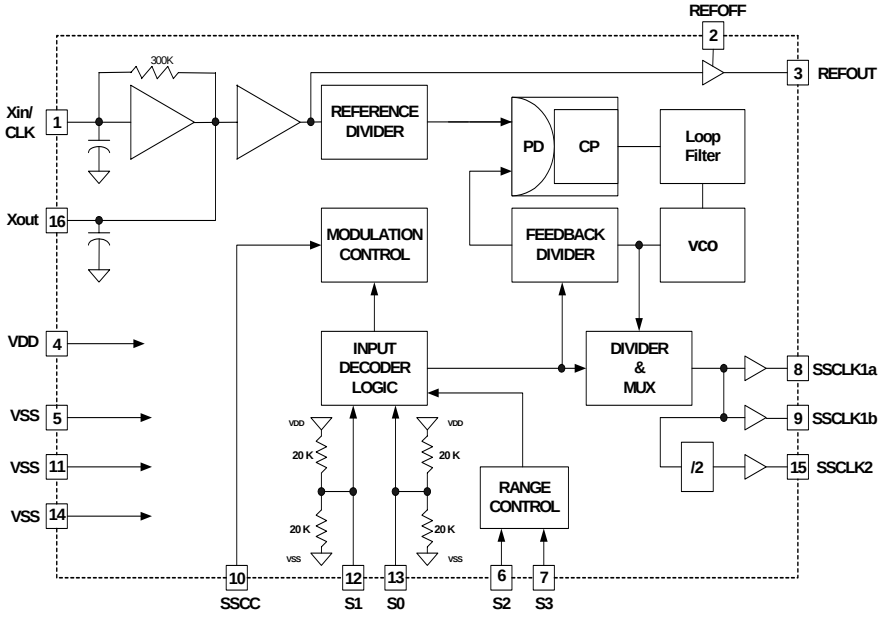
## Applications

- High-resolution VGA controllers
- LCD panels and monitors
- Printers and MFPs

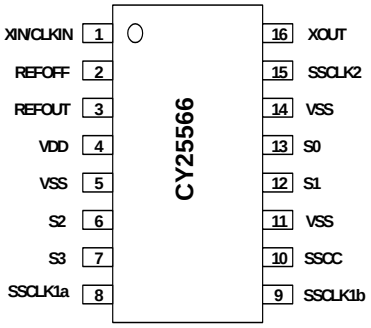
## Benefits

- Peak EMI reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

## Block Diagram




## Pin Configuration



## Pin Description

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | XIN/CLKIN | I | **Clock or Crystal connection input**. Refer to *Table 1*, *Table 2,* and *Table 3* for input frequency range selection. |
| 2 | REFOFF | I | **Input pin enables REFOUT clock at pin 3**. REFOFF 400KΩ internal pull-up resistor. Logic “0” enables REFOUT, logic “1” disables REFOUT. Default = disabled. |
| 3 | REFOUT | O | **Buffered, non-modulated output clock derived from XIN/CLKIN input frequency**. There is a 180° phase shift from XIN to REFOUT. |
| 4 | VDD | P | **Positive power supply**. Bypass to ground with 0.1-μF capacitor. |
| 5, 11, 14 | VSS | G | **Positive power supply ground**. |
| 6 | S2 | I | **VCO range control**. Refer to *Table 1*, *Table 2,* and *Table 3* for detailed programming information. Has 400-KΩ internal pull-up to $V_{DD}$. |
| 7 | S3 | I | **VCO range control**. Refer to *Table 1*, *Table 2,* and *Table 3* for detailed programming information. Has 400-KΩ internal pull-up to $V_{DD}$. |
| 8 | SSCLK1a | O | **Modulated clock output**. Pins 8 and 9 are identical but separate drivers. |
| 9 | SSCLK1b | O | **Modulated clock output**. Pins 8 and 9 are identical but separate drivers. |
| 10 | SSCC | I | **Spread Spectrum clock control (enable/disable) function**. SSCG function is enabled when input is high and disabled when input is low. Internal 400-KΩ pull-up defaults to modulation ON. |
| 12 | S1 | I | **Tri-level logic input control pin used to select frequency and bandwidth**. Frequency/bandwidth selection and tri-level logic programming details. See *Figure 2* and *Table 1*, *Table 2,* and *Table 3*. Pin 8 has internal resistor divider network to $V_{DD}$ and $V_{SS}$. |
| 13 | S0 | I | **Tri-level logic input control pin used to select frequency and bandwidth**. Frequency/bandwidth selection and tri-level logic programming details. See *Figure 2* and *Table 1*, *Table 2,* and *Table 3*. Pin 8 has internal resistor divider network to $V_{DD}$ and $V_{SS}$. |
| 15 | SSCLK2 | O | **Modulated output clock**. Frequency of SSCLK2 = SSCLK1a/2. BW% of SSCLK2 is equal to BW% of SSCLK1a/b. |
| 16 | XOUT | O | **Oscillator output pin connected to crystal**. Leave this pin unconnected if an external clock drives XIN/CLK. |

## General Description

The Cypress CY25566 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing electromagnetic interference (EMI) found in today’s high-speed digital electronic systems.

The CY25566 uses a Cypress-proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the digital clock. By frequency modulating the clock, (SSCLK1a/b and SSCLK2), the measured EMI at the fundamental and harmonic frequencies is greatly reduced. The modulated output frequency is centered on the input frequency.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The CY25566 provides four output clocks: SSCLK1a, SSCLK1b, SSCLK2, and REFOUT. SSCLK1a/b and SSCLK2 are modulated clocks and REFOUT is a buffered copy of the reference clock or oscillator. The CY25566 frequency and spread % ranges are selected by programming S0, S1, S2, and S3 digital inputs. S0 and S1 use three (3) logic states including High (H), Low (L), and Middle (M) to select one of nine available frequency and spread % ranges. Refer to *Figure 2* for details on programming three level inputs S0 and S1. See *Table 1*, *Table 2,* and *Table 3* for programming details for S2 and S3.

The CY25566 will operate over a wide range of frequencies from 25 to 200 MHz. Operation to 200 MHz is possible with the use of dual drivers at pins 8 and 9. With a wide range of selectable bandwidths, the CY25566 is a very flexible low-EMI clock. Modulation can be disabled to provide a four-output conventional clock.

The CY25566 is available in a 16-pin SOIC (150-mil.) package with a commercial operating temperature range of 0°C to 70°C.

## Output Clock Architecture

The CY25566 provides four separate output clocks: REFOUT, SSCLK1a, SSCLK1b, and SSCLK2 for use in a wide variety of applications. Each clock output is described below in detail.

### REFOUT

REFOUT is a 3.3V CMOS level non-modulated inverted copy of the clock at XIN/CLKIN. As an inverted clock, the output clock at REFOUT is 180° out of phase with the input clock at XIN/CLKIN. Placing a high(1) logic state of REFOFF, pin 2, will disable the REFOUT clock. When REFOUT is disabled, REFOUT, pin 3 is at a low(0) logic state.

### SSCLK1a/b

SSCLK1a and SSCLK1b are spread spectrum clock outputs used for the purpose of reducing EMI in digital systems. SSCLK1a and SSCLK1b can be connected in several different ways to provide flexibility in application designs. Each clock can drive separate nets with a capacitative load up to 15 pF each or connected together to provide drive to a single net with a capacitative load as high as 33 pF. When both clocks are connected together, the CY25566 is capable of driving 3.3V CMOS-compatible clocks to frequencies as high as 200 MHz. If one clock output is not connected to a load, negligible EMI will be generated at the unused pin because there is no current being driven. The frequency and bandwidth of SSCLK1a and SSCLK1b is programmed by the logic states presented to S2 and S3. The frequency multiplication at SSCLK1a and SSCLK1b is either 1X or 2X, controlled by S2 and S3. The modulated output clock SSCLK1 is provided at pins 8 and 9 with each pin having separate but identical drivers. Refer to *Figure 1* below.

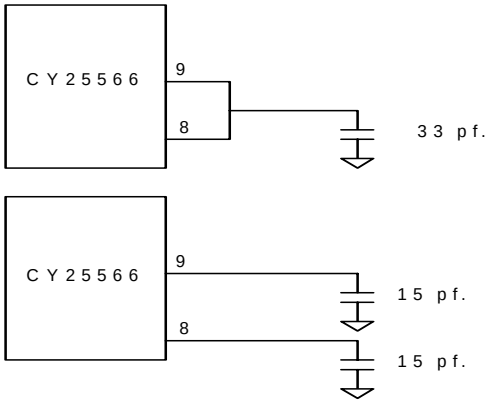



**Figure 1. SSCLK1a/b Driver Configurations**

### SSCLK2

SCLK2 is a Spread Spectrum Clock with a frequency half that of the SSCLK1a clock frequency. When SSCLK1a is programmed to provide a 2.5% modulated clock at 1X times the reference clock, 40 MHz for example, the frequency of SSCLK2 will be 20 MHz with a BW of 2.5%. Note that by programming the frequency of SSCLK1a to 2X, the frequency of SSCLK2 will be 1X times the reference clock frequency.

## Control Logic Structures

The CY25566 has six input control pins for programming VCO range, BW %, Mod ON/OFF and REFOUT ON/OFF. These programmable control pins are described below.

### REFOFF

The output clock REFOUT can be enabled or disabled by controlling the state of REFOFF. When REFOFF is at a logic low(0) state, REFOUT is enabled and the reference clock frequency is present at pin 3. When REFOFF is at a logic high state (1), REFOUT is disabled and is set to a logic low state on pin 3. REFOFF has a 400-KW internal pull-up resistor to $V_{DD}$.

### S0 and S1 (Tri-level Inputs)

S0 and S1 are used to program the frequency range and bandwidth of the modulated output clocks SSCLK1a/b and SSCLK2. S0 and S1 of the CY25566 are designed to sense three different analog levels. With this tri-level structure, the CY25566 is able to detect 9 different logic states. Refer to tables 5, 6 and 7 for the results of each of these 9 states. The level of each state is defined as follows:

Logic State “0” is a voltage that is between 0 and 0.15 × $V_{DD}$V.

Logic State “M” is a voltage between 0.4 × $V_{DD}$ and 0.6 × $V_{DD}$V.

Logic State “1” is a voltage between 0.85 × $V_{DD}$ and $V_{DD}$.

*Figure 2* illustrates how to program tri-level logic.

### S2 and S3

S2 and S3 are used to program the CY25566 into different frequency ranges and multipliers. The CY25566 operates over a frequency range of 25 to 200 MHz and a 1X or 2X multiplication of the reference frequency. S2 and S3 are binary logic inputs and each has a 400 K W pull-up resistor to $V_{DD}$. See *Table 1*, *Table 2*, and *Table 3* for programming details.

## SSCC

SSCC is an input control pin that enables or disables SSCG modulation of the output clock at SSCLK1a/b and SSCLK2. Disabling modulation is a method of comparing radiated EMI in a product with SSCG turned on or off.

The CY25566 can be used as a conventional low jitter multiple output clock when SSCC is set to low (0). SSCC has a 400-KW internal pull-up resistor. Logic high (1) = Modulation ON, logic low (0) = Modulation OFF. Default is modulation ON.

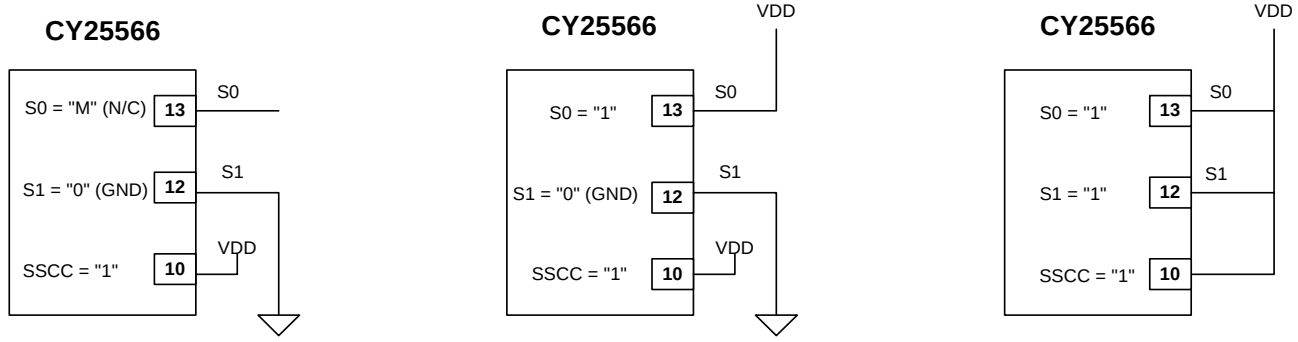



**Figure 2.**

## Modulation Rate

Spread Spectrum clock generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmod. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. The CY25566 utilizes two different modulation rate dividers, depending on the range selected on S2 and S3 digital control inputs. Refer to the example below.

| S3, S2 | CDiv | Output Frequency |
|---|---|---|
| 0,0 | 1166 | 1X |
| 0,1 | 1166 | 2X |
| 1,0 | 2332 | 1X |
| 1,1 | N/A | N/A |

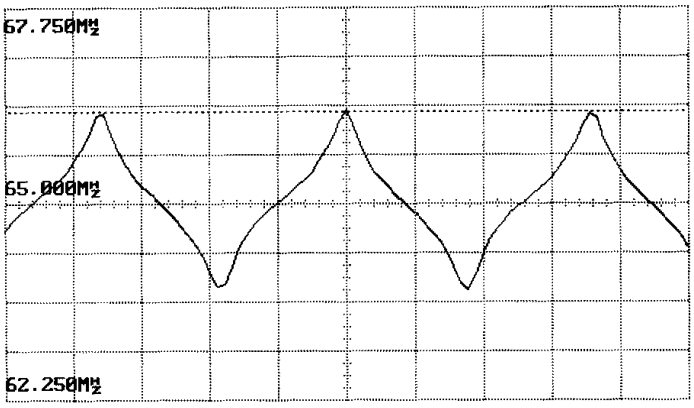
Example:
Device = CY25566
Fin = 65 MHz
Range = S3 = 0, S2 = 1, S0 = 0
Then: modulation rate = Fmod = 65 MHz/1166 = 55.7 kHz

The CY25566 has three frequency groups to select from. Each combination of frequency and bandwidth can be selected by programming the input control lines, S0–S3, to the proper logic state.

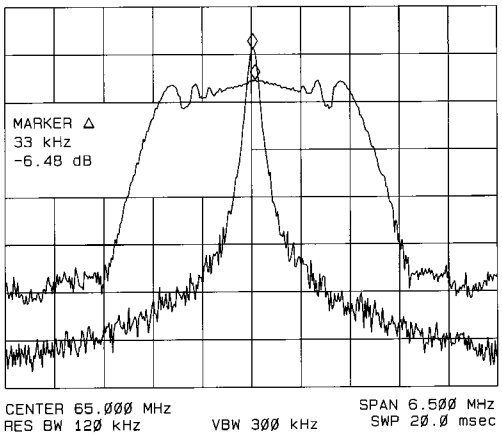
Group 1 is the 1X low-frequency range and operates from 25 to 100 MHz.

Group 2 is the 1X high-frequency range and operates from 50 to 200 MHz.

Group 3 is the 2X low frequency range and operates from 25 to 50 MHz and 50 to 100 MHz output.




Modulation Profile

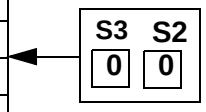



Spectrum Analyzer

**Figure 3. SSCG Clock, CY25566, 65 MHz**

**Table 1. Frequency and Bandwidth Selection Chart (Group 1)(Low Frequency (1x) Selection Chart)**

| 25–50 MHz (Low Range) | | | | | |
|---|---|---|---|---|---|
| **XIN/CLK (MHz)** | **S1 = M S0 = M** | **S1 = M S0 = 0** | **S1 = 1 S0 = 0** | **S1 = 0 S0 = 0** | **S1 = 0 S0 = M** |
| 25–35 | 4.3 | 3.8 | 3.4 | 2.9 | 2.8 |
| 35–40 | 3.9 | 3.5 | 3.1 | 2.5 | 2.4 |
| 40–45 | 3.7 | 3.3 | 2.8 | 2.4 | 2.3 |
| 45–50 | 3.4 | 3.1 | 2.6 | 2.2 | 2.1 |
| **50–100 MHz (High Range)** | | | | | |
| **XIN/CLK (MHz)** | **S1 = 1 S0 = M** | **S1 = 0 S0 = 1** | **S1 = 1 S0 = 1** | **S1 = M S0 = 1** | |
| 50–60 | 2.9 | 2.1 | 1.5 | 1.2 | |
| 60–70 | 2.8 | 2.0 | 1.4 | 1.1 | |
| 70–80 | 2.6 | 1.8 | 1.3 | 1.1 | |
| 80–100 | 2.4 | 1.7 | 1.2 | 1.0 | |



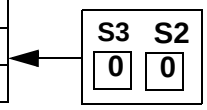
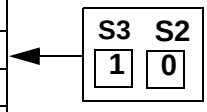




**Table 2. Frequency and Bandwidth Selection Chart (Group 2)(High Frequency (1x) Selection Chart)**

| 50–100 MHz (Low Range) | | | | | |
|---|---|---|---|---|---|
| **XIN/CLK (MHz)** | **S1 = M S0 = M** | **S1 = M S0 =0** | **S1 = 1 S0 = 0** | **S1 = 0 S0 = 0** | **S1 = 0 S0 = M** |
| 50–60 | 4.2 | 3.8 | 3.2 | 2.8 | 2.7 |
| 60–70 | 4.0 | 3.6 | 3.1 | 2.6 | 2.5 |
| 70–80 | 3.8 | 3.4 | 2.9 | 2.5 | 2.4 |
| 80–100 | 3.5 | 3.1 | 2.7 | 2.2 | 2.1 |
| **100–200 MHz (High Range)** | | | | | |
| **XIN/CLK (MHz)** | **S1 = 1 S0 = M** | **S1 = 0 S0 = 1** | **S1 = 1 S0 = 1** | **S1 = M S0 = 1** | |
| 100–120 | 3.0 | 2.4 | 1.6 | 1.3 | |
| 120–130 | 2.7 | 2.1 | 1.4 | 1.1 | |
| 130–140 | 2.6 | 2.0 | 1.3 | 1.1 | |
| 140–150 | 2.6 | 2.0 | 1.3 | 1.1 | |
| 150–160 | 2.5 | 1.8 | 1.2 | 1.0 | |
| 160–170 | 2.4 | 1.8 | 1.2 | 1.0 | |
| 170–180 | 2.4 | 1.8 | 1.2 | 1.0 | |
| 180–190 | 2.3 | 1.7 | 1.1 | 0.9 | |
| 190–200 | 2.3 | 1.6 | 1.1 | 0.9 | |



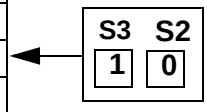
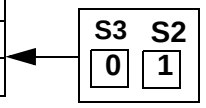




**Table 3. Frequency and Bandwidth Selection Chart (Group 3)(Low Frequency (2x) Selection Chart)**

| 25–50 MHz (Low Range, 2X) | | | | | | |
|---|---|---|---|---|---|---|
| **XIN/CLK (MHz)** | **SSCLK1 (MHz)** | **S1 = M S0 = M** | **S1 = M S0 = 0** | **S1 = 1 S0 = 0** | **S1 = 0 S0 = 0** | **S1 = 0 S0 = M** |
| 25–35 | 50-70 | 4.0 | 3.5 | 3.0 | 2.6 | 2.5 |
| 35–40 | 70-80 | 3.8 | 3.3 | 2.9 | 2.4 | 2.3 |
| 40–45 | 80-90 | 3.5 | 3.1 | 2.7 | 2.2 | 2.1 |
| 45–50 | 90-100 | 3.3 | 2.9 | 2.5 | 2.1 | 2.0 |



## Application Schematic

In this example, the CY25566 is being driven by a 75-MHz reference clock.

S0 = 0 and S1 = 0 are programmed to select a BW of 2.5%. (Refer to *Table 1* and *2*.)

S2 = 0 and S3 = 1 are programmed to select the Group 2 range.

$V_{DD}$ = 3.30 VDC.

SSCLK1a = 75 MHz @ 2.5% center spread modulation.

SSCLK1b = 75 MHz @ 2.5% center spread modulation.

SSCLK 2 = 37.5 MHz @ 2.5% center spread modulation.

REFOUT = 37.5 MHz non-modulated clock.

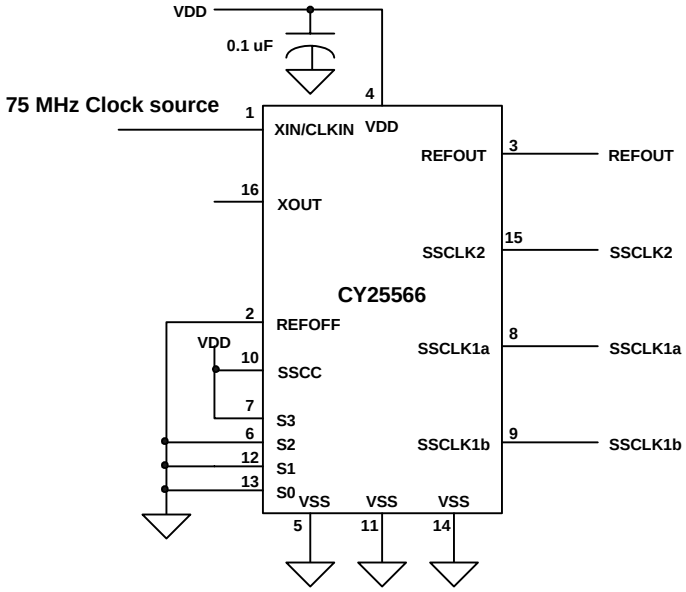



**Figure 4. Application Schematic**

## Absolute Maximum Ratings[1, 2]

Supply Voltage ($V_{DD}$: .....+6V

Operating Temperature: .....0°C to 70°C

Storage Temperature .....–65°C to +150°C

**Table 4. DC Electrical Characteristics** $V_{DD}$ = 3.3V, Temp. = 25°C, unless otherwise noted

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Range | ±10% | 2.97 | 3.3 | 3.63 | V |
| $V_{INH}$ | Input High Voltage | S0 and S1 only. | $0.85V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V |
| $V_{INM}$ | Input Middle Voltage | S0 and S1 only. | $0.40V_{DD}$ | $0.50V_{DD}$ | $0.60V_{DD}$ | V |
| $V_{INL}$ | Input Low Voltage | S0 and S1 only. | 0.0 | 0.0 | $0.15V_{DD}$ | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = 6 ma, SSCLKa | 2.4 | | | V |
| $V_{OH2}$ | Output High Voltage | $I_{OH}$ = 20 ma, SSCLKb | 2.0 | | | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OH}$ = 6 ma, SSCLKa | | | 0.4 | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OH}$ = 20 ma, SSCLKb | | | 1.2 | V |
| $C_{in1}$ | Input Capacitance | Xin/CLK (Pin 1) | 3 | 4 | 5 | pF |
| $C_{in2}$ | Input Capacitance | Xout (Pin 8) | 6 | 8 | 10 | pF |
| $C_{in2}$ | Input Capacitance | All input pins except 1. | 3 | 4 | 5 | pF |
| $I_{DD1}$ | Power Supply Current | FIN = 40 MHz,15 pF@all outputs | | 27 | 32 | mA |
| $I_{DD1}$ | Power Supply Current | FIN = 40 MHz, No Load | | 21 | 28 | mA |
| $I_{DD2}$ | Power Supply Current | FIN = 165 MHz,15 pF@all outputs | | 68 | 80 | mA |
| $I_{DD2}$ | Power Supply Current | FIN = 165 MHz, No Load | | 48 | 60 | mA |

**Table 5. Electrical Timing Characteristics** $V_{DD}$ = 3.3V, T = 25°C and $C_L$ = 15 pF, unless otherwise noted. Rise/Fall @ 0.4–2.4V, Duty@1.5V

| Parameter | Description | Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CLKFR}$ | Input Clock Frequency Range | Non-crystal, 3.0V Pk–Pk ext. source | 25 | | 200 | MHz |
| $t_{RISE(a)}$ | Clock Rise Time | SSCLK1a or SSCLK1b, Freq = 100 MHz | 1.0 | 1.3 | 1.6 | ns |
| $t_{FALL(a)}$ | Clock Fall Time | SSCLK1a or SSCLK1b, Freq = 100 MHz | 1.0 | 1.3 | 1.6 | ns |
| $t_{RISE(a+b)}$ | Clock Rise Time | SSCLK1(a+b), CL = 33 pF, 100 MHz | 1.2 | 1.5 | 1.8 | ns |
| $t_{FALL(a+b)}$ | Clock Fall Time | SSCLK1(a+b), CL = 33 pF, 100 MHz | 1.2 | 1.5 | 1.8 | ns |
| $t_{RISE(a+b)}$ | Clock Rise Time | SSCLK1(a+b), CL = 33 pF, 200 MHz | 1.1 | 1.4 | 1.7 | ns |
| $t_{FALL(a+b)}$ | Clock Fall Time | SSCLK1(a+b), CL = 33 pF, 200 MHz | 1.1 | 1.4 | 1.7 | ns |
| $t_{RISE(REF)}$ | Clock Rise Time | REFOUT, Pin 3, CL = 15 pF, 50 MHz | 1.0 | 1.3 | 1.6 | ns |
| $t_{FALL(REF)}$ | Clock Fall Time | REFOUT, Pin 3, CL = 15 pF, 50 MHz | 1.0 | 1.3 | 1.6 | ns |
| $D_{TYin}$ | Input Clock Duty Cycle | XIN/CLK (Pin) | 30 | 50 | 70 | % |
| $D_{TYout}$ | Output Clock Duty Cycle | SSCLK1a/b (Pin 8 and 9) | 45 | 50 | 55 | % |
| $C_{CJ1}$ | Cycle-to-Cycle Jitter | F = 100 MHz, SSCLK1a/b CL = 33 pF | | 300 | 400 | ps |
| $C_{CJ2}$ | Cycle-to-Cycle Jitter | F = 200 MHz, SSCLK1a/b CL = 33 pF | | 500 | 600 | ps |
| REFOUT | Refout Frequency Range | CL = 15 pF | 25 | | 108 | MHz |

**Note:**

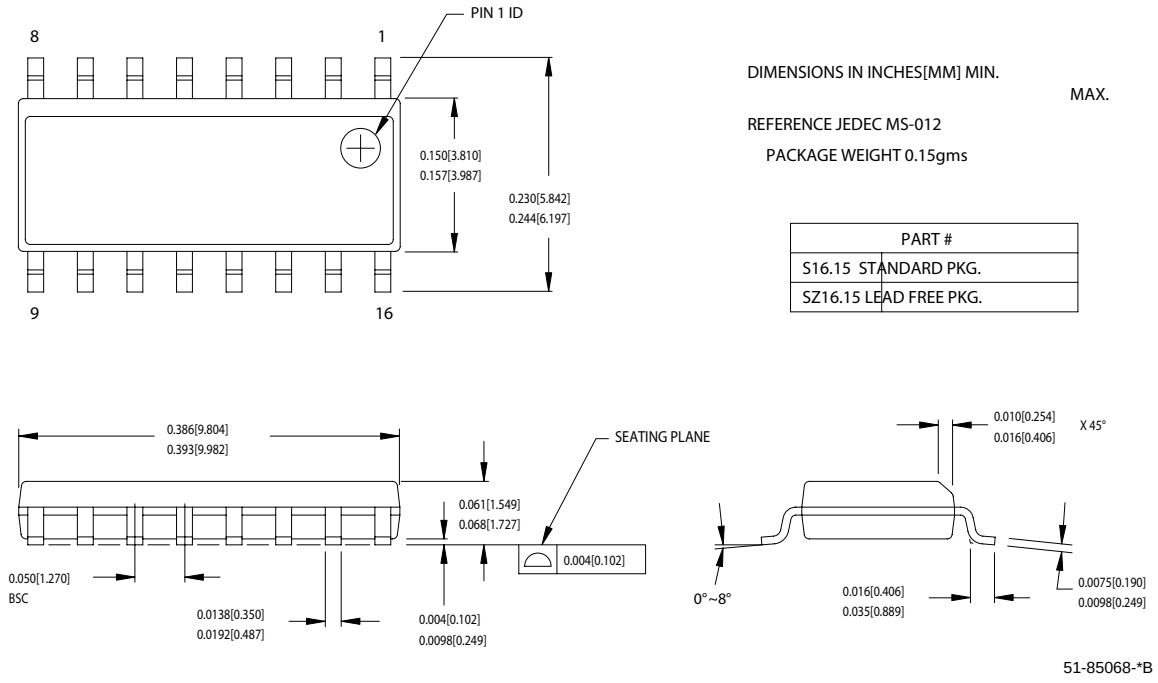
1. Operation at any Absolute Maximum Rating is not implied.
2. **Single Power Supply:** The voltage on any input or I/O pin cannot exceed the power pin during power-up.

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY25566SC | 16-pin SOIC | Commercial, 0° to 70°C |
| CY25566SCT | 16-pin SOIC–Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

**16-Lead (150-Mil) SOIC S16.15**

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| Document Title:CY25566 Spread Spectrum Clock Generator<br>Document Number: 38-07429 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 115771 | 07/01/02 | OXC | New Data Sheet |
| *A | 122705 | 12/30/02 | RBI | Added power up requirements to maximum ratings information. |
| *B | 404070 | See ECN | RGL | Minor Change: Typo error on table 1, column 2 , S0 = 0 (not M) |