ADVANCE INFORMATION

CY14B256L

256-Kbit (32K x 8) nvSRAM

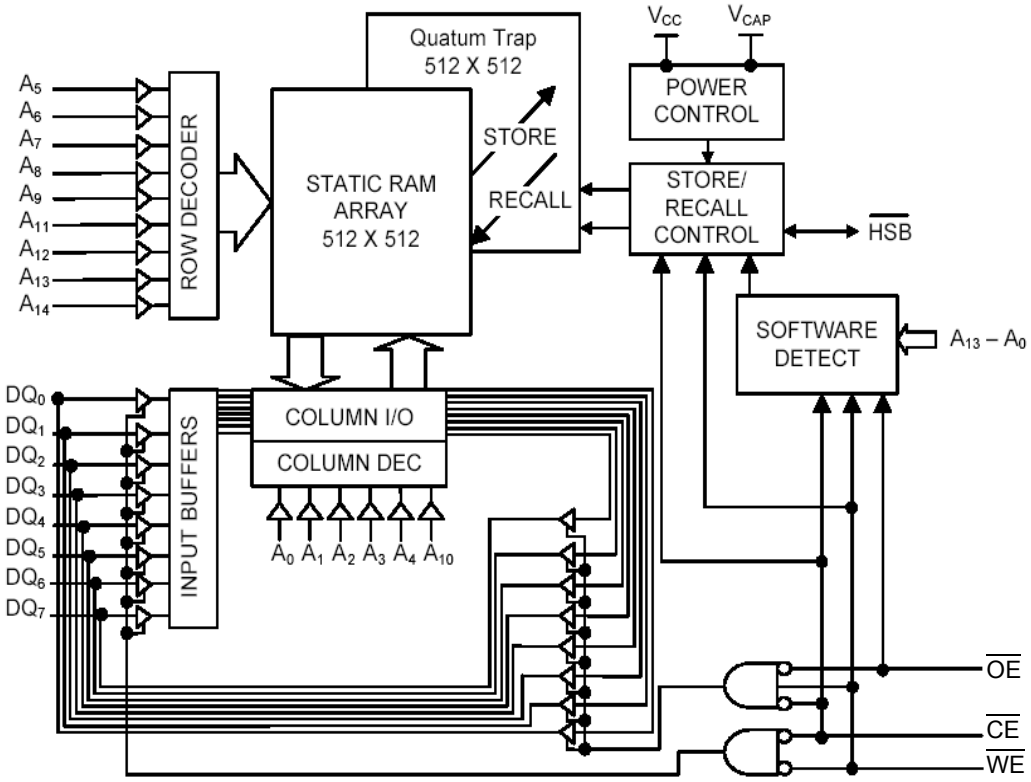
Features

- **25 ns, 35 ns and 45 ns Access Times**
- **"Hands-off" Automatic *STORE* on Power Down with only a small capacitor**
- ***STORE* to QuantumTrap™ Nonvolatile Elements is initiated by Software, device pin, or Autostore™ on Power-down**
- ***RECALL* to SRAM Initiated by Software or Power-up**
- **Unlimited *READ, WRITE* and *RECALL* Cycles**
- **10 mA Typical I_{CC} at 200 ns Cycle Time**
- **1,000,000 *STORE* Cycles to QuantumTrap**
- **100-Year Data Retention**
- **Single 3V Operation +20%, -10%**
- **Commercial and Industrial Temperature**
- **SOIC and SSOP Packages**
- **RoHS Compliance**

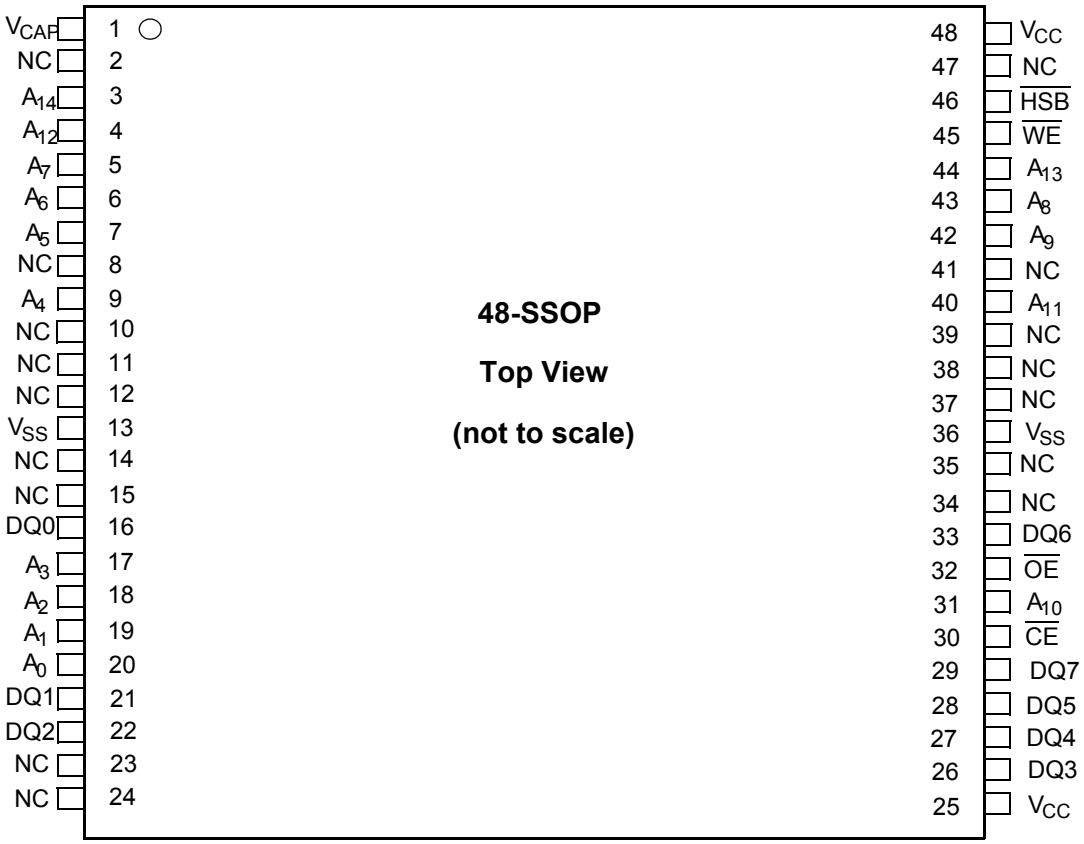
Functional Description

The Cypress CY14B256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

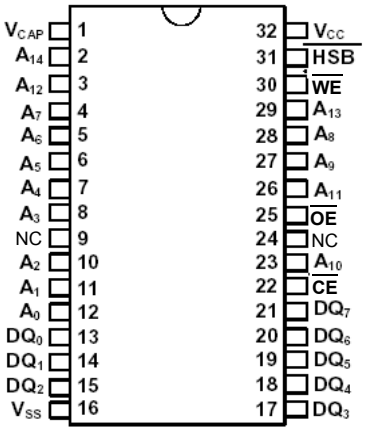
Logic Block Diagram



Pin Configurations



32-Lead SOIC



Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{14}	Input	**Address Inputs used to select one of the 131,072 bytes of the nvSRAM**.
DQ0-DQ7	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	No Connect	**No Connects**. This pin is not connected to the die.
$\overline{WE}$	Input	**Write Enable Input, active LOW**. When selected LOW, enables data on the I/O pins to be written to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tri-state.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	Power Supply	**Power Supply inputs to the device**.
$\overline{HSB}$	Input/Output	**Hardware Store Busy**. When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull-up resistor keeps this pin high if not connected. (Connection Optional)
V_{CAP}	Power Supply	**Autostore™ Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The CY14B256L nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14B256L supports unlimited reads and writes just like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 1 million STORE operations.

SRAM Read

The CY14B256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are low while $\overline{WE}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AA} (READ cycle #1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs will be valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought high, or $\overline{WE}$ or $\overline{HSB}$ is brought low.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes high at the end of the cycle. The data on the common I/O pins $I/O_{0–7}$ will be written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. It is recommended that $\overline{OE}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left low, internal circuitry will turn off the output buffers t_{HZWE} after $\overline{WE}$ goes low.

AutoStore Operation

The CY14B256L stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by $\overline{HSB}$, Software Store, activated by an address sequence, and AutoStore, on device power down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B256L.

During normal operation, the device will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC Characteristics table for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull-up should be placed on $\overline{WE}$ to hold it inactive during power-up.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an AutoStore cycle is in progress.

Hardware STORE ($\overline{HSB}$) Operation

The CY14B256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin can be used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the CY14B256L will conditionally initiate a STORE operation after t_{DELAY}. An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last

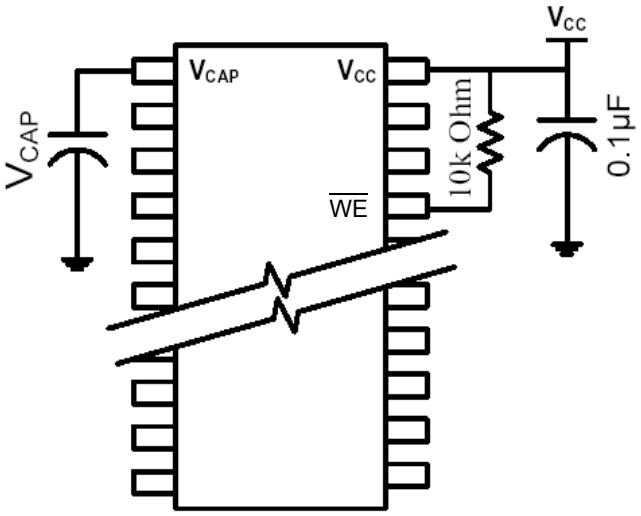


Figure 1. AutoStore™ Mode

STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when HSB is driven low by any means are given time to complete before the STORE operation is initiated. After HSB goes low, the CY14B256L will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when HSB is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after HSB goes low will be inhibited until HSB returns high.

During any STORE operation, regardless of how it was initiated, the CY14B256L will continue to drive the HSB pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14B256L will remain disabled until the HSB pin returns high.

If HSB is not used, it should be left unconnected.

Hardware RECALL (Power-up)

During power-up, or after any low-power condition (V_{CC} < V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{HRECALL}$ to complete.

Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B256L software STORE cycle is initiated by executing sequential CE-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence may be clocked with CE-controlled READs or OE-controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that OE be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Software RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE-controlled READ operations must be performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

Data Protection

The CY14B256L protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} < V_{SWITCH}. If the CY14B256L is in a WRITE mode (both CE and WE low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power-up or brown-out conditions.

Noise Considerations

The CY14B256L is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs,

careful routing of power, ground, and signals will reduce circuit noise.

Low Average Active Power

CMOS technology provides the CY14B256L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. *Figure 2* shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC} = 3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B256L depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITEs.
4. The operating temperature.
5. The V_{CC} level.
6. I/O loading.

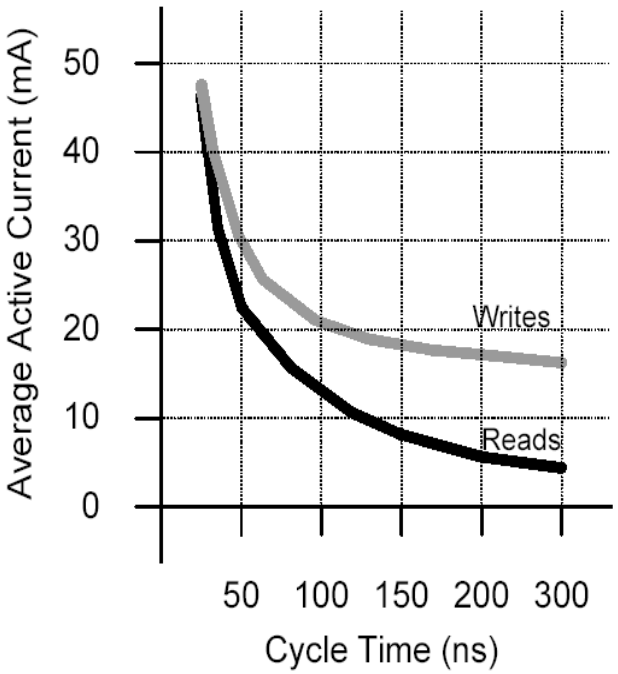


Figure 2. Current vs. Cycle Time

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND..... –0.5V to 4.1V

Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage ..... –0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +240°C

Output Short Circuit Current[1] ..... 15 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Table 1. Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

Shaded area contains Advance Information

DC Electrical Characteristics Over the Operating Range (V_{CC} = 2.7V to 3.6V)[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0mA.	Commercial		65 55 50	mA mA mA
			Industrial		70 60 55	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns, 3V, 25°C typical	$\overline{WE}$ > (V_{CC} – 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			3	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE}$ > (V_{CC} – 0.2). All others V_{IN} < 0.2V or > (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0MHz.			3	mA
I_{IX}	Input Leakage Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$		-1	+1	µA
I_{OZ}	Off-State Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > V_{IH}		-1	+1	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 5V Rated		17	120	µF

Table 2. Capacitance[3]

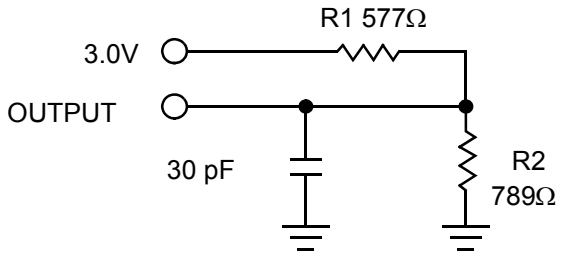
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

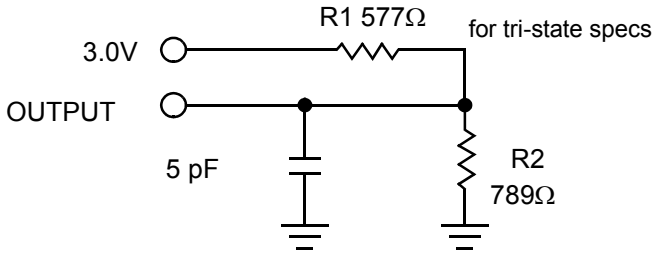
Notes:
1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and V_{CC} = 3V. Not 100% tested.
3. These parameters are guaranteed but not tested.

Table 3. Thermal Resistance[3]

Parameter	Description	Test Conditions	48-SSOP	32-SOIC	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

AC Test Loads





AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times (10% - 90%) ..... ≤5ns
Input and Output Timing Reference Levels 1.5V

Table 4. AC Switching Characteristics

Parameters		Description	CY14B256L-25		CY14B256L-35		CY14B256L-45		Unit
Cypress Parameter	Alt. Parameter		Min.	Max.	Min.	Max.	Min.	Max.	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
t_{RC}[4]	t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}[5]	t_{AA}	Address Access Time		25		35		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
t_{OHA}[5]	t_{OH}	Output Hold After Address Change	3		3		3		ns
t_{LZCE}[6]	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE}[6]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE}[6]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE}[6]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU}[3]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD}[3]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DW}	Data Set-Up to End of Write	10		12		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Set-Up to End of Write	20		25		30		ns
t_{SA}	t_{AS}	Address Set-Up to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE}[6,7]	t_{WZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE}[6]	t_{OW}	Output Active after End of Write	3		3		3		ns

Notes:
4. $\overline{WE}$ must be HIGH during SRAM Read Cycles.
5. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
6. Measured ±200mV from steady state output voltage.
7. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low,the outputs remain in the High Impedance State

Table 5. AutoStore/Power-Up RECALL

Parameters	Description	CY14B256L		Units
$t_{HRECALL}$[8]	Power-Up RECALL Duration		20	ms
t_{STORE}[9]	STORE Cycle Duration		12.5	ms
V_{SWITCH}	Low Voltage Trigger Level	2.55	2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		µs

Table 6. Software Controlled STORE/RECALL Cycle[10,11]

Parameters	Description	CY14B256L-25		CY14B256L-35		CY14B256L-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{AS}	Address Set-Up Time	0		0		0		ns
t_{CW}	Clock Pulse Width	20		25		30		ns
t_{GLAX}	Address Hold Time	20		20		20		ns
t_{RECALL}	RECALL Duration		60		60		60	µs

Table 7. Hardware STORE Cycle

Parameters	Description	CY14B101L		Units
		Min	Max	
t_{DELAY}[12]	Time allowed to complete SRAM Cycle	1		µs
t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{HLBL}	Hardware STORE Low to STORE Busy		300	ns

Switching Waveforms

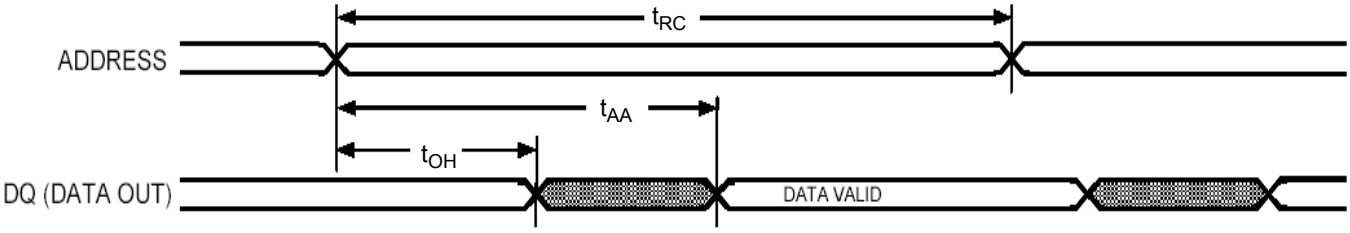


Figure 3. SRAM Read Cycle #1: Address Controlled[4, 5, 13]

Notes:
8. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
9. If an SRAM Write has not taken place since the last non-volatile cycle, no STORE will take place.
10. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled READs.
11. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.
12. Read and Write cycles in progress before $\overline{HSB}$ are given this amount of time to complete.
13. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

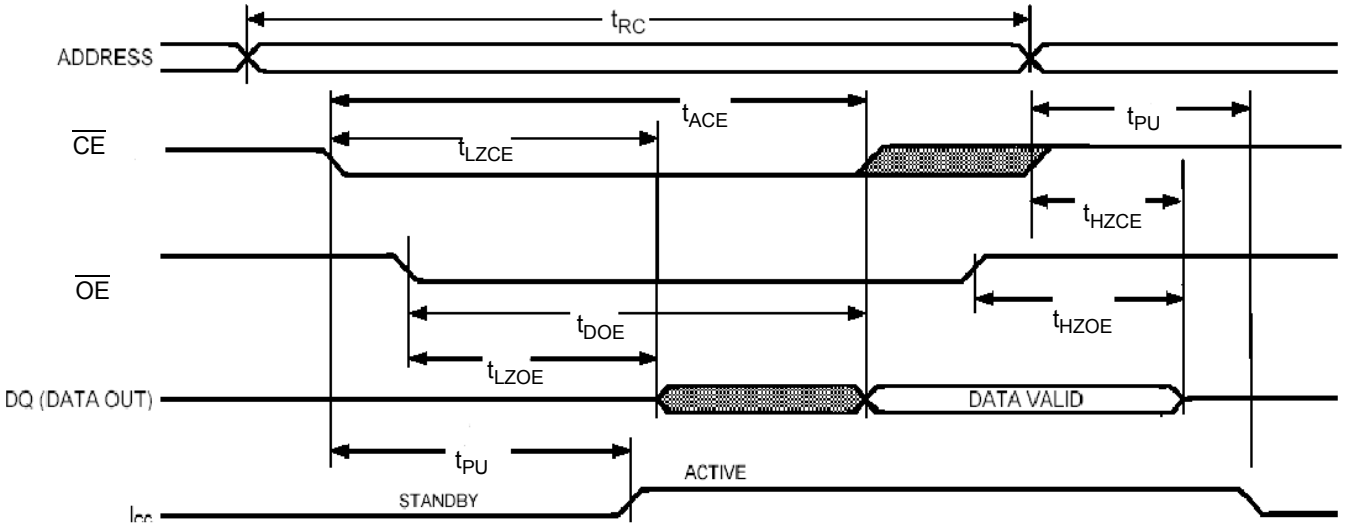


Figure 4. SRAM Read Cycle #2: $\overline{CE}$ and $\overline{OE}$ Controlled[4,13]

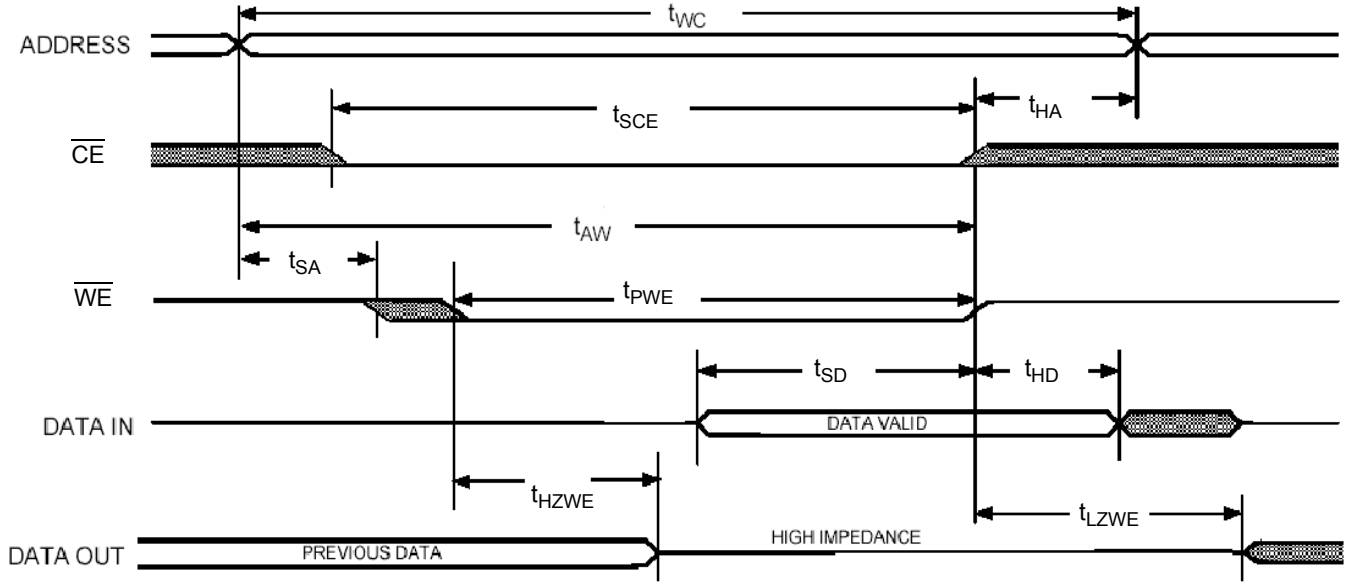


Figure 5. SRAM Write Cycle #1: $\overline{WE}$ Controlled[13,14]

Note:
14. $\overline{CE}$ or $\overline{WE}$ must be > V_{IH} during address transitions.

Switching Waveforms (continued)

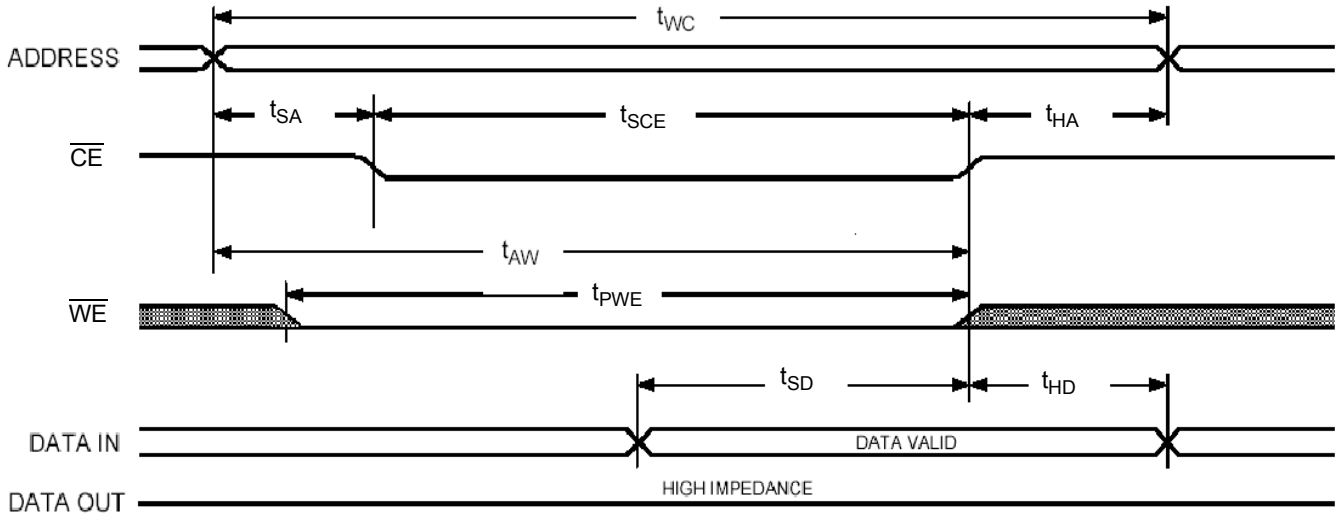


Figure 6. SRAM Write Cycle #2: $\overline{CE}$ Controlled

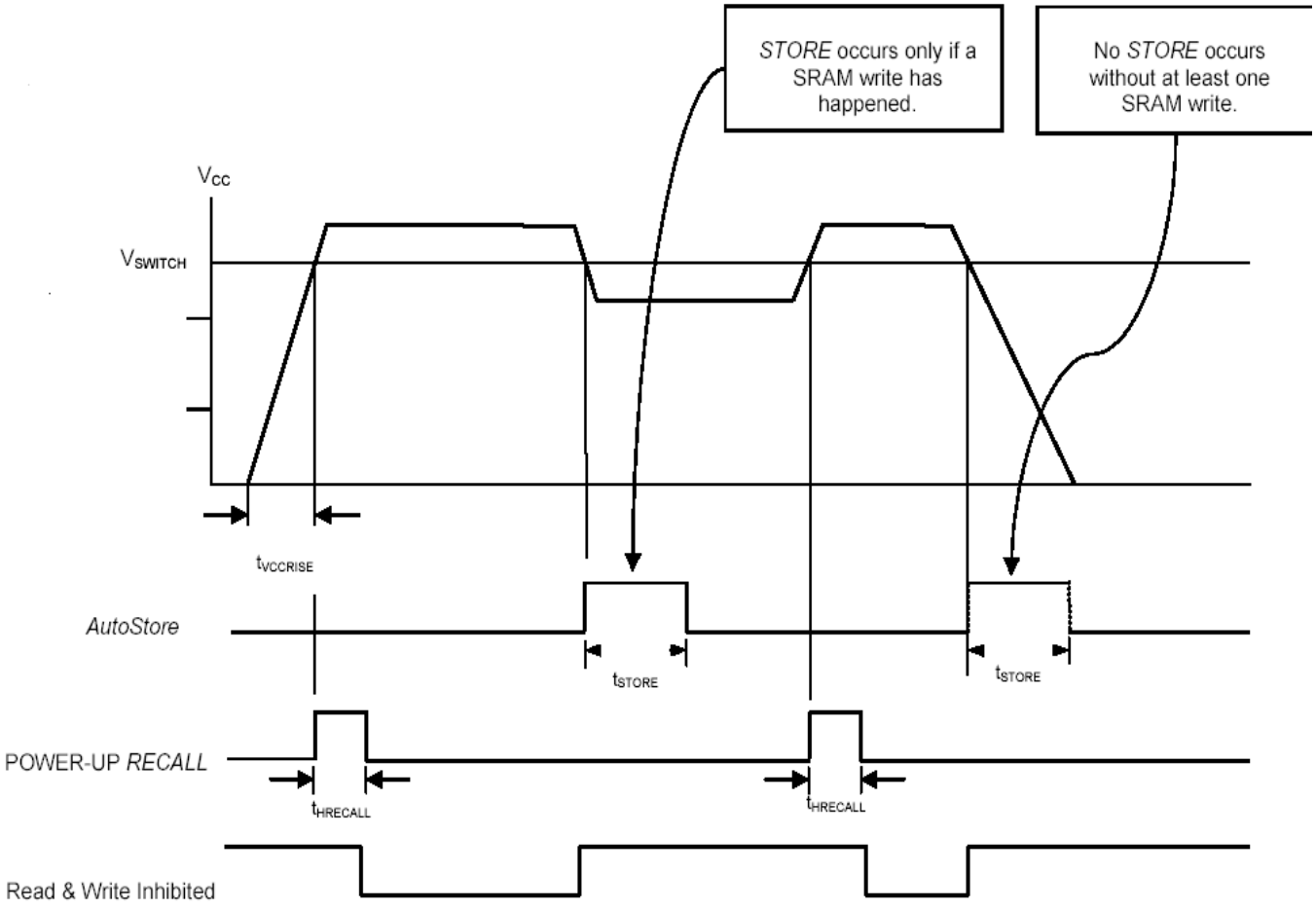


Figure 7. AutoStore/Power-Up RECALL

Switching Waveforms (continued)

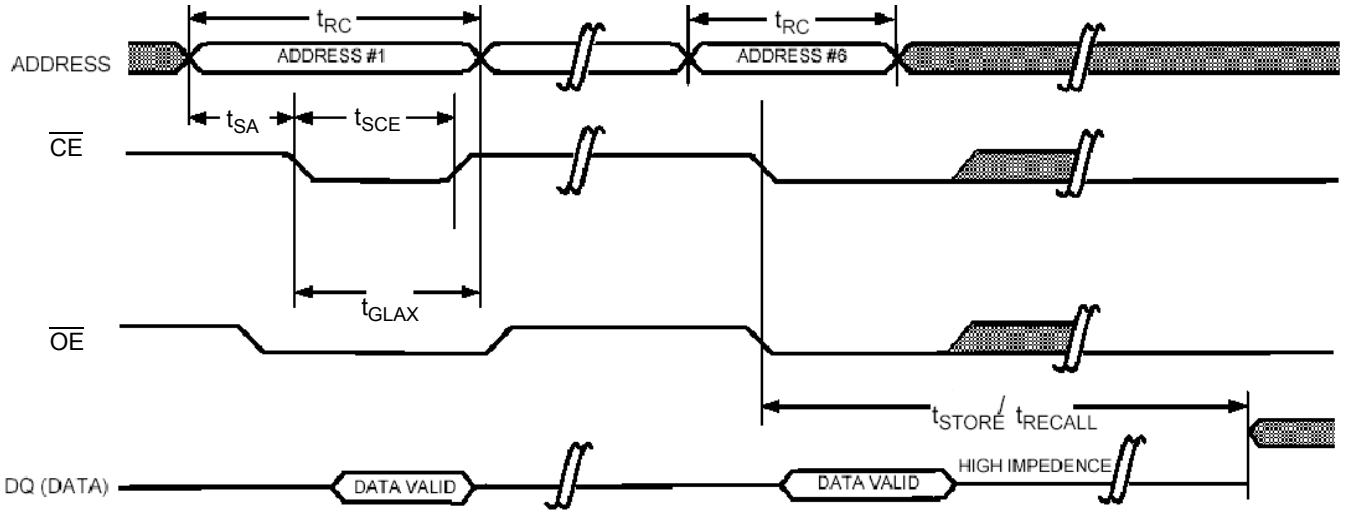


Figure 8. $\overline{CE}$-controlled Software STORE/RECALL Cycle[11]

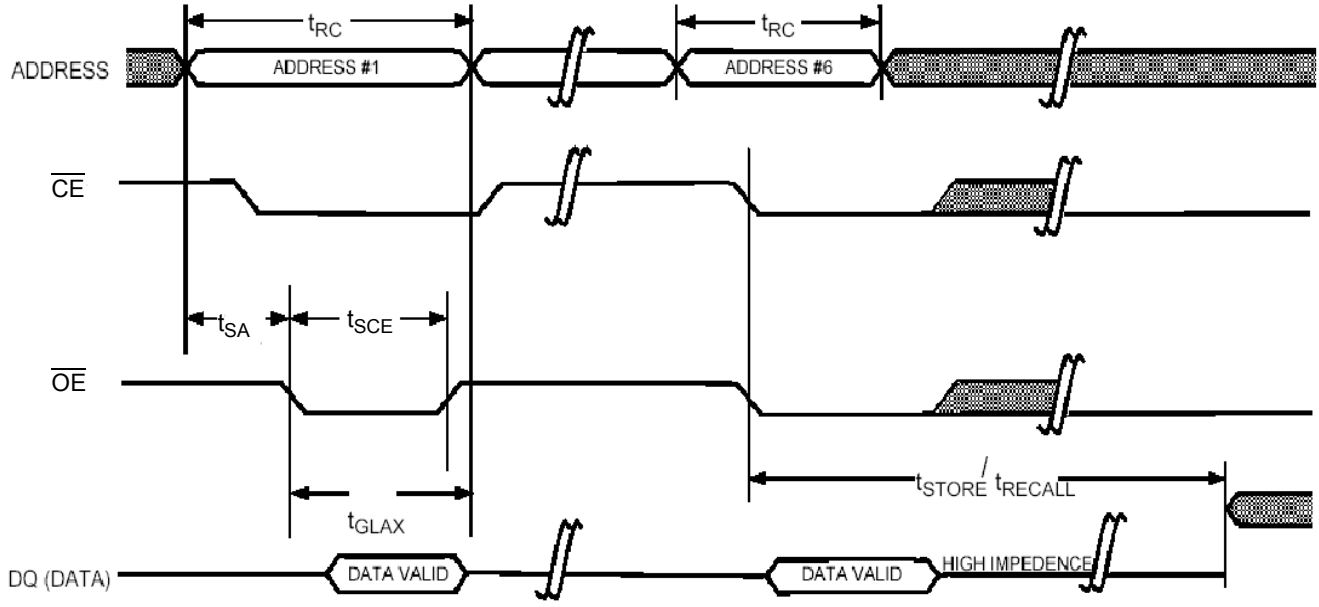


Figure 9. $\overline{OE}$-controlled Software STORE/RECALL Cycle[11]

Switching Waveforms (continued)

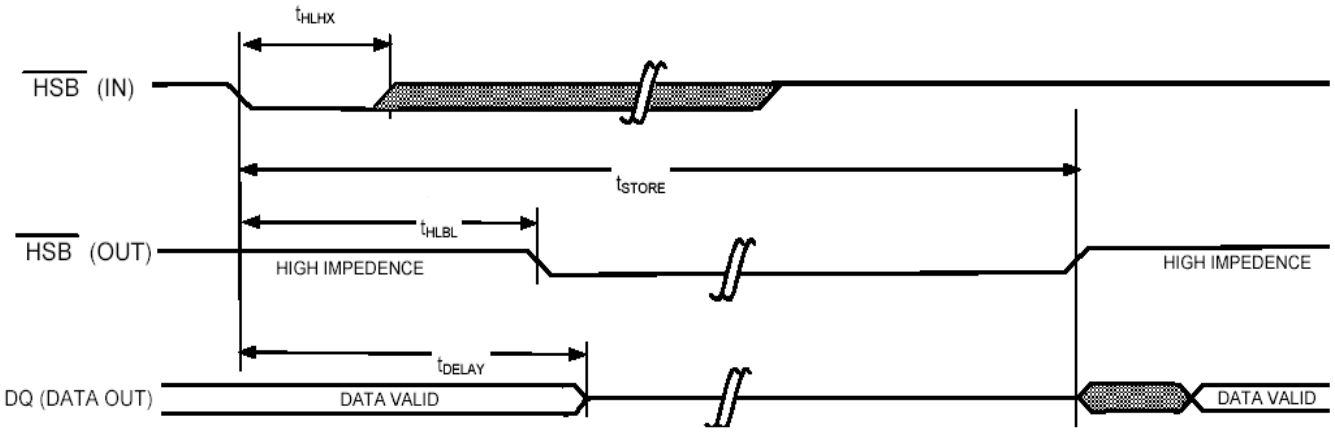


Figure 10. Hardware STORE Cycle

PART NUMBERING NOMENCLATURE

CY 14 B 256 L- SZ 25 C T

- Option:
  - T - Tape & Reel
  - Blank - Std.
- Temperature:
  - C - Commercial (0 to 70°C)
  - I - Industrial (–40 to 85°C)
  - A - Automotive (–40 to 125°C)
- Speed:
  - 25 - 25 ns
  - 35 - 35 ns
  - 45 - 45 ns
  - 55 - 55 ns
- Package:
  - SZ - 32 SOIC
  - SP - 48 SSOP
- Data Bus:
  - K - x8 + RTC
  - L - x8
- Density:
  - 016 - 16 Kb
  - 064 - 64 Kb
  - 256 - 256 Kb
  - 101 - 1 Mb
  - 102 - 2 Mb
  - 104 - 4 Mb
- Voltage:
  - A - 1.8V
  - B - 3.0V
  - C - 3.3V
  - D - 3.0/3.3V
  - E - 5.0V
- NVSRAM
  - 14 - AutoStore + software store + hardware store
  - 11 - Software store
  - 15 - AutoStore + software store
  - 16 - AutoStorePlus + hardware store
  - 10 - Hardware store
  - 22 - AutoStore + Hardware Store
  - 25 - AutoStore
- Cypress

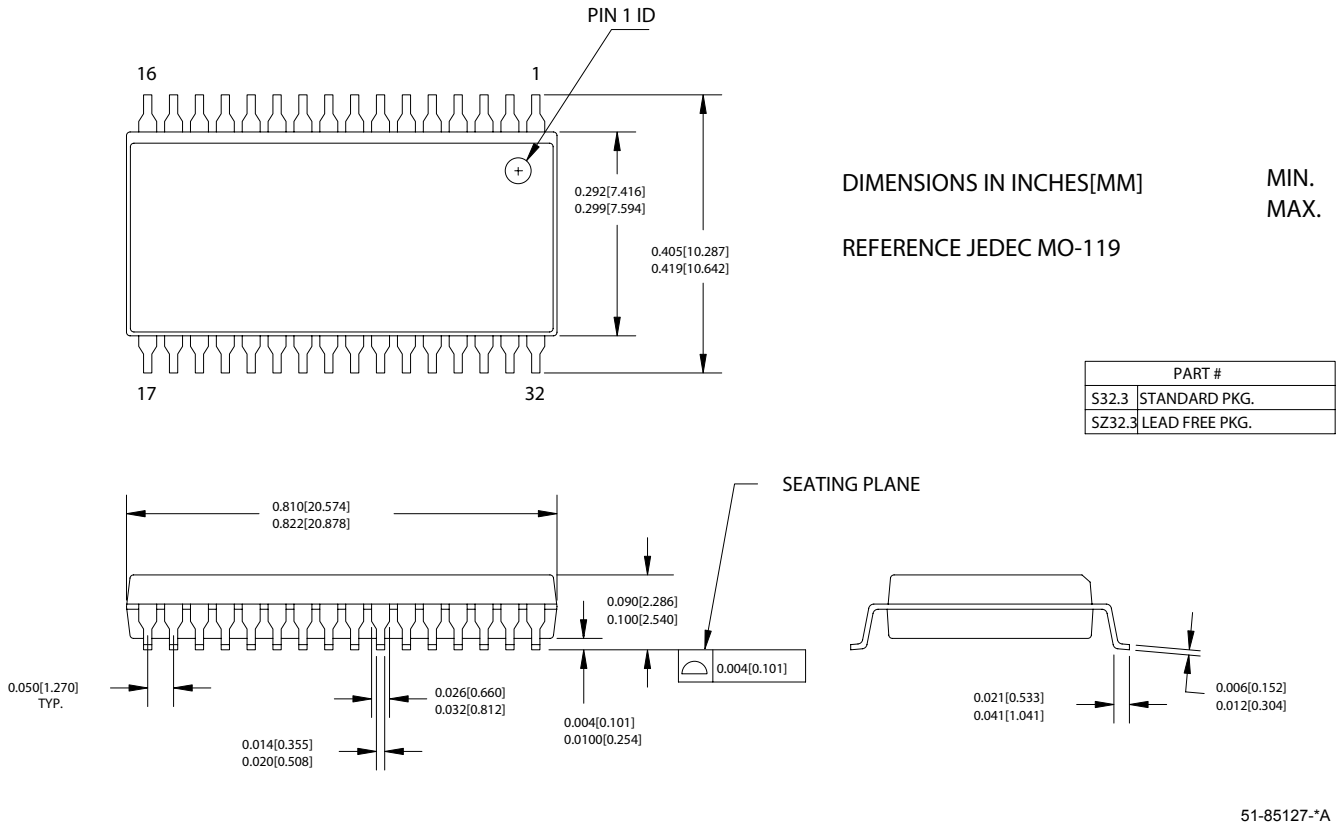
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B256L-SZ25CT	51-85127	32-pin SOIC Pb-Free	Commercial
	CY14B256L-SP25CT	51-85061	48-pin SSOP Pb-Free	
	CY14B256L-SZ25IT	51-85127	32-pin SOIC Pb-Free	Industrial
	CY14B256L-SP25IT	51-85061	48-pin SSOP Pb-Free	
	CY14B256L-SZ25I	51-85127	32-pin SOIC Pb-Free	
	CY14B256L-SP25I	51-85061	48-pin SSOP Pb-Free	
35	CY14B256L-SZ35CT	51-85127	32-pin SOIC Pb-Free	Commercial
	CY14B256L-SP35CT	51-85061	48-pin SSOP Pb-Free	
	CY14B256L-SZ35IT	51-85127	32-pin SOIC Pb-Free	Industrial
	CY14B256L-SP35IT	51-85061	48-pin SSOP Pb-Free	
	CY14B256L-SZ35I	51-85127	32-pin SOIC Pb-Free	
	CY14B256L-SP35I	51-85061	48-pin SSOP Pb-Free	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

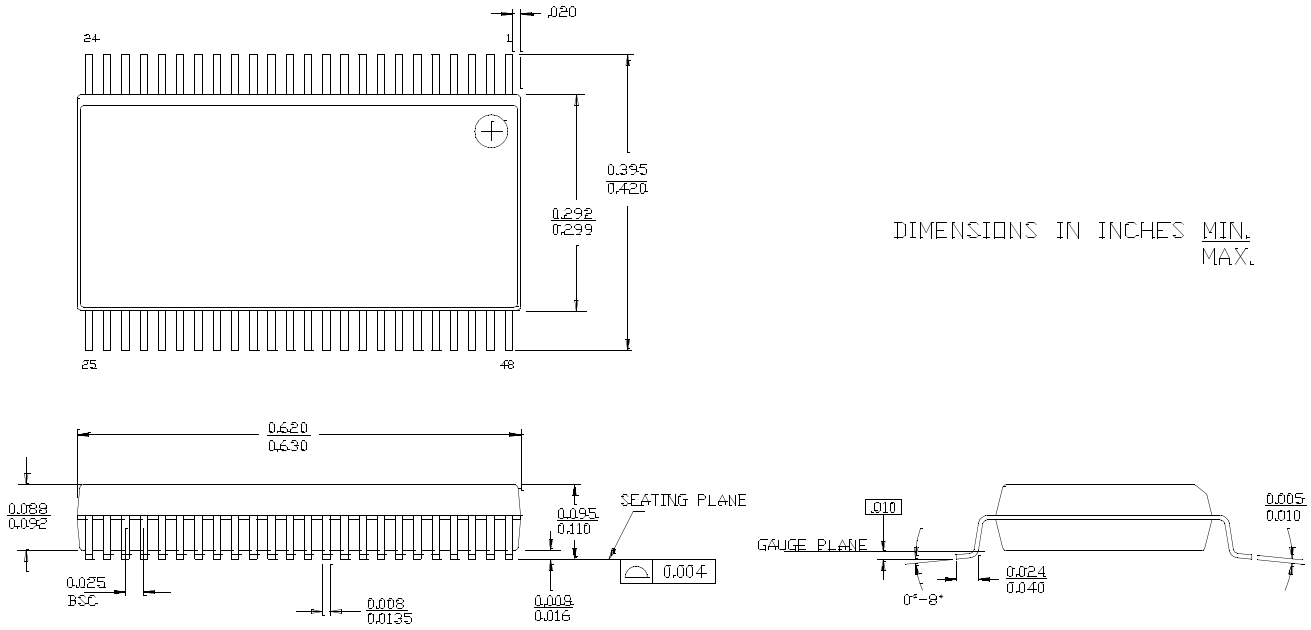
Package Diagrams

32-Lead (300-Mil) SOIC (51-85127)



Package Diagrams (continued)

48-Lead Shrunk Small Outline Package (51-85061)



51-85061-*C

Document History Page

Document Title: CY14B256L 256-Kbit (32K x 8) nvSRAM Document Number: 001-06422				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	425138	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on external Web