Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS
S E M I C O N D U C T O R

CD74FCT273

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 5.3ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **SCR Latchup Resistant BiCMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S**
- **48mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7V at V_{CC} = 5V**
- **Controlled Output Edge Rates**
- **Input/Output Isolation to V_{CC}**
- **BiCMOS Technology with Low Quiescent Power**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT273E	0 to 70	20 Ld PDIP	E20.3
CD74FCT273M	0 to 70	20 Ld SOIC	M20.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
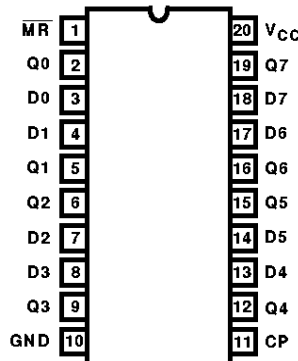
Description

The CD74FCT273 octal D flip-flop with reset uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

Information at the D input of the CD74FCT273 is transferred to the Q output on the positive going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

Pinout

CD74FCT273
(PDIP, SOIC)
TOP VIEW

```
         ┌───┐ ┌───┐
  MR  [ 1│   └─┘   │20] VCC
  Q0  [ 2│         │19] Q7
  D0  [ 3│         │18] D7
  D1  [ 4│         │17] D6
  Q1  [ 5│         │16] Q6
  Q2  [ 6│         │15] Q5
  D2  [ 7│         │14] D5
  D3  [ 8│         │13] D4
  Q3  [ 9│         │12] Q4
 GND  [10│         │11] CP
         └─────────┘
```

File Number **2303.2**

CD74FCT273

Functional Diagram


```
CLOCK ─── 11 ─┤          ├─ 2 ─── Q0
  CP

   D0 ──── 3 ─┤          ├─ 5 ─── Q1
   D1 ──── 4 ─┤          ├─ 6 ─── Q2
   D2 ──── 7 ─┤          ├─ 9 ─── Q3
   D3 ──── 8 ─┤          ├─ 12 ── Q4
   D4 ─── 13 ─┤          ├─ 15 ── Q5
   D5 ─── 14 ─┤          ├─ 16 ── Q6
   D6 ─── 17 ─┤          ├─ 19 ── Q7
   D7 ─── 18 ─┤      1   │
 RESET MR ────┘          │
```

DATA INPUTS

DATA OUTPUTS

GND = PIN 10
V_{CC} = PIN 20
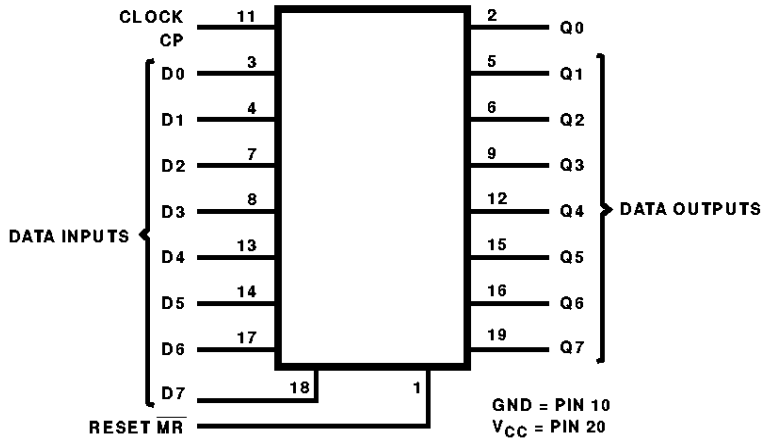
TRUTH TABLE (Note 1)

INPUTS			OUTPUTS
RESET $\overline{MR}$	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

NOTE:

1. H = HIGH Voltage Level (Steady State)
   L = LOW Voltage Level (Steady State)
   X = Irrelevant
   ↑ = Transition from low to high level.
   Q0 = The level of Q before the indicated steady state input conditions were established.

IEC Logic Symbol
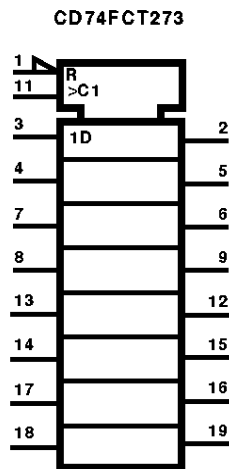
CD74FCT273

CD74FCT273

Absolute Maximum Ratings

DC Supply Voltage (V_{CC}). . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}). 400mA

Operating Conditions

Operating Temperature Range (T_A) . . . . .0°C to 70°C
Supply Voltage Range, V_{CC}. . . . . .4.75V to 5.25V
DC Input Voltage, V_I. . . . . 0 to V_{CC}
DC Output Voltage, V_O. . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv. . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
  PDIP Package 135
  SOIC Package. 125
Maximum Junction Temperature. . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . .300°C
  (SOIC-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 25°C MIN	25°C MAX	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	μA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	μA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	μA
	I_{OZL}	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

4. Inputs that are not measured are at V_{CC} or GND.

5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. at 70°C.

CD74FCT273

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays						
CP to Qn	t_{PLH}, t_{PHL}	5	7	2	13	ns
$\overline{MR}$ to Qn	t_{PLH}, t_{PHL}	5	8	2	13	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	36	-	-	pF
Input Capacitance	C_I	-	-	-	10	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.

7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
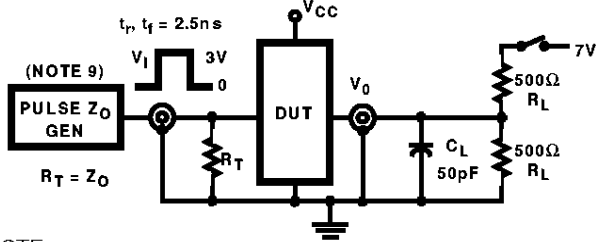 f_I = input frequency

Prerequisite for Switching (Note 8)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Data to CP Setup Time	t_{SU}	5	-	3	-	ns
Hold Time	t_H	5	-	2	-	ns
Removal Time, $\overline{MR}$ to CP	t_{REM}	5	-	4	-	ns
$\overline{MR}$ Pulse Width	t_W	5	-	7	-	ns
CP Pulse Width	t_W	5	-	7	-	ns
CP Frequency	f_{MAX}	5	-	70	-	MHz

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

CD74FCT273

Test Circuits and Waveforms

$t_r, t_f = 2.5ns$

(NOTE 9)

PULSE Z_O GEN

$R_T = Z_O$

V_{CC}

DUT

V_O

C_L 50pF

500Ω R_L

500Ω R_L

7V

NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; $t_f, t_r \leq 2.5ns$.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

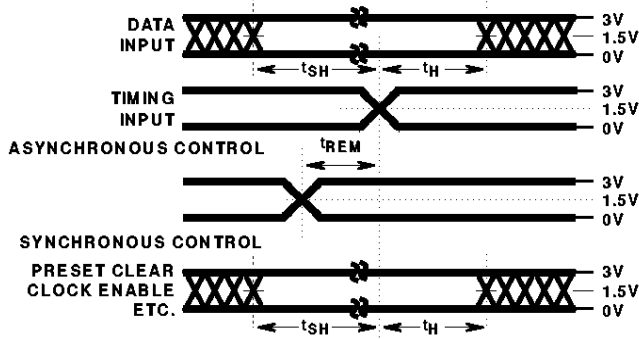Input: $t_r = t_f = 2.5ns$ (10% to 90%), unless otherwise specified

DATA INPUT — 3V / 1.5V / 0V — t_{SH}, t_H

TIMING INPUT — 3V / 1.5V / 0V

ASYNCHRONOUS CONTROL — t_{REM} — 3V / 1.5V / 0V

SYNCHRONOUS CONTROL

PRESET CLEAR CLOCK ENABLE ETC. — 3V / 1.5V / 0V — t_{SH}, t_H

FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

LOW-HIGH-LOW PULSE — 1.5V — t_W

HIGH-LOW-HIGH PULSE — 1.5V

FIGURE 3. PULSE WIDTH

ENABLE   DISABLE

CONTROL INPUT — 3V / 1.5V / 0V

t_{PZL} t_{PLZ}

OUTPUT NORMALLY LOW — SWITCH CLOSED — 3.5V / 1.5V — 3.5V — 0.3V — V_{OL}

t_{PZH} t_{PHZ}

OUTPUT NORMALLY HIGH — SWITCH OPEN — 1.5V / 0V — 0.3V — V_{OH} / 0V
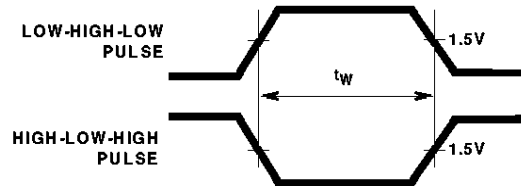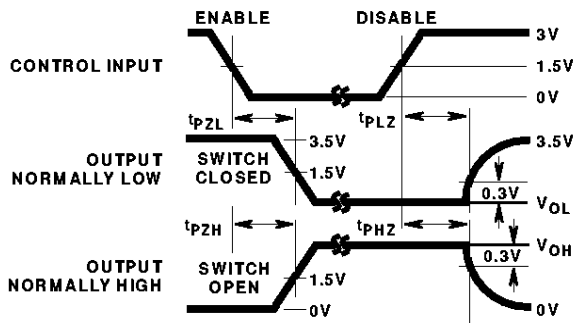
FIGURE 4. ENABLE AND DISABLE TIMING

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V

t_{PLH} t_{PHL}

OUTPUT — V_{OH} / 1.5V / V_{OL}

t_{PLH} t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

FIGURE 5. PROPAGATION DELAY

OTHER OUTPUTS — V_{OH} / V_{OL}

OUTPUT UNDER TEST — V_{OH} / V_{OHV} — V_{OLP} / V_{OL}
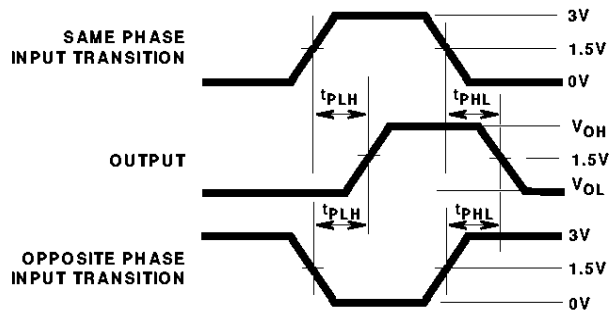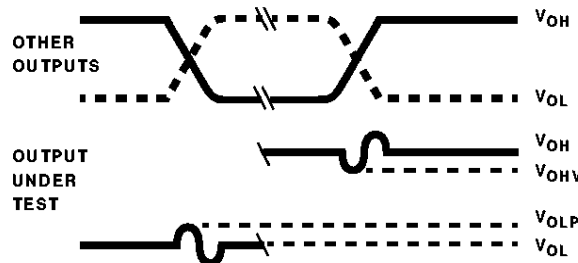
NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.

11. Input pulses have the following characteristics:
    $P_{RR} \leq$ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.

12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS