

TLV2442, TLV2442A, TLV2444, TLV2444A Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

SLOS169H – NOVEMBER 1996 – REVISED MARCH 2001

- Output Swing Includes Both Supply Rails
- Extended Common-Mode Input Voltage Range . . . 0 V to 4.25 V (Min) at 5-V Single Supply
- No Phase Inversion
- Low Noise . . . 16 nV/√Hz Typ at f = 1 kHz
- Low Input Offset Voltage
950 μV Max at T_A = 25°C (TLV244xA)
- Low Input Bias Current . . . 1 pA Typ
- 600-Ω Output Drive
- High-Gain Bandwidth . . . 1.8 MHz Typ
- Low Supply Current . . . 750 μA Per Channel Typ
- Macromodel Included
- Available in Q-Temp Automotive
HighRel Automotive Applications
Configuration Control/Print Support
Qualification to Automotive Standards

description

The TLV244x and TLV244xA are low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range of these devices has been extended over typical standard CMOS amplifiers, making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. Both devices offer comparable ac performance while having lower noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLV244x has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecommunications applications.

The other members in the TLV244x family are the low-power, TLV243x, and micro-power, TLV2422, versions.

The TLV244x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV244xA is available with a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

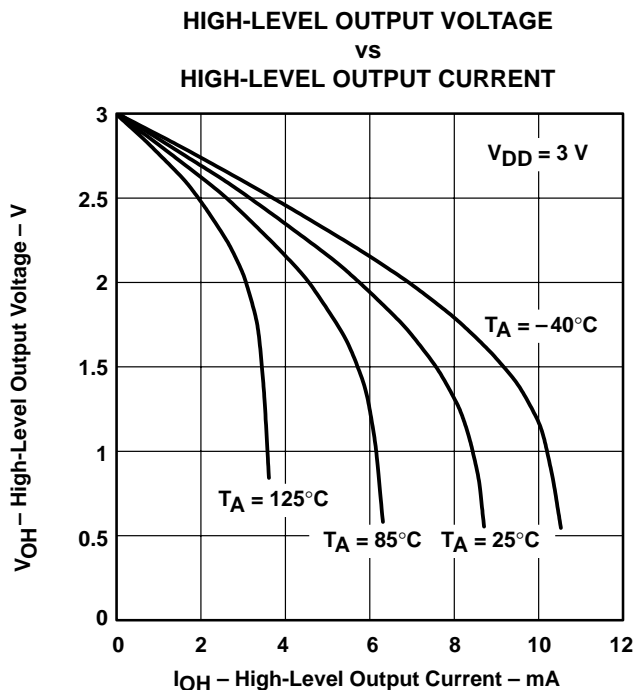


Figure 1



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TLV2442 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	2.5 mV	TLV2442CD	—	—	TLV2442CPW	—
–40°C to 85°C	950 μV 2.5 mV	TLV2442AID TLV2442ID	—	—	TLV2442AIPW —	—
–40°C to 125°C	950 μV 2.5 mV	TLV2442AQD TLV2442QD	—	—	TLV2442AQPW TLV2442QPW	—
–55°C to 125°C	950 μV 2.5 mV	—	TLV2442AMFK TLV2442MFK	TLV2442AMJG TLV2442MJG	—	TLV2442AMU TLV2442MU

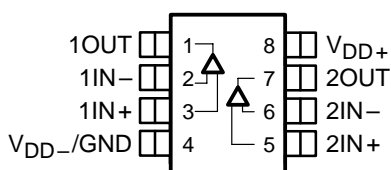
The D and PW packages are available taped and reeled. Add R suffix to device type (e.g., TLV2442CDR).

TLV2444 AVAILABLE OPTIONS

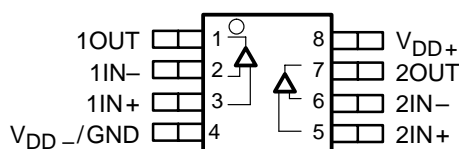
T _A	V _{IO} max AT 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
0°C to 70°C	2.5 mV	TLV2444CD	TLV2444CPW
–40°C to 125°C	950 μV 2.5 mV	TLV2444AID TLV2444ID	TLV2444AIPW TLV2444IPW

The D and PW packages are available taped and reeled. Add R suffix to device type (e.g., TLV2444CDR).

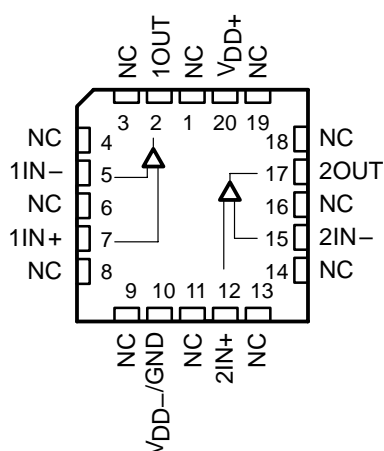
**TLV2442
D OR JG PACKAGE
(TOP VIEW)**



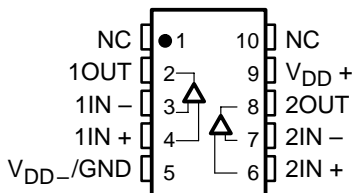
**TLV2442
PW PACKAGE
(TOP VIEW)**



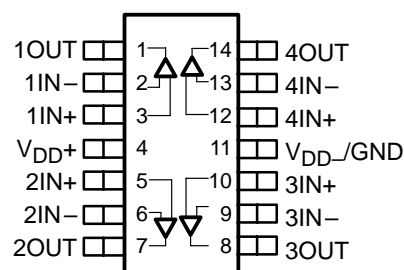
**TLV2442
FK PACKAGE
(TOP VIEW)**



**TLV2442
U PACKAGE
(TOP VIEW)**



**TLV2444
D OR PW PACKAGE
(TOP VIEW)**



NC – No internal connection

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage, V_I (any input, see Note 1)	-0.3 V to V_{DD}
Input current, I_I (any input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix (dual)	-40°C to 85°C
I suffix (quad)	-40°C to 125°C
Q suffix	-40°C to 125°C
M suffix	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current will flow if input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1$	V_{DD-}	$V_{DD+} - 1$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1$	V_{DD-}	$V_{DD+} - 1$	$V_{DD-} + 2$	$V_{DD+} - 1.3$	$V_{DD-} + 2$	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	125	-40	125	-55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2442			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 1.5\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	TLV244xC TLV244xI	25°C	300	2000	μV
			Full range	2500		
		TLV244xAI	25°C	300	950	
			Full range	1500		
		TLV2442AQ TLV2442AM	25°C	300	950	
			Full range	1600		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 85°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.002		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60	pA	
		Full range	150			
I_{IB} Input bias current		25°C	1	60	pA	
		-40°C to 85°C	150			
		125°C	350			
		TLV2442Q/AQ TLV2442M/AM	Full range	260		
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 2.25	-0.25 to 2.5	V	
		Full range	0 to 2			
		25°C to -55°C	0 to 2.25	-0.25 to 2.5		
		125°C	0 to 2			
V_{OH} High-level output voltage	$I_O = -100\ \mu\text{A}$	25°C	2.98		V	
		25°C	2.5			
		Full range	2.25			
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_O = 100\ \mu\text{A}$	25°C	0.02		V	
		25°C	0.63			
		Full range	1			
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to }2\text{ V}$	$R_L = 600\ \Omega$	25°C	0.7	1	V/mV
			Full range	0.4		
		$R_L = 1\ \text{M}\Omega$	25°C	750		
r_{id} Differential input resistance		25°C	1000		$\text{G}\Omega$	
r_i Common-mode input resistance		25°C	1000		$\text{G}\Omega$	
c_i Common-mode input capacitance	$f = 10\ \text{kHz}$	25°C	8		pF	
z_o Closed-loop output impedance	$f = 1\ \text{MHz}$, $A_V = 10$	25°C	130		Ω	

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is -40°C to 85°C. Full range for the quad I suffix is -40°C to 125°C. Full range for the Q suffix is -40°C to 125°C. Full range for the M suffix is -55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2442			UNIT
			MIN	TYP	MAX	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.25\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	65	75	dB	
		Full range	55			
		Full range	50			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, No load $V_{IC} = V_{DD}/2$,	25°C	80	95	dB	
		Full range	80			
I_{DD} Supply current (per channel)	$V_O = 1.5\text{ V}$, No load	25°C	725	1100	μA	
		Full range	1100			

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is –40°C to 85°C. Full range for the quad I suffix is –40°C to 125°C. Full range for the Q suffix is –40°C to 125°C. Full range for the M suffix is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV244x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }2\text{ V}$, $R_L = 600\ \Omega$, $C_L = 100\text{ pF}$	25°C	0.65	1.3	$\text{V}/\mu\text{s}$	
		Full range	0.65			
		Full range	0.4			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	170		$\text{nV}/\sqrt{\text{Hz}}$	
		25°C	18			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	2.6		μV	
		25°C	5.1			
I_n Equivalent input noise current		25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $R_L = 600\ \Omega$, $f = 1\text{ kHz}$	25°C	$A_V = 1$	0.08%		
			$A_V = 10$	0.3%		
			$A_V = 100$	2%		
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	25°C	1.75		MHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$,	25°C	0.9		MHz	
t_s Settling time	$A_V = -1$, Step = –2.3 V to 2.3 V, $R_L = 600\ \Omega$, $C_L = 100\text{ pF}$	25°C	To 0.1%	1.5		
			To 0.01%	3.2		
ϕ_m Phase margin at unity gain	$R_L = 600\ \Omega$, $C_L = 100\text{ pF}$	25°C	65°			
Gain margin		25°C	9		dB	

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is –40°C to 85°C. Full range for the quad I suffix is –40°C to 125°C. Full range for the Q suffix is –40°C to 125°C. Full range for the M suffix is –55°C to 125°C.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV244x			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TLV244xC TLV244xI	25°C	300	2000	μV
			Full range		2500	
		TLV244xA	25°C	300	950	
			Full range		1500	
		TLV2442AQ TLV2442AM	25°C	300	950	
			Full range		1600	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.002		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60	pA	
		Full range	150			
I_{IB} Input bias current		25°C	1	60	pA	
		-40°C to 85°C	150			
		125°C	350			
		TLV2442Q/AQ TLV2442M/AM	Full range	260		
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 4.25	-0.25 to 4.5	V	
		Full range	0 to 4			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$	25°C	4.97		V	
	$I_{OH} = -5\text{ mA}$	25°C	4	4.35		
		Full range	4			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 100\ \mu\text{A}$	25°C	0.01		V	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 5\text{ mA}$	25°C	0.8			
		Full range	1.25			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 600\ \Omega$ ‡	25°C	0.9	1.3	V/mV
			Full range	0.5		
		$R_L = 1\text{ M}\Omega$ ‡	25°C	950		
r_{id} Differential input resistance		25°C	1000		$\text{G}\Omega$	
r_i Common-mode input resistance		25°C	1000		$\text{G}\Omega$	
c_i Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	8		pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 10$	25°C	140		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }4.25\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	75	dB	
		Full range	70			

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‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV244x			UNIT
			MIN	TYP	MAX	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		dB
		Full range	80			
I_{DD} Supply current (per channel)	$V_O = 2.5\text{ V}$, No load	25°C	750	1100		μA
		Full range	1100			

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is –40°C to 85°C. Full range for the quad I suffix is –40°C to 125°C. Full range for the Q suffix is –40°C to 125°C. Full range for the M suffix is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV244x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}$, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.75	1.4		$\text{V}/\mu\text{s}$
		Full range	0.75			
		Full range	0.5			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	130			$\text{nV}/\sqrt{\text{Hz}}$
		25°C	16			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1.8			μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	3.6			
I_n Equivalent input noise current		25°C	0.6			$\text{fA}/\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V}$, $f = 1\text{ kHz}$, $R_L = 600\ \Omega$ ‡	25°C	$A_V = 1$			
			$A_V = 10$			
			$A_V = 100$			
Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	1.81			MHz
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 600\ \Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	0.5			MHz
t_s Settling time	$A_V = -1$, Step = 0.5 V to 2.5 V, $R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	To 0.1%			μs
			To 0.01%			
ϕ_m Phase margin at unity gain	$R_L = 600\ \Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	68°			
Gain margin		25°C	8			dB

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TYPICAL CHARACTERISTICS

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		vs Free-air temperature	26
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		vs Free-air temperature	29
I_{DD}	Supply current	vs Supply voltage	30
SR	Slew rate	vs Load capacitance	31
		vs Free-air temperature	32
V_O	Inverting large-signal pulse response		33, 34
	Voltage-follower large-signal pulse response		35, 36
	Inverting small-signal pulse response		37, 38
	Voltage-follower small-signal pulse response		39, 40
V_n	Equivalent input noise voltage	vs Frequency	41, 42
	Noise voltage	Over a 10-second period	43
THD + N	Total harmonic distortion plus noise	vs Frequency	44, 45
	Gain-bandwidth product	vs Free-air temperature	46
		vs Supply voltage	47
ϕ_m	Phase margin	vs Frequency	19, 20
		vs Load capacitance	48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

† For all graphs where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TLV2442, TLV2442A, TLV2444, TLV2444A
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2442
 INPUT OFFSET VOLTAGE**

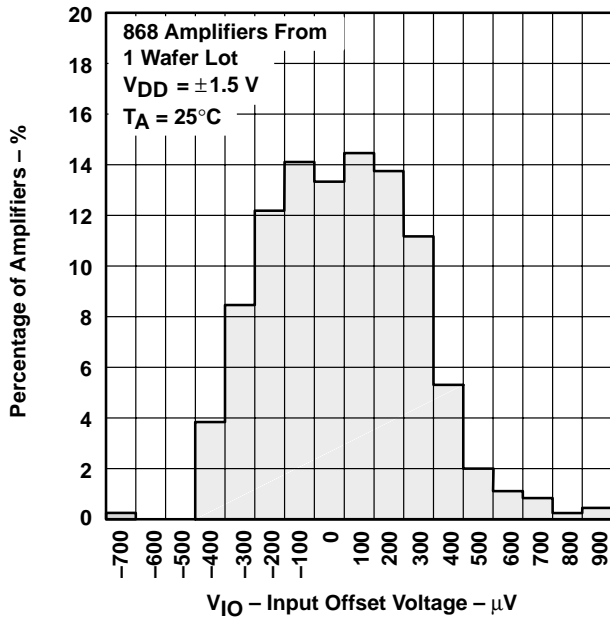


Figure 2

**DISTRIBUTION OF TLV2442
 INPUT OFFSET VOLTAGE**

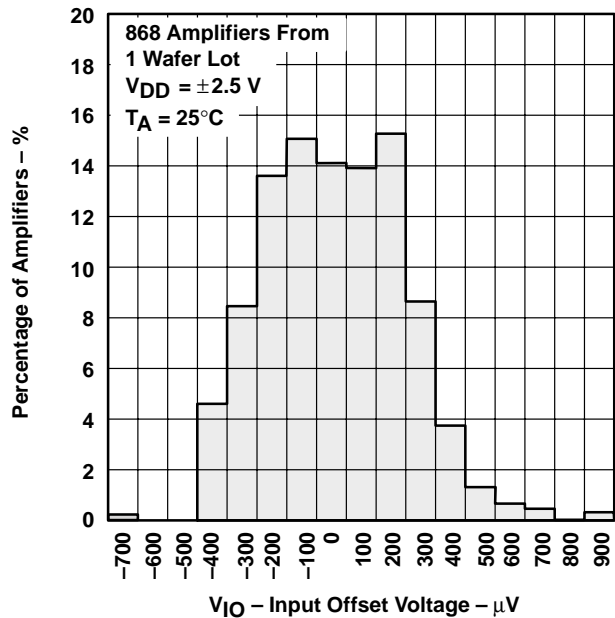


Figure 3

**INPUT OFFSET VOLTAGE
 vs
 COMMON-MODE INPUT VOLTAGE**

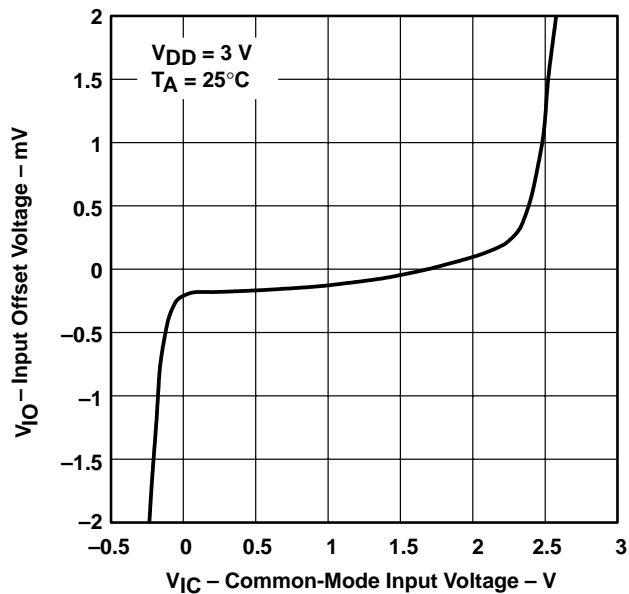


Figure 4

**INPUT OFFSET VOLTAGE
 vs
 COMMON-MODE INPUT VOLTAGE**

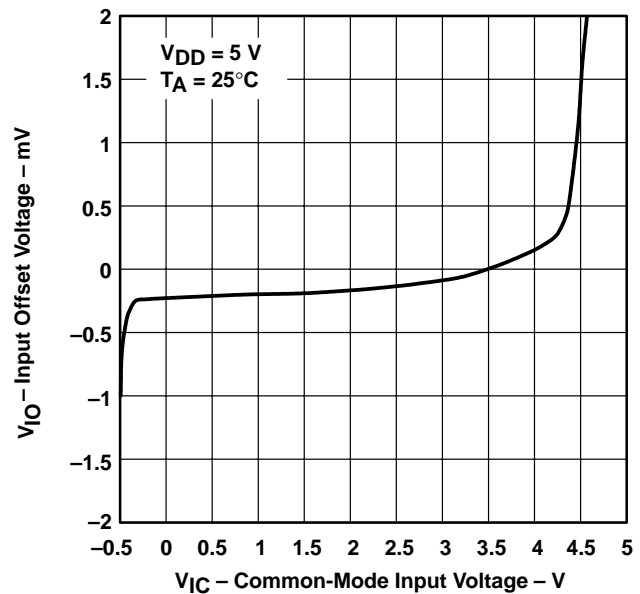


Figure 5



TYPICAL CHARACTERISTICS

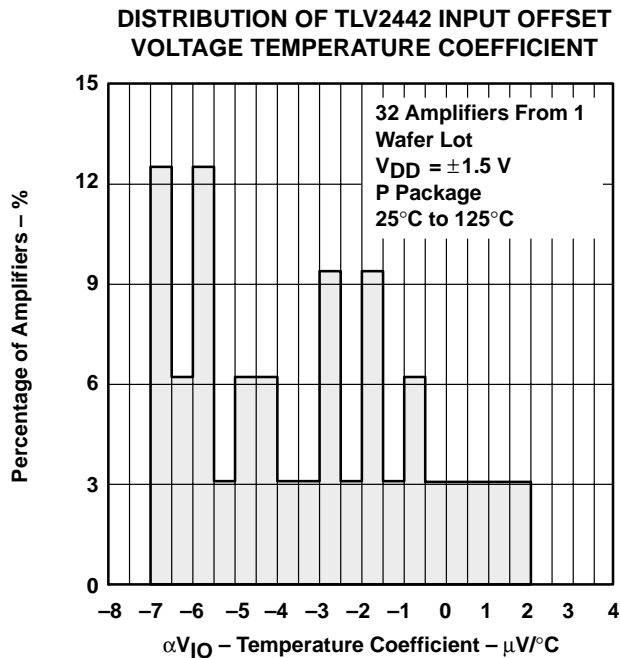


Figure 6

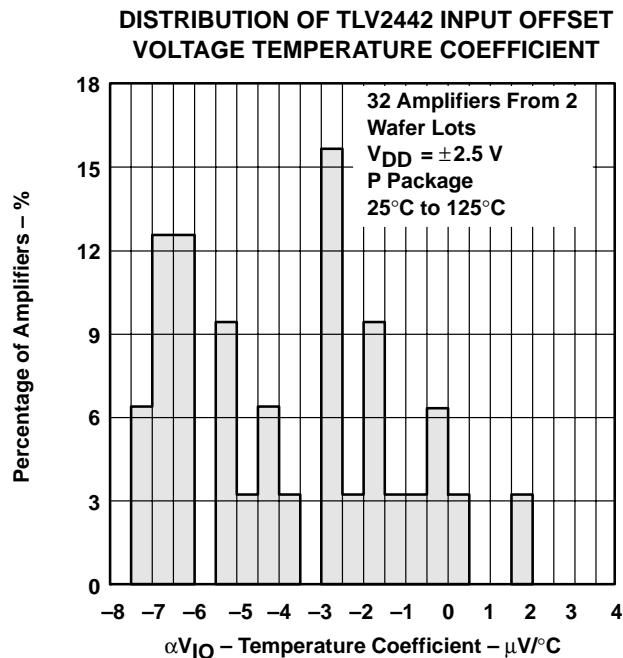


Figure 7

**INPUT BIAS AND INPUT OFFSET CURRENTS
 vs
 FREE-AIR TEMPERATURE**

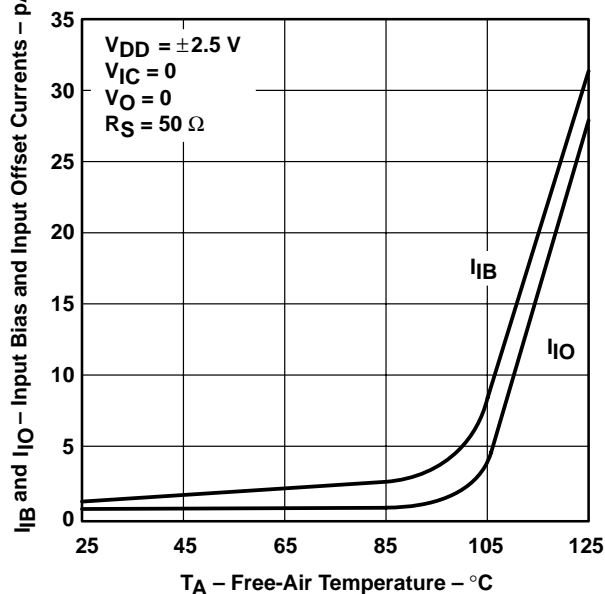


Figure 8

**HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT**

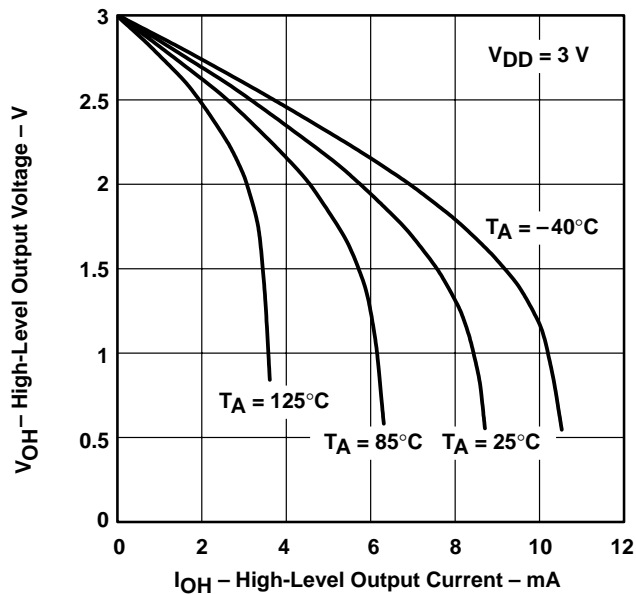


Figure 9

TLV2442, TLV2442A, TLV2444, TLV2444A
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
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TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

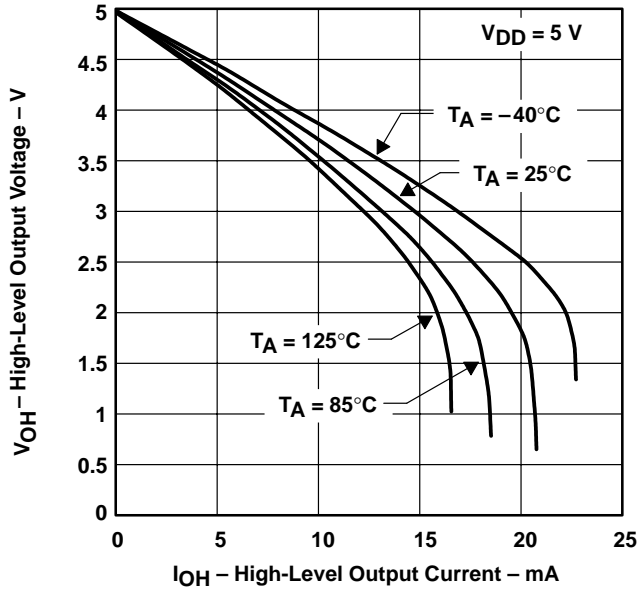


Figure 10

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

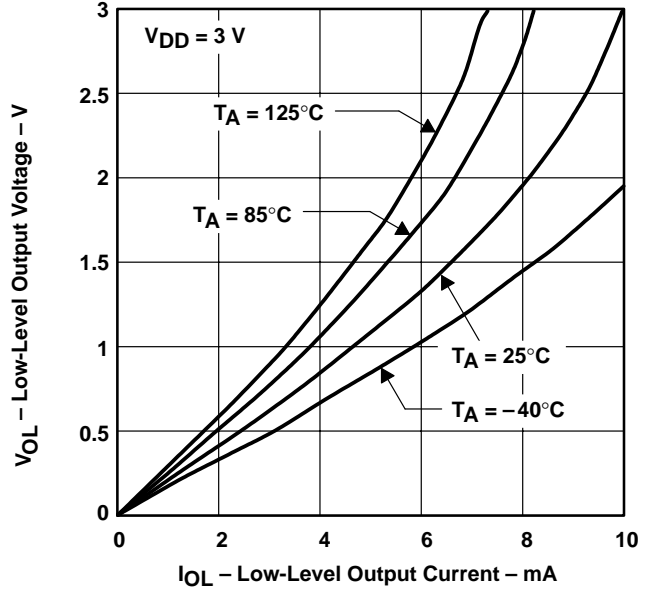


Figure 11

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

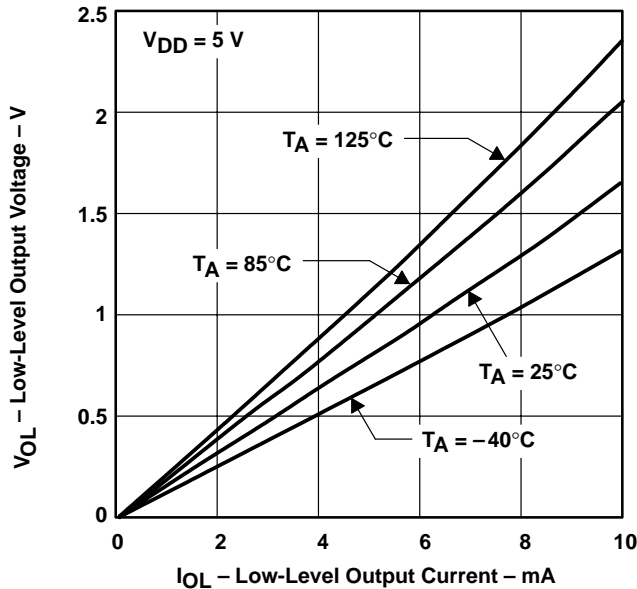


Figure 12

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

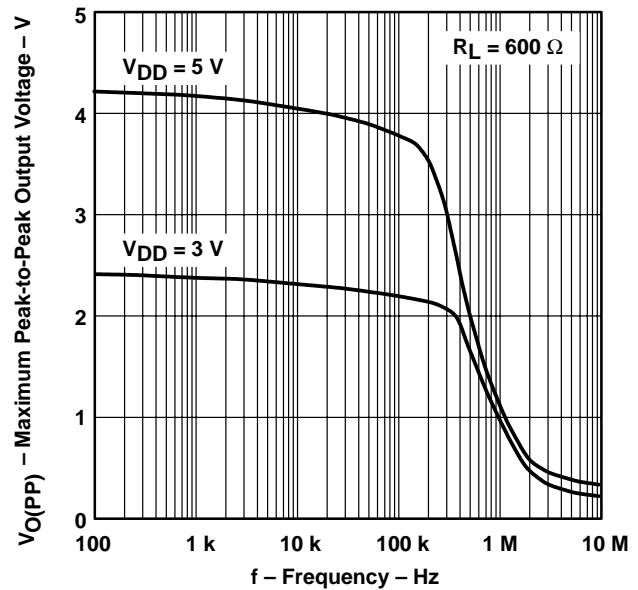


Figure 13



TYPICAL CHARACTERISTICS

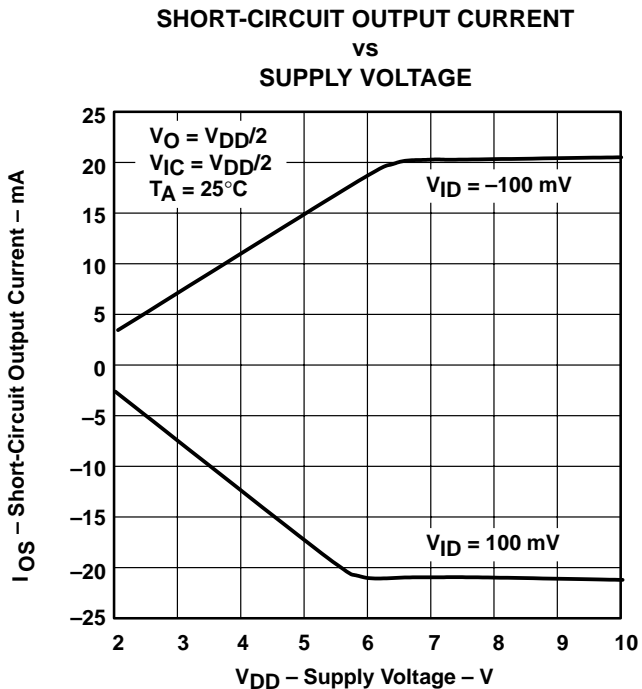


Figure 14

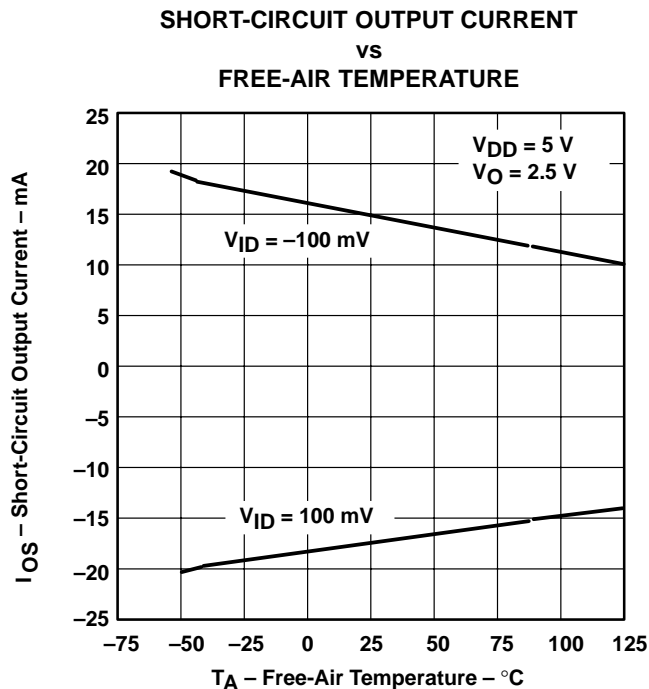


Figure 15

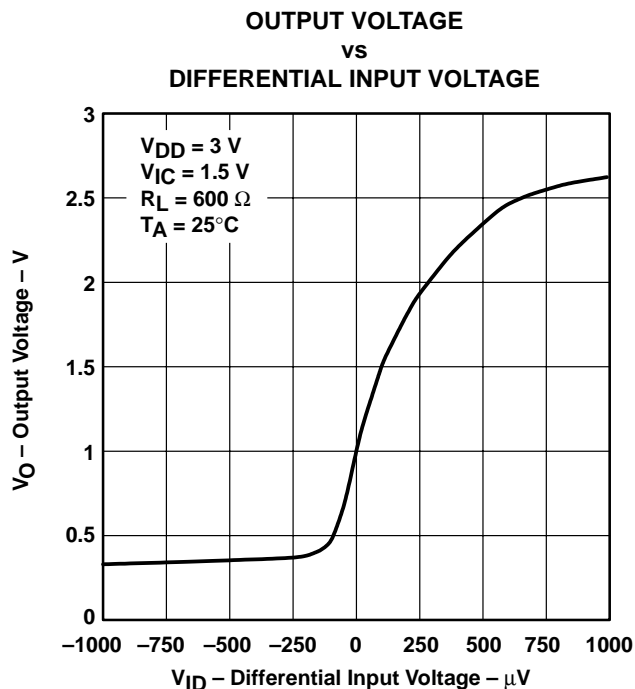


Figure 16

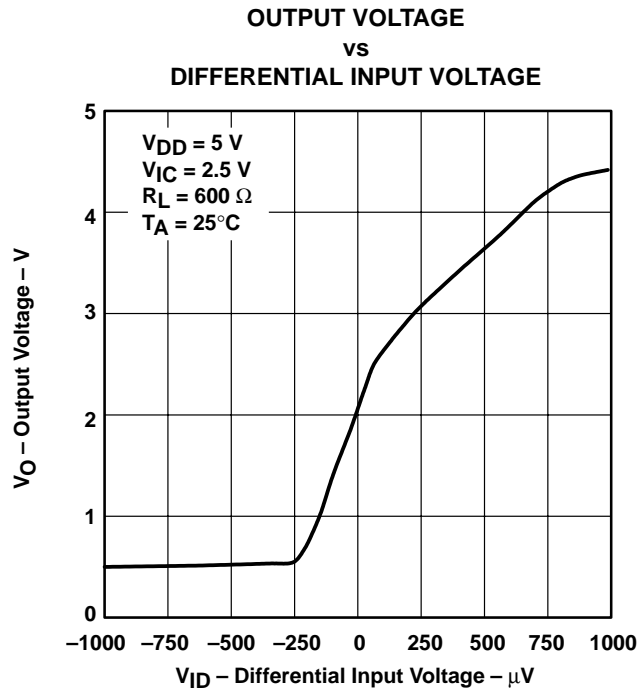


Figure 17

TLV2442, TLV2442A, TLV2444, TLV2444A
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

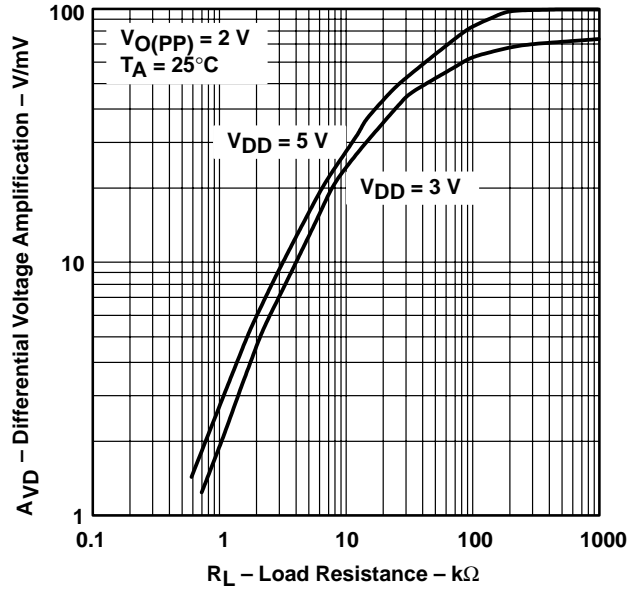


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

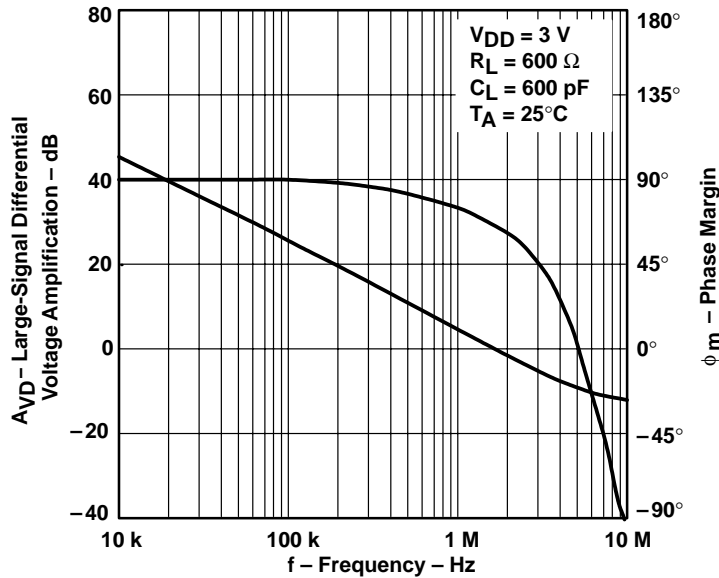


Figure 19



TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN
 vs
 FREQUENCY



Figure 20

LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE



Figure 21

LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE

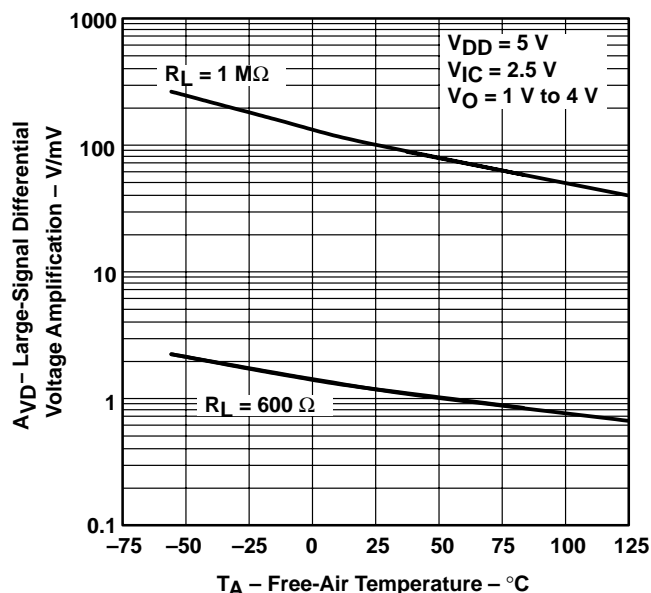


Figure 22

TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**OUTPUT IMPEDANCE
vs
FREQUENCY**

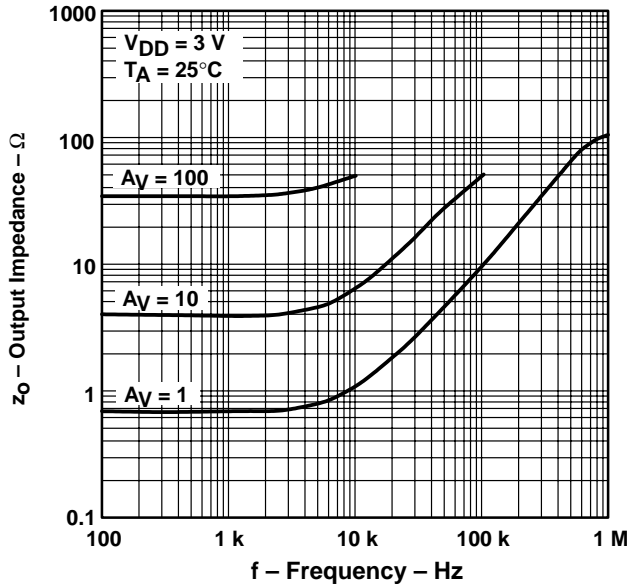


Figure 23

**OUTPUT IMPEDANCE
vs
FREQUENCY**

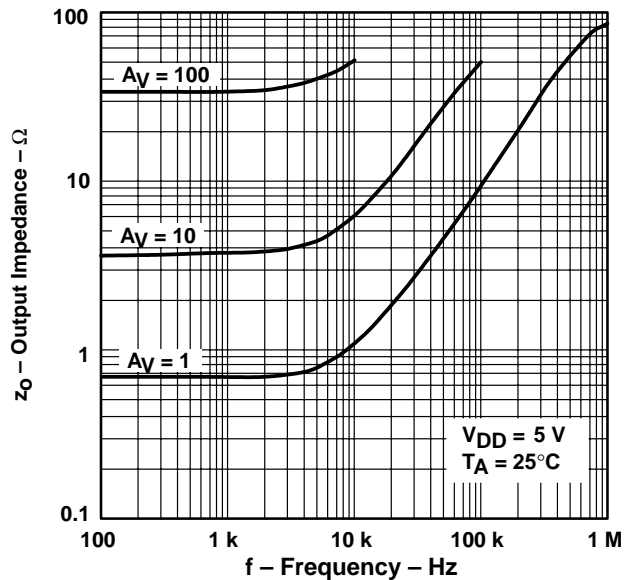


Figure 24

**COMMON-MODE REJECTION RATIO
vs
FREQUENCY**

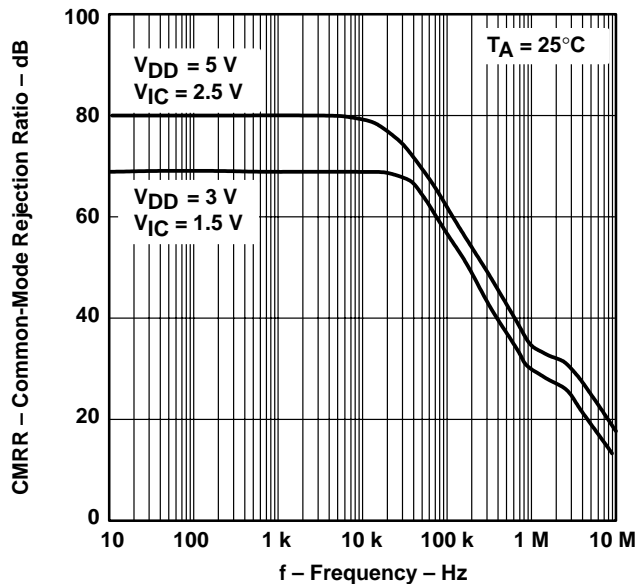


Figure 25

**COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE**

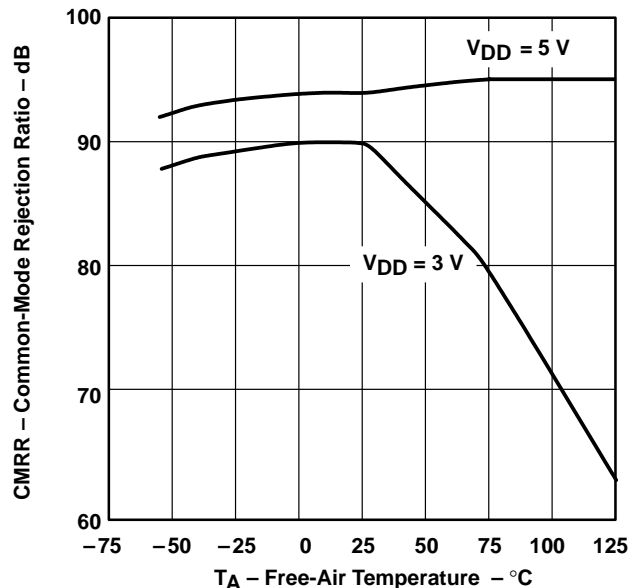


Figure 26



TYPICAL CHARACTERISTICS



Figure 27



Figure 28

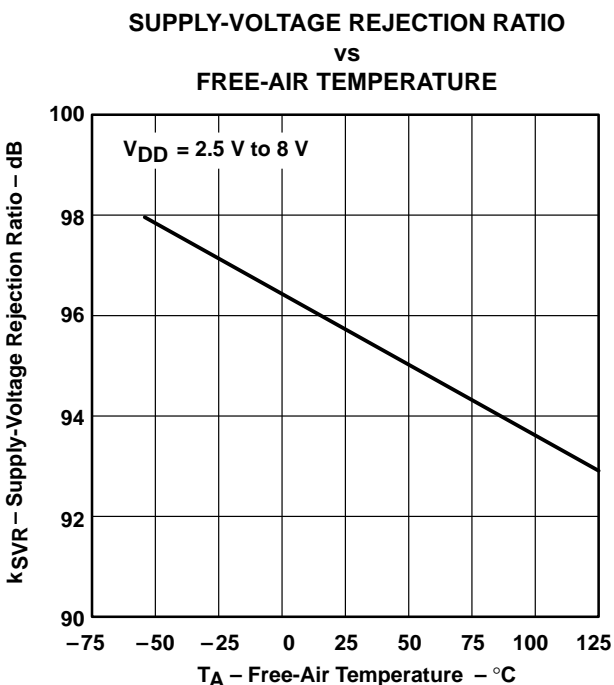


Figure 29

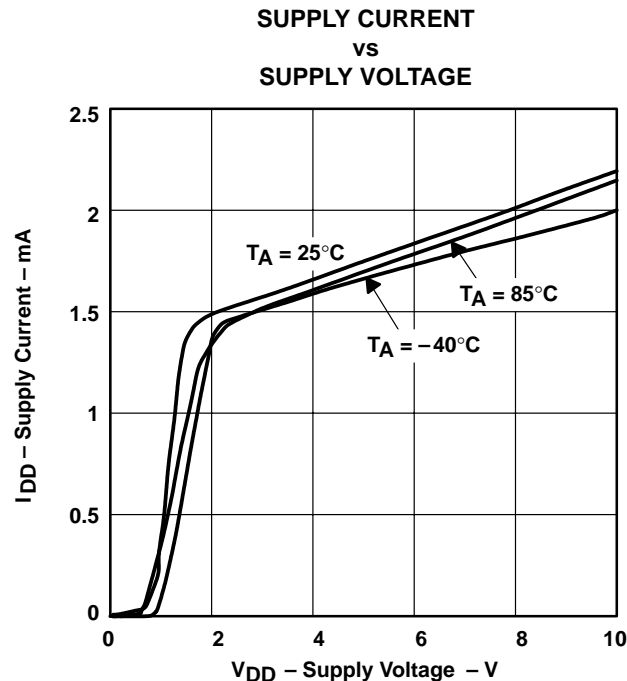


Figure 30

TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**SLEW RATE
vs
LOAD CAPACITANCE**

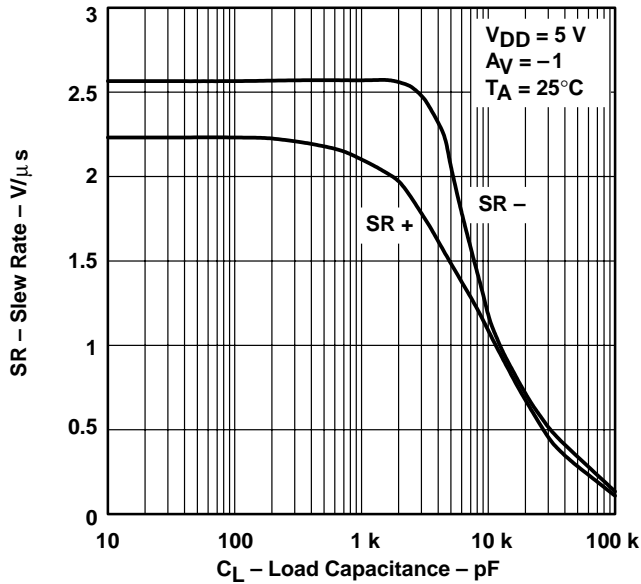


Figure 31

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

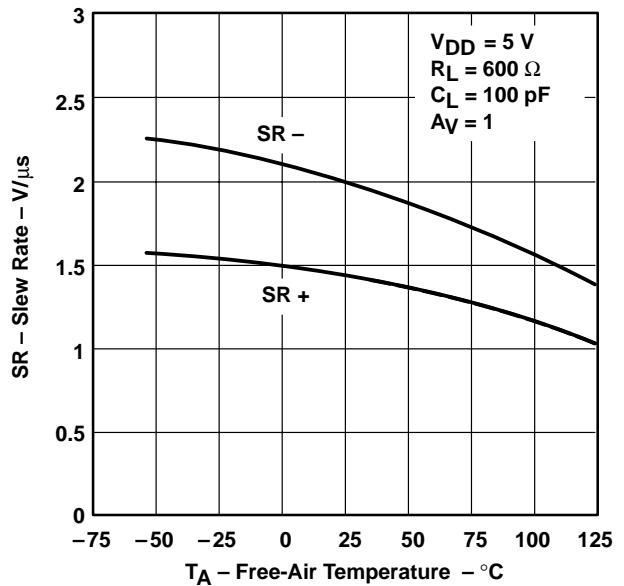


Figure 32

INVERTING LARGE-SIGNAL PULSE RESPONSE

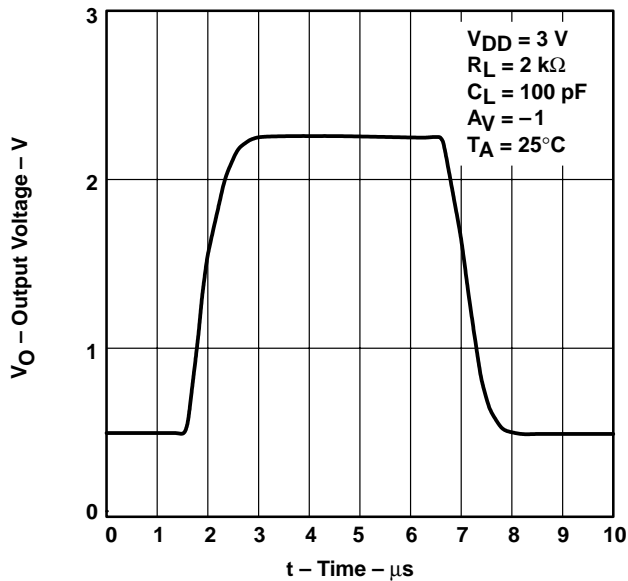


Figure 33

INVERTING LARGE-SIGNAL PULSE RESPONSE

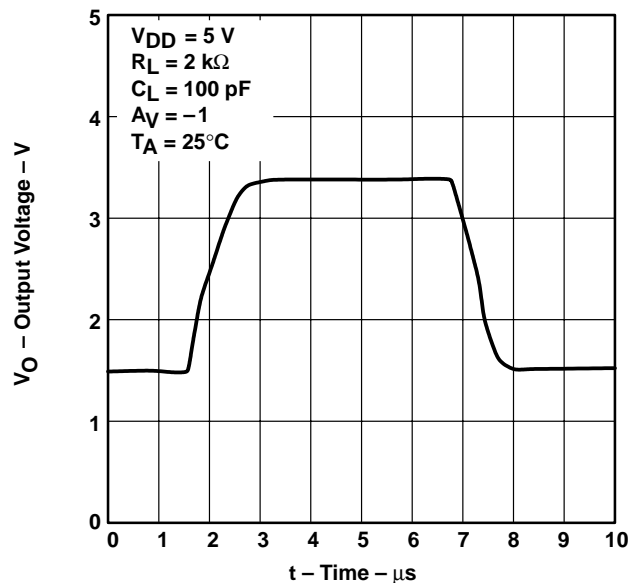


Figure 34



TYPICAL CHARACTERISTICS

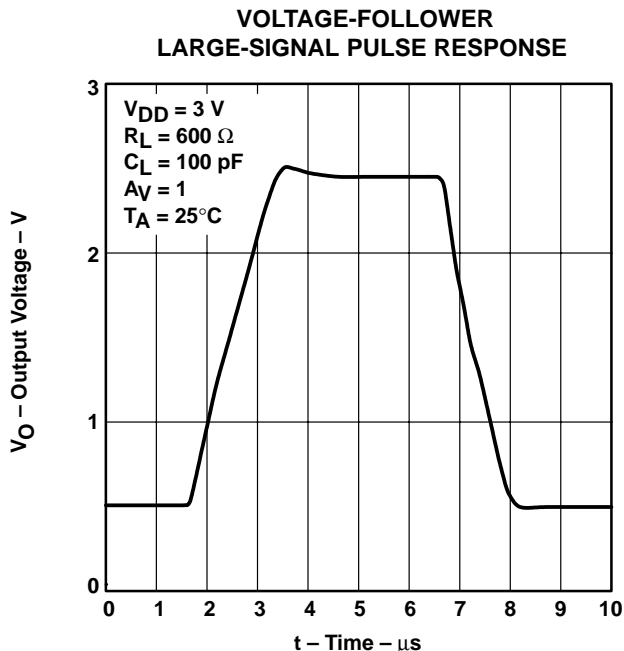


Figure 35



Figure 36

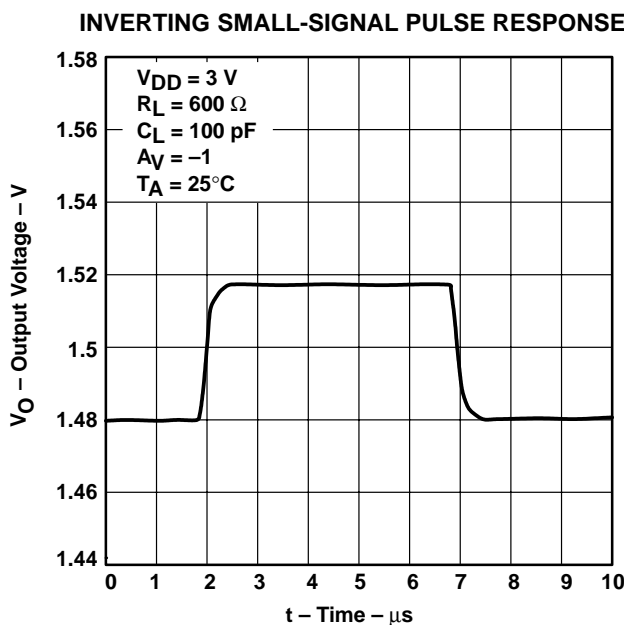


Figure 37

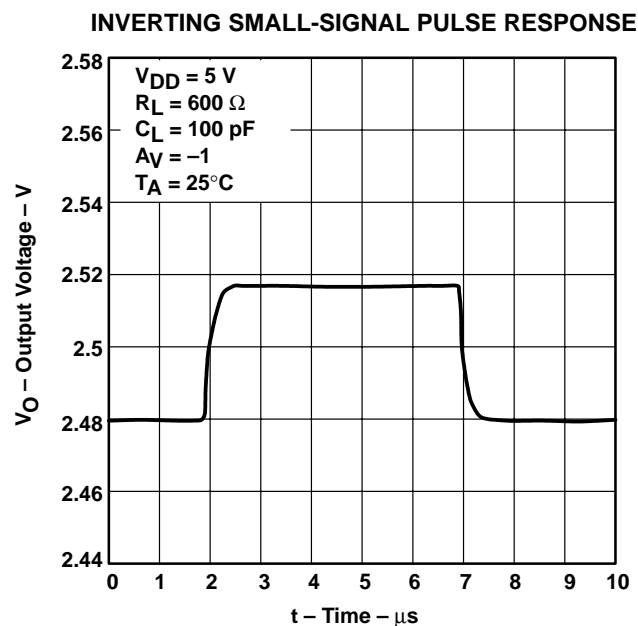


Figure 38

TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER
 SMALL-SIGNAL PULSE RESPONSE**

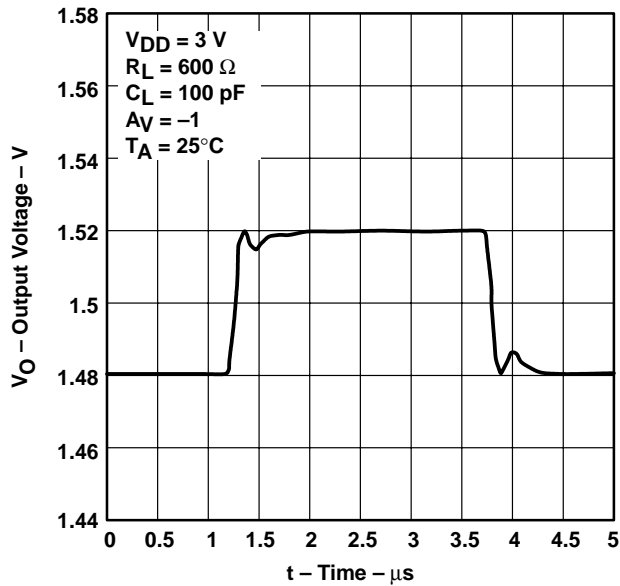


Figure 39

**VOLTAGE-FOLLOWER
 SMALL-SIGNAL PULSE RESPONSE**

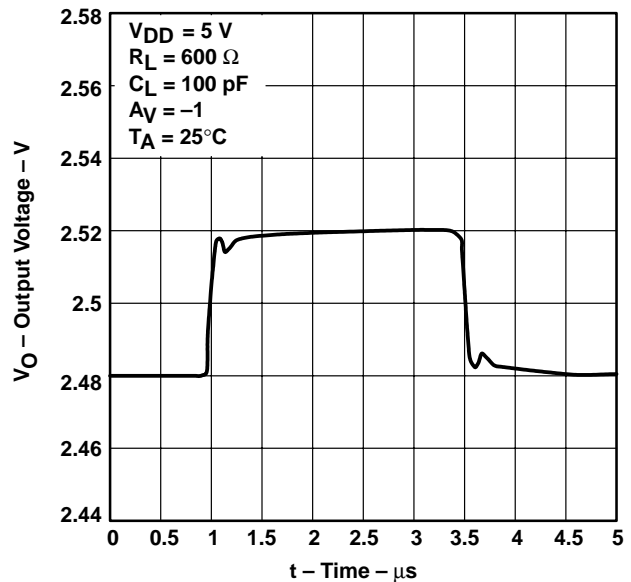


Figure 40

**EQUIVALENT INPUT NOISE VOLTAGE
 VS
 FREQUENCY**

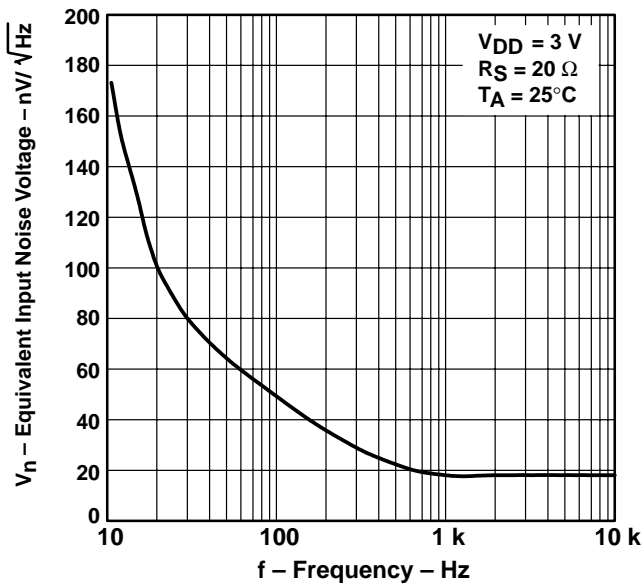


Figure 41

**EQUIVALENT INPUT NOISE VOLTAGE
 VS
 FREQUENCY**

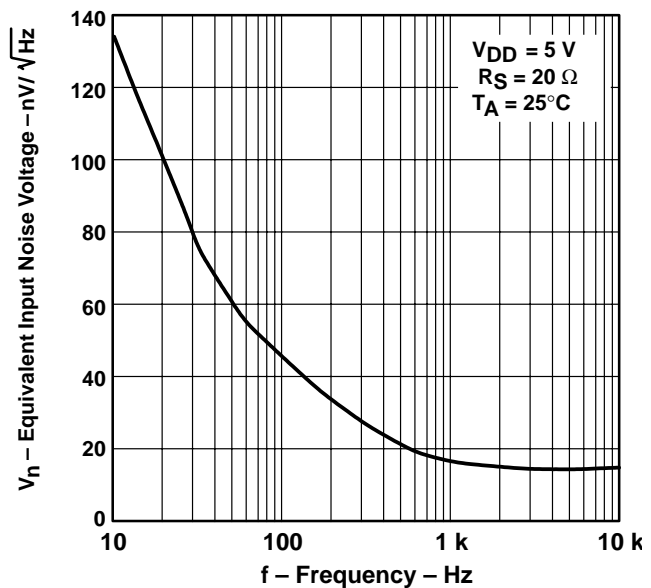


Figure 42



TYPICAL CHARACTERISTICS

NOISE VOLTAGE
 OVER A 10-SECOND PERIOD



Figure 43

TOTAL HARMONIC DISTORTION PLUS NOISE
 vs
 FREQUENCY



Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
 vs
 FREQUENCY



Figure 45

GAIN-BANDWIDTH PRODUCT
 vs
 FREE-AIR TEMPERATURE

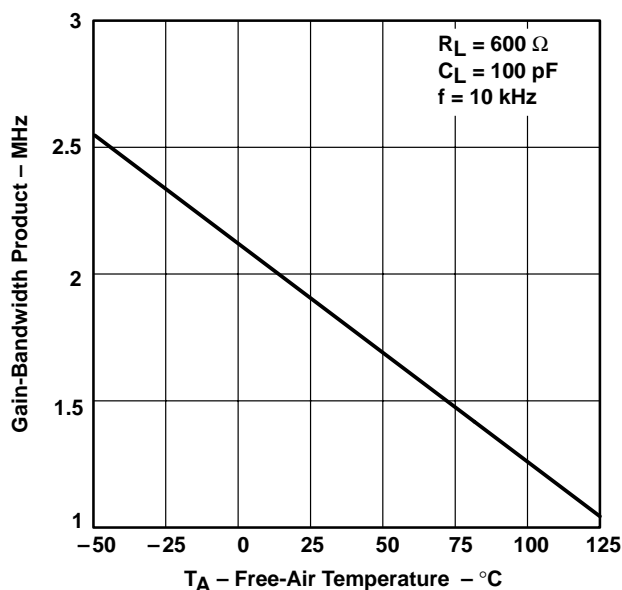


Figure 46

TLV2442, TLV2442A, TLV2444, TLV2444A
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

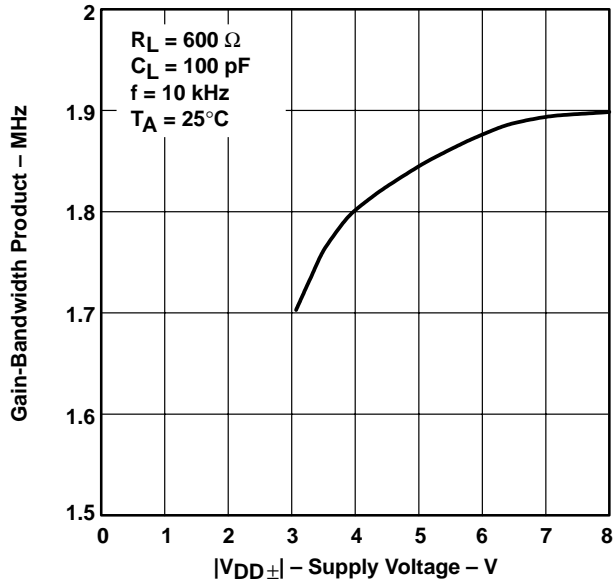


Figure 47

PHASE MARGIN
vs
LOAD CAPACITANCE

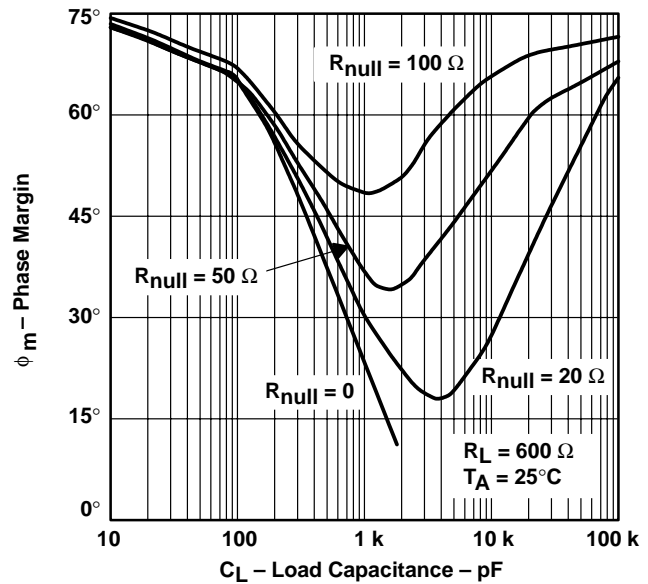


Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

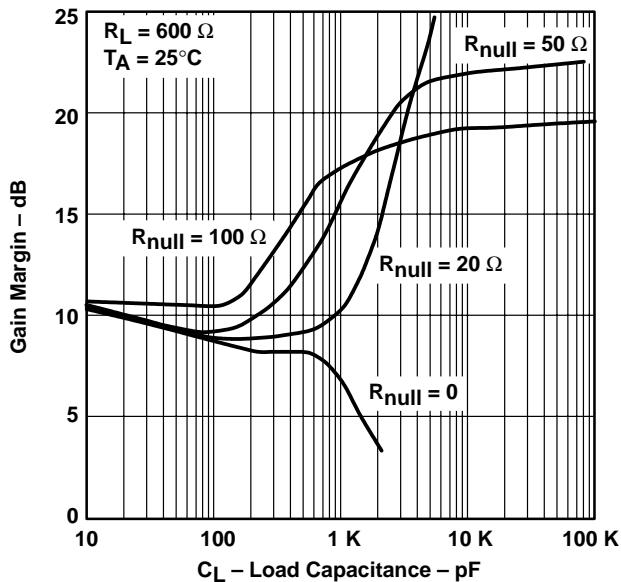


Figure 49

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

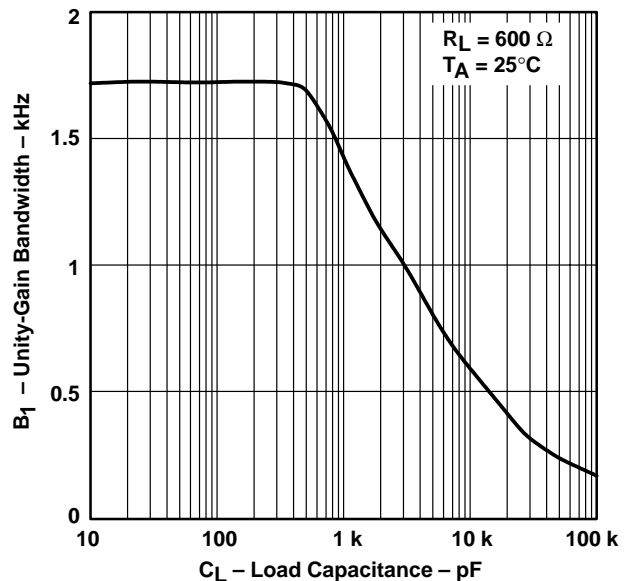


Figure 50



TLV2442, TLV2442A, TLV2444, TLV2444A Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 51 were generated using the TLV244x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

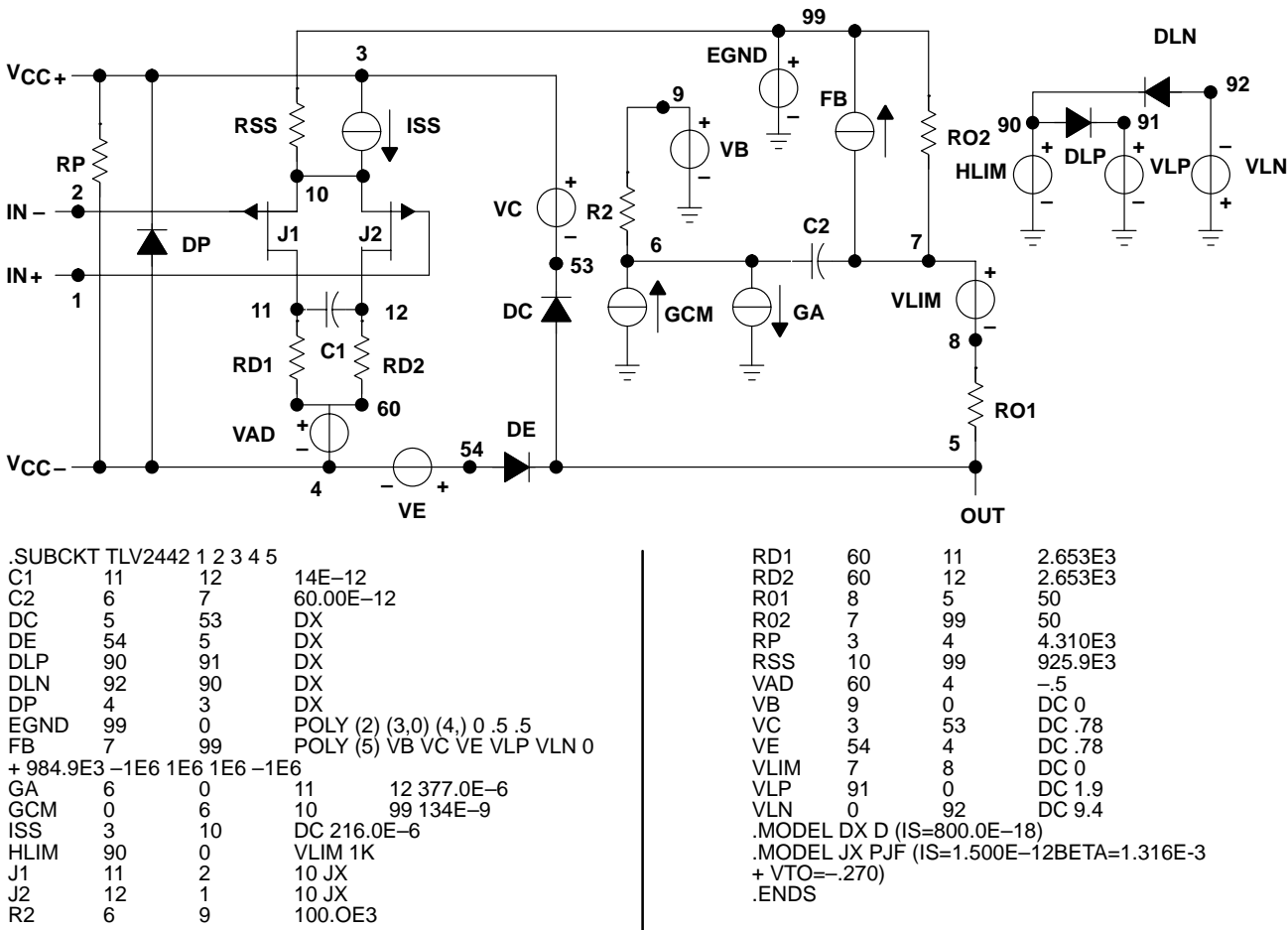


Figure 51. Boyle Macromodel and Subcircuit

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TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

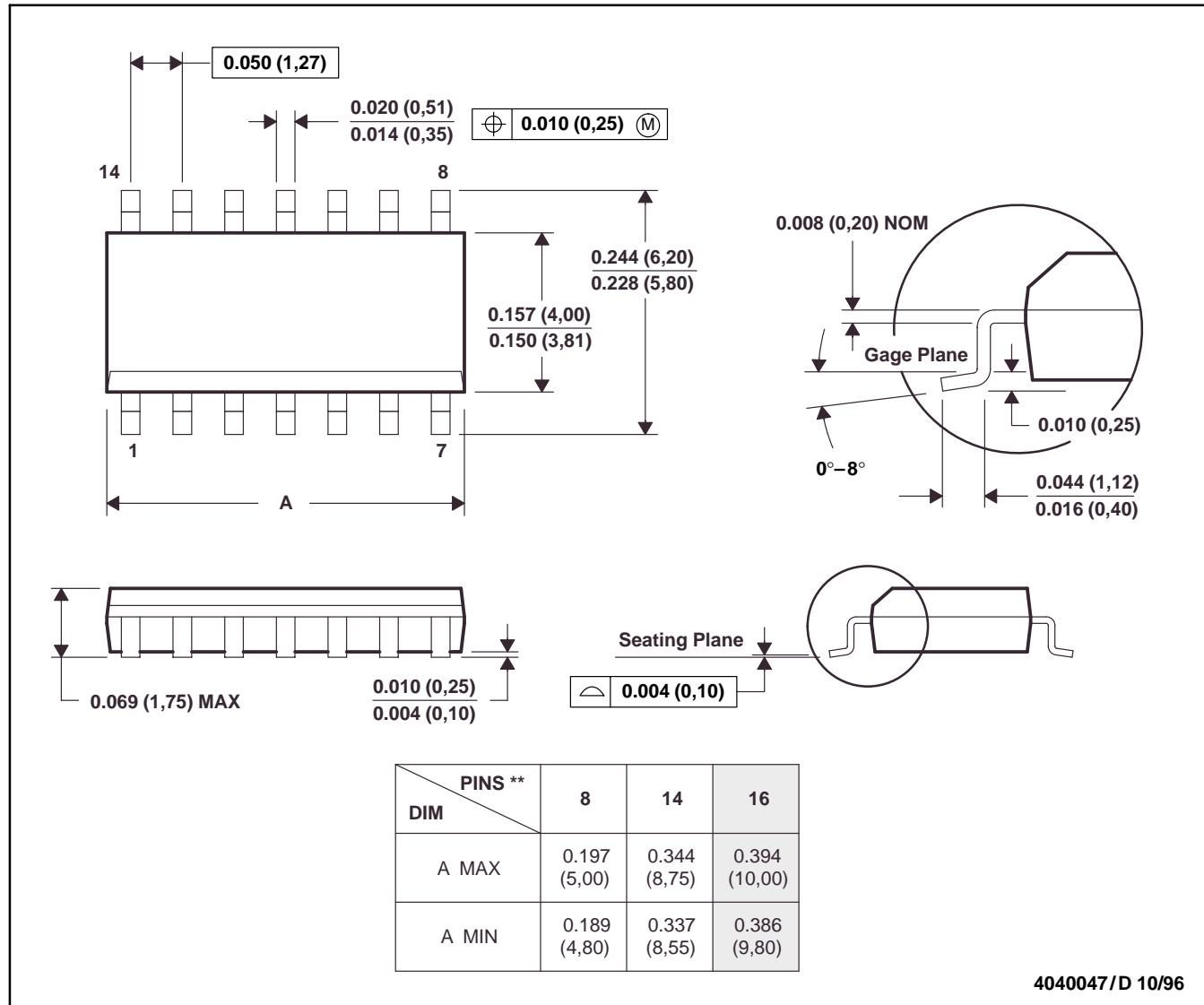
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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MECHANICAL DATA

FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004

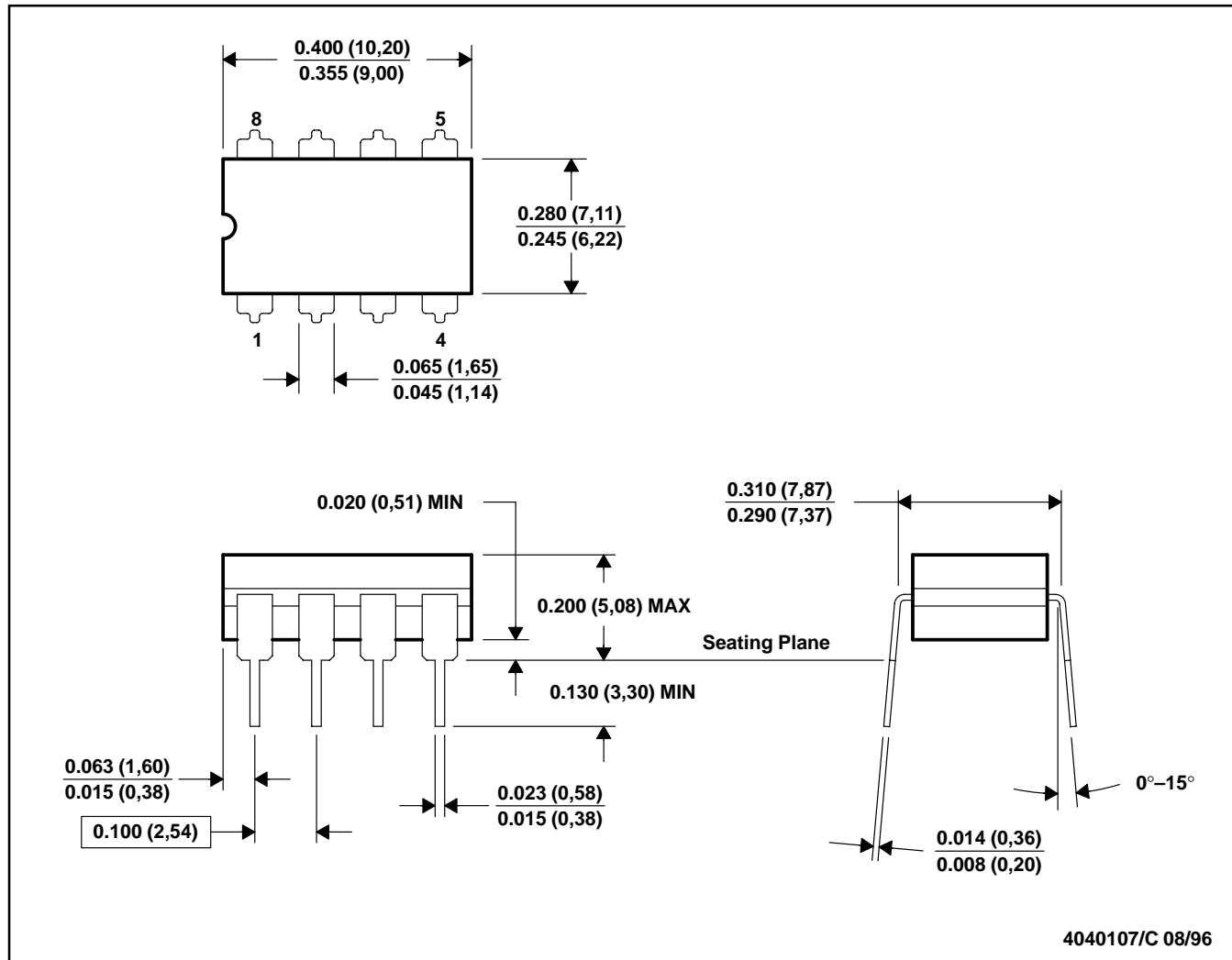
TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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MECHANICAL DATA

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T8



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TLV2442, TLV2442A, TLV2444, TLV2444A
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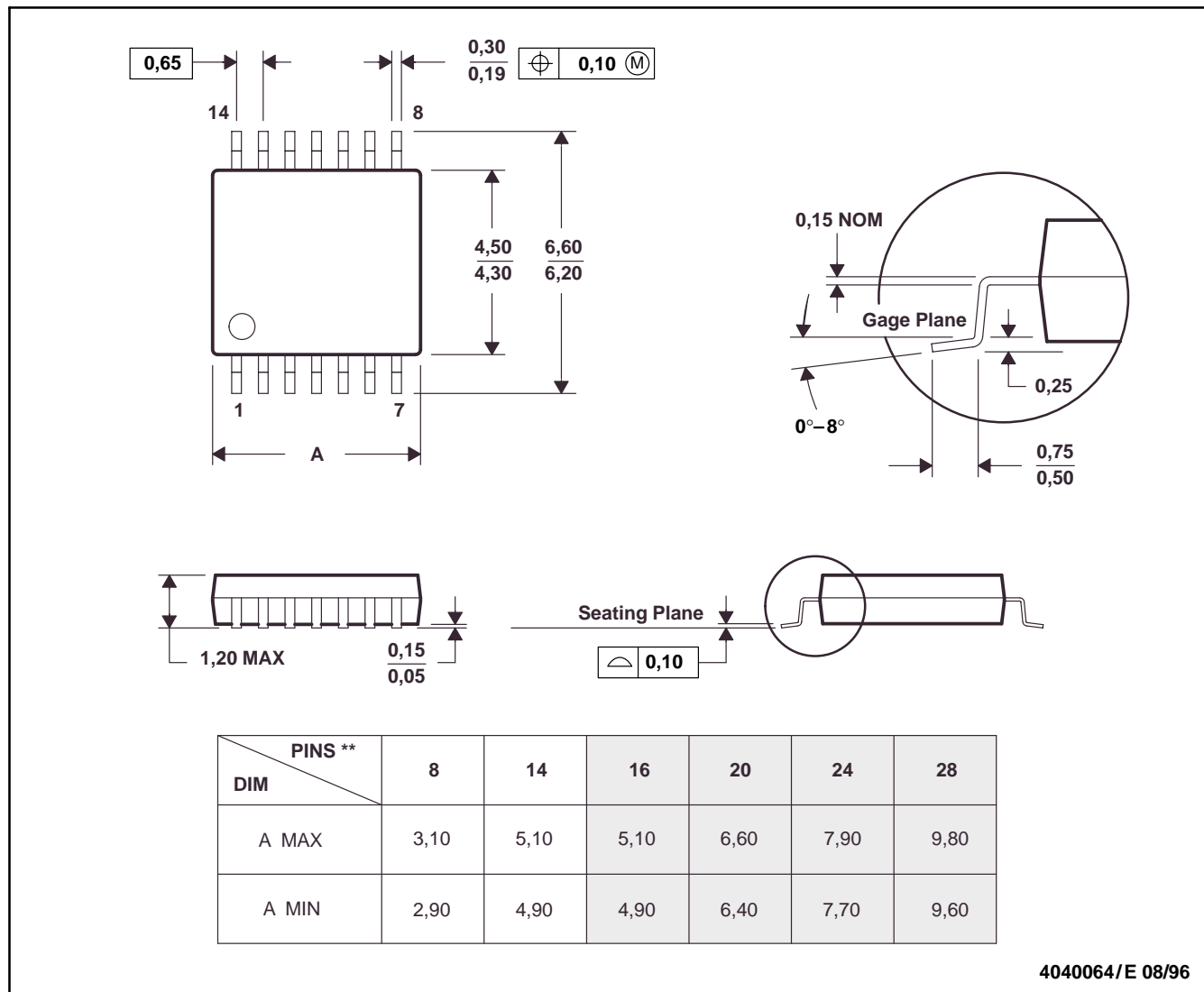
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MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/E 08/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

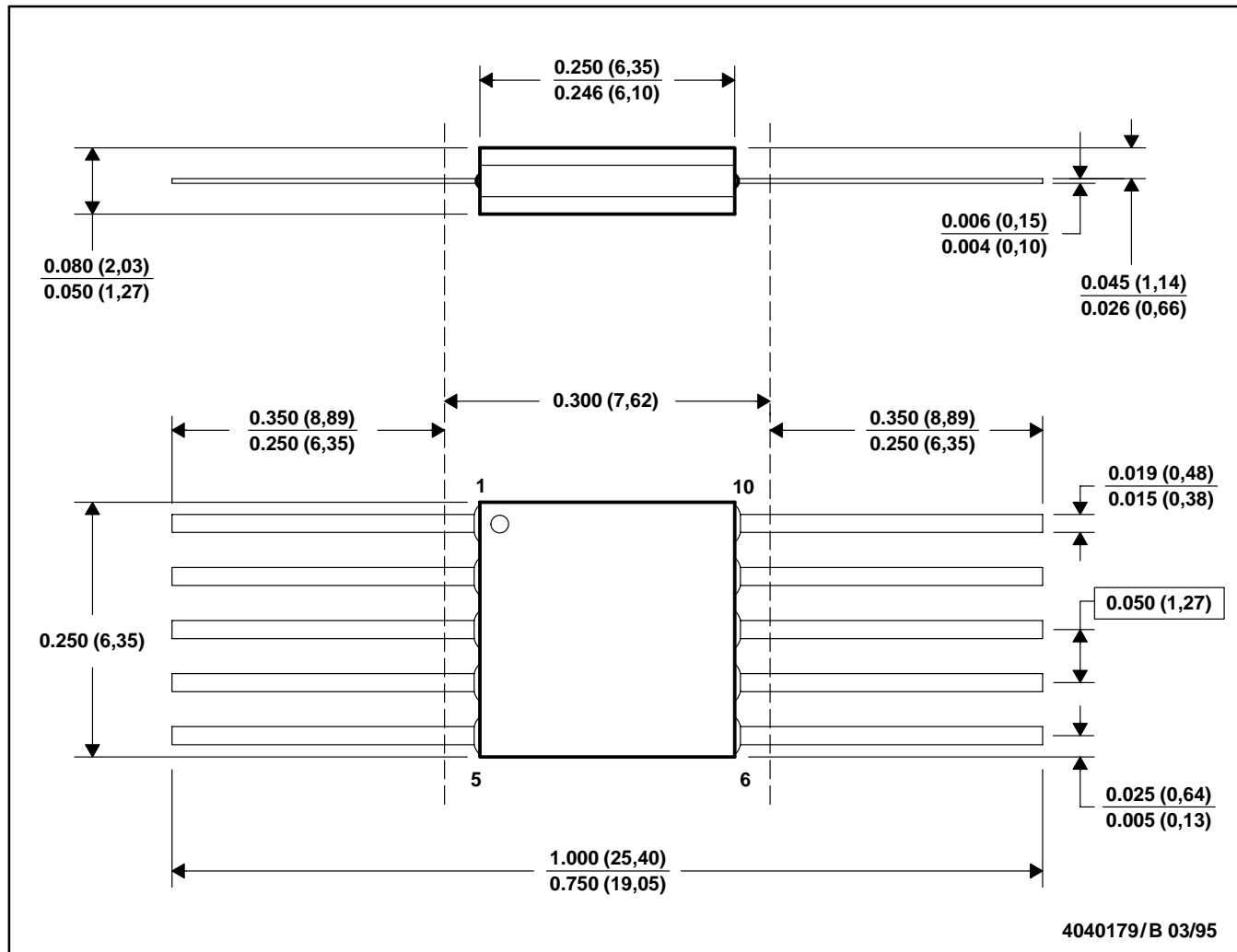
TLV2442, TLV2442A, TLV2444, TLV2444A
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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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MECHANICAL DATA

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9751101Q2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751101Q2A TLV2442 MFKB	
5962-9751101QHA	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751101QHA TLV2442M	
5962-9751101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751101QPA TLV2442M	Samples
5962-9751102Q2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751102Q2A TLV2442 AMFKB	
5962-9751102QHA	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751102QHA TLV2442AM	
5962-9751102QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751102QPA TLV2442AM	Samples
TLV2442AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TV2442	Samples
TLV2442AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TV2442	Samples
TLV2442AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		
TLV2442AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442AI	Samples
TLV2442AMFKB	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751102Q2A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TLV2442 AMFKB	
TLV2442AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751102QPA TLV2442AM	Samples
TLV2442AMUB	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751102QHA TLV2442AM	
TLV2442AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2442A	Samples
TLV2442AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2442A	Samples
TLV2442AQPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2442AQ	Samples
TLV2442AQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2442AQ	Samples
TLV2442CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2442C	Samples
TLV2442CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2442C	Samples
TLV2442CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2442C	Samples
TLV2442CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2442	Samples
TLV2442CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TLV2442CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2442	Samples
TLV2442ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442I	Samples
TLV2442IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442I	Samples
TLV2442IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2442I	Samples
TLV2442MFKB	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751101Q2A TLV2442 MFKB	
TLV2442MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751101QPA TLV2442M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2442MUB	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751101QHA TLV2442M	
TLV2442QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLV2442QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2442Q	Samples
TLV2442QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2442Q	Samples
TLV2442QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2442Q	Samples
TLV2444AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444AI	Samples
TLV2444CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2444CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2444C	Samples
TLV2444ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444I	Samples
TLV2444IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444I	Samples
TLV2444IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444I	Samples
TLV2444IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2444I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2442, TLV2442A, TLV2442AM, TLV2442M, TLV2444A :

- Catalog: [TLV2442A](#), [TLV2442](#)

- Automotive: [TLV2442-Q1](#), [TLV2442A-Q1](#), [TLV2442A-Q1](#), [TLV2442-Q1](#), [TLV2444A-Q1](#)

- Military: [TLV2442M](#), [TLV2442AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2442AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2442AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2442AQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2442CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2442CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2442IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2442IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2442QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2444AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2444CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2444CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2444IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2444IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2442AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2442AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2442AQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2442CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2442CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2442IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV2442IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2442QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2444AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2444CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2444CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2444IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2444IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

JG (R-GDIP-T8)

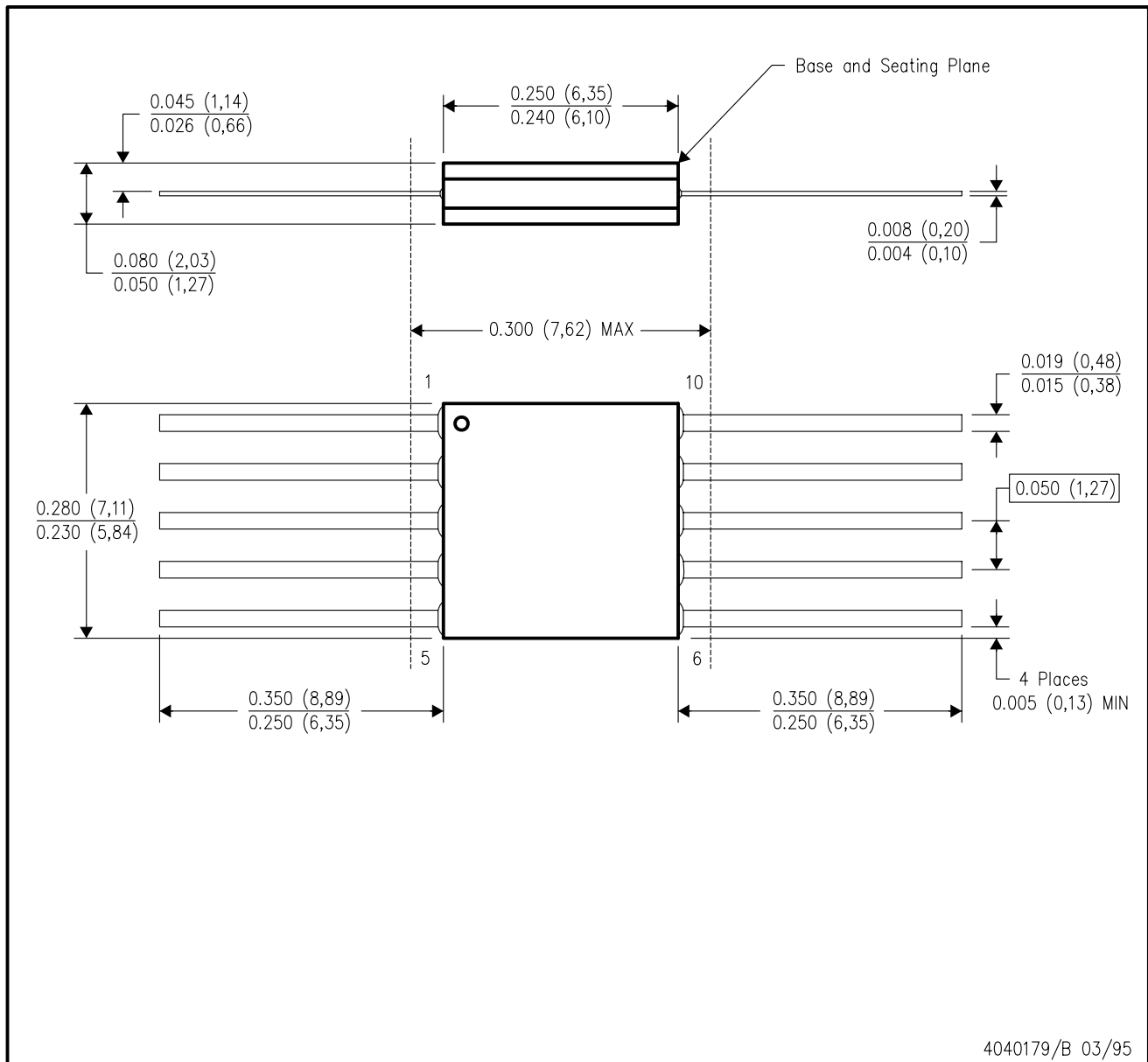
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



4040179/B 03/95

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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