

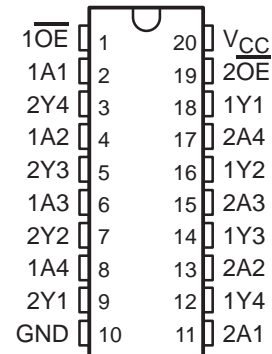
SN74LVT240A

3.3-V ABT OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS134K – SEPTEMBER 1992 – REVISED JANUARY 2004

- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down To 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This octal buffer and line driver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT240A is organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|---------------|-----------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tube | SN74LVT240ADW | LVT240A |
| | | Tape and reel | SN74LVT240ADWR | |
| | SOP – NS | Tape and reel | SN74LVT240ANSR | LVT240A |
| | SSOP – DB | Tape and reel | SN74LVT240ADBR | LX240A |
| | TSSOP – PW | Tube | SN74LVT240APW | LX240A |
| | | Tape and reel | SN74LVT240APWR | |
| TVSOP – DGV | Tape and reel | SN74LVT240ADGVR | LX240A | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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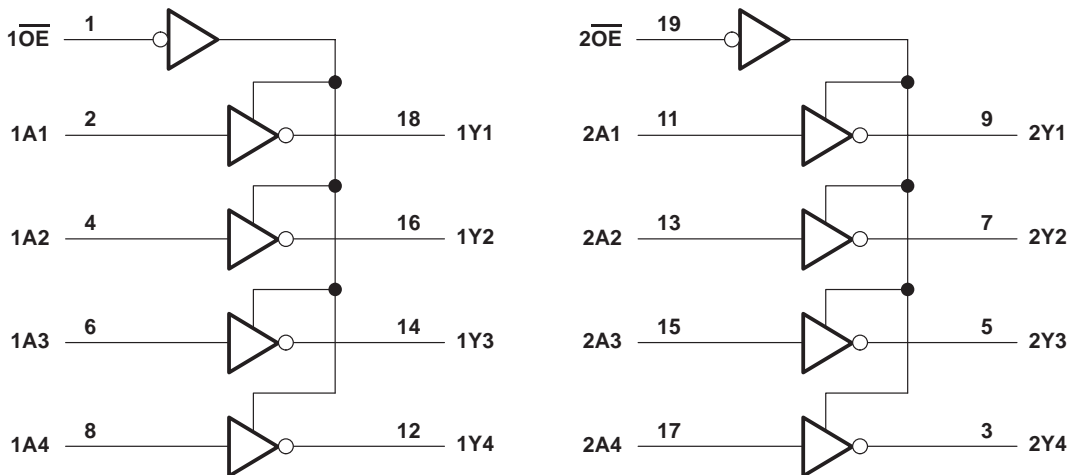
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WITH 3-STATE OUTPUTS

SCBS134K – SEPTEMBER 1992 – REVISED JANUARY 2004

FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): | |
| DB package | 70°C/W |
| DGV package | 92°C/W |
| DW package | 58°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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SCBS134K – SEPTEMBER 1992 – REVISED JANUARY 2004

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----------------|-----|--------|
| V _{CC} | Supply voltage | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | V |
| V _I | Input voltage | | 5.5 | V |
| I _{OH} | High-level output current | | -32 | mA |
| I _{OL} | Low-level output current | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 5 ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | μs/V |
| T _A | Operating free-air temperature | -40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|--|---|------------------------------|------|------|------|
| V _{IK} | V _{CC} = 2.7 V, | I _I = -18 mA | | | -1.2 | V |
| V _{OH} | V _{CC} = 2.7 V to 3.6 V, | I _{OH} = -100 μA | V _{CC} -0.2 | | | V |
| | V _{CC} = 2.7 V, | I _{OH} = -8 mA | 2.4 | | | |
| | V _{CC} = 3 V, | I _{OH} = -32 mA | 2 | | | |
| V _{OL} | V _{CC} = 2.7 V | I _{OL} = 100 μA | | | 0.2 | V |
| | | I _{OL} = 24 mA | | | 0.5 | |
| | V _{CC} = 3 V | I _{OL} = 16 mA | | | 0.4 | |
| | | I _{OL} = 32 mA | | | 0.5 | |
| | | I _{OL} = 64 mA | | | 0.55 | |
| I _I | V _{CC} = 0 or 3.6 V, | V _I = 5.5 V | | | 10 | μA |
| | V _{CC} = 3.6 V | V _I = V _{CC} or GND | Control inputs | ±1 | | |
| | | V _I = V _{CC} | Data inputs | 1 | | |
| | | V _I = 0 | | -5 | | |
| I _{off} | V _{CC} = 0, | V _I or V _O = 0 to 4.5 V | | | ±100 | μA |
| I _{OZH} | V _{CC} = 3.6 V, | V _O = 3 V | | | 5 | μA |
| I _{OZL} | V _{CC} = 3.6 V, | V _O = 0.5 V | | | -5 | μA |
| I _{OZPU} | V _{CC} = 0 to 1.5 V, | V _O = 0.5 V to 3 V, | \overline{OE} = don't care | | ±100 | μA |
| I _{OZPD} | V _{CC} = 1.5 V to 0, | V _O = 0.5 V to 3 V, | \overline{OE} = don't care | | ±100 | μA |
| I _{CC} | V _{CC} = 3.6 V, V _I = V _{CC} or GND | I _O = 0, | Outputs high | | 0.19 | mA |
| | | | Outputs low | | 5 | |
| | | | Outputs disabled | | 0.19 | |
| ΔI _{CC} ‡ | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | | | 0.2 | mA |
| C _i | V _I = 3 V or 0 | | | | 4 | pF |
| C _o | V _O = 3 V or 0 | | | | 7 | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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WITH 3-STATE OUTPUTS

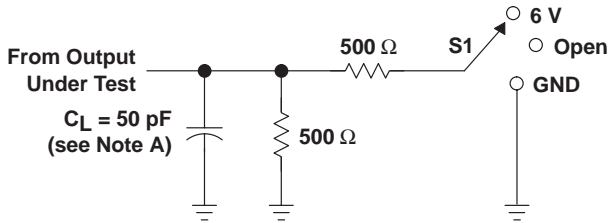
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|---|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1.1 | 2.2 | 3.8 | 4.6 | | ns |
| t_{PHL} | | | 1.3 | 2.6 | 4 | 4.2 | | |
| t_{PZH} | \overline{OE} | Y | 1.1 | 2.6 | 4.6 | 5.6 | | ns |
| t_{PZL} | | | 1.4 | 2.7 | 4.4 | 5 | | |
| t_{PHZ} | \overline{OE} | Y | 2 | 2.9 | 4.4 | 4.6 | | ns |
| t_{PLZ} | | | 1.8 | 3 | 4.3 | 4.3 | | |

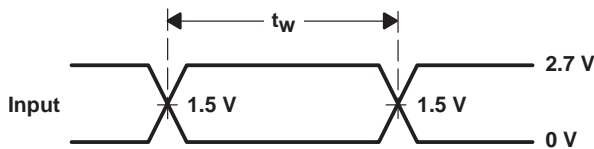
† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

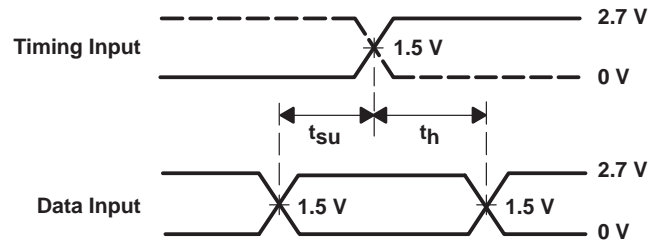


LOAD CIRCUIT

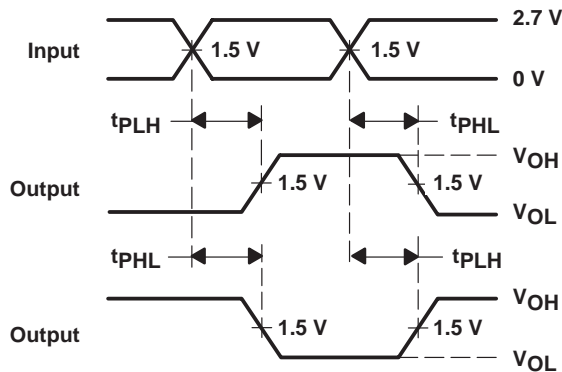
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



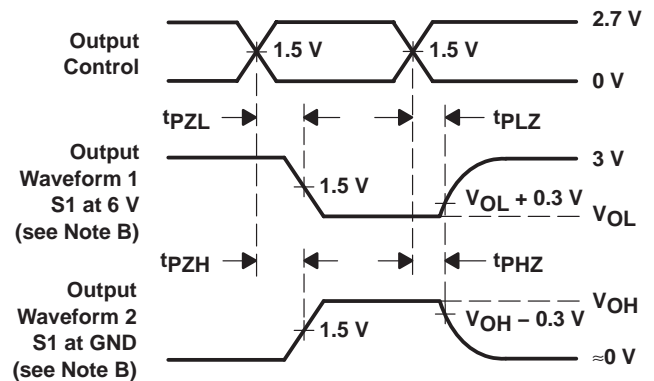
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVT240ADBG4 | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADGVRE4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT240APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

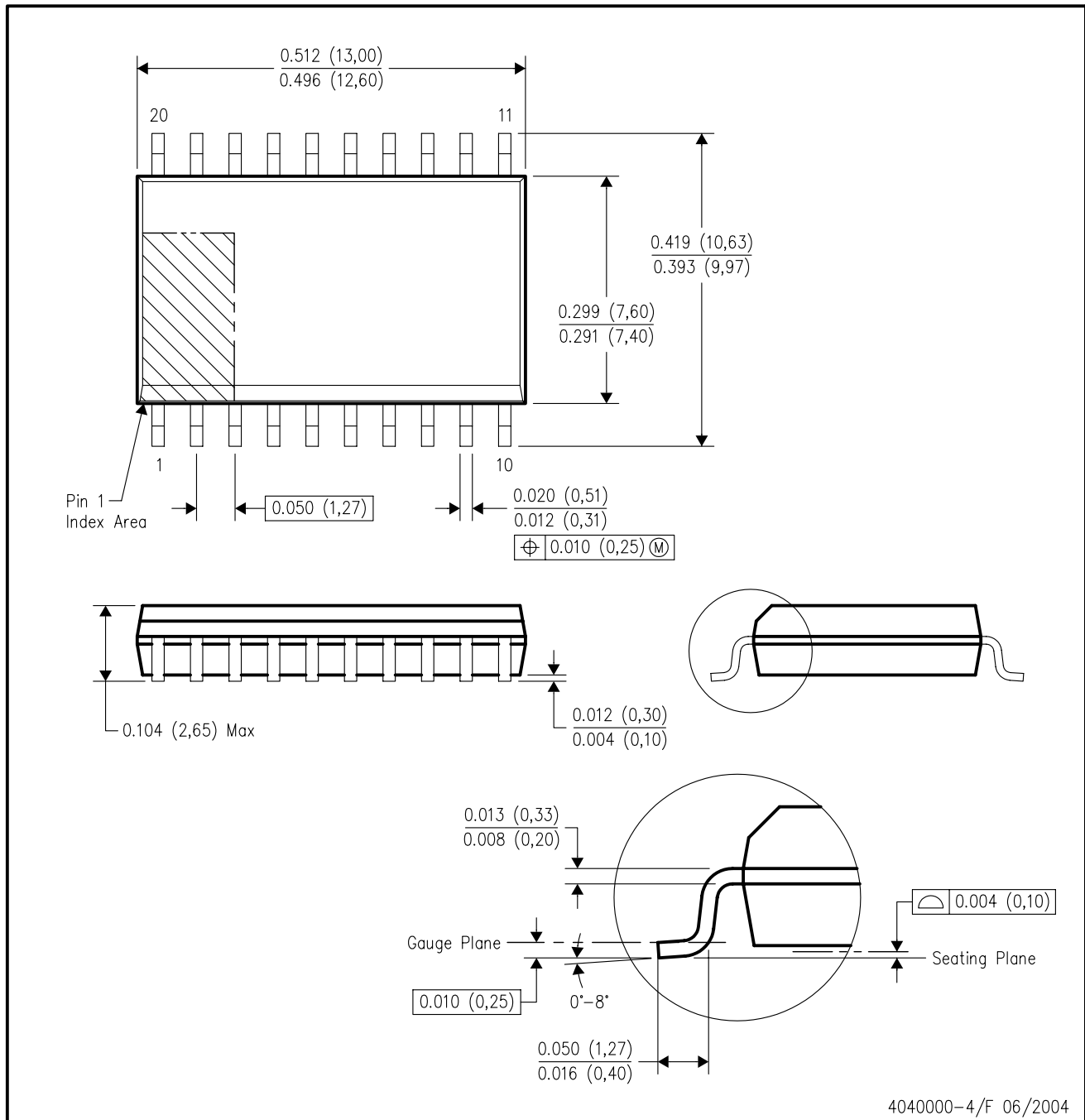
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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