



MOTOROLA

Product Preview

Dual D-Type Positive Edge-Triggered Flip-Flop

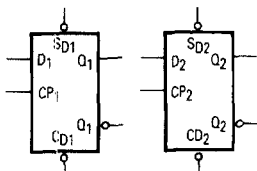
The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs

LOGIC SYMBOL



PIN NAMES

- D₁, D₂ Data Inputs
- CP₁, CP₂ Clock Pulse Inputs
- \bar{C}_D1 , \bar{C}_D2 Direct Clear Inputs
- \bar{S}_D1 , \bar{S}_D2 Direct Set Inputs
- Q₁, \bar{Q}_1 , Q₂, \bar{Q}_2 Outputs

TRUTH TABLE (Each Half)

Inputs				Outputs	
\bar{S}_D	\bar{C}_D	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	\uparrow	H	H	L
H	H	\downarrow	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 \uparrow = LOW-to-HIGH Clock Transition
 $Q_0(\bar{Q}_0)$ = Previous Q(\bar{Q}) before LOW-to-HIGH Transition of Clock

**MC74AC74
MC74ACT74**

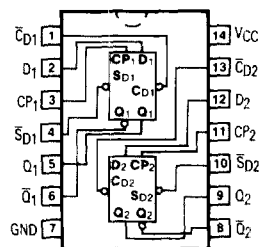
**DUAL D-TYPE POSITIVE
EDGE-TRIGGERED
FLIP-FLOP**



**N SUFFIX
CASE 646-06
PLASTIC**



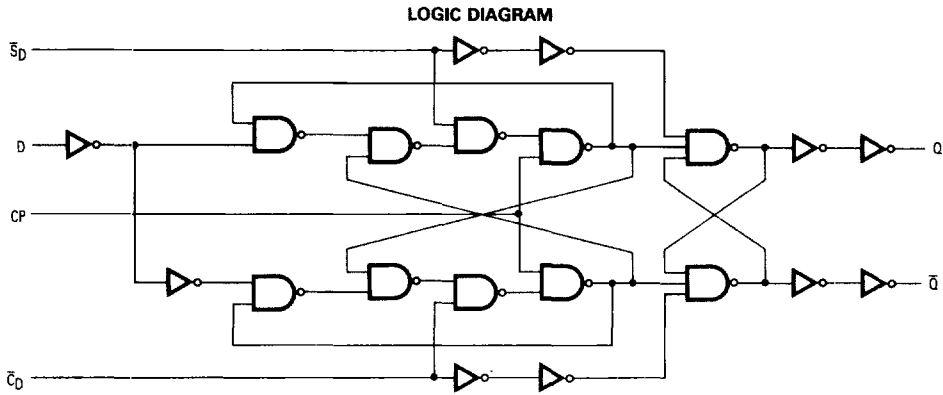
**D SUFFIX
CASE 751A-02
PLASTIC**



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC74AC74 • MC74ACT74



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V, T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V, T_A = 25^\circ C$
I_{CCT}	Maximum Additional I_{CC} /Input (ACT74)	1.5	mA	$V_{IN} = V_{CC} - 2.1 V, V_{CC} = 5.5 V, T_A = \text{Worst Case}$

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}^* (V)	74AC			74AC		Units	Fig. No.
			$T_A = +25^\circ C, C_L = 50 pF$			$T_A = -40^\circ C \text{ to } +85^\circ C, C_L = 50 pF$			
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 125		MHz	3-3
t_{PLH}	Propagation Delay C_{Dn} or S_{Dn} to Q_n or \bar{Q}_n	3.3 5.0	1.0 1.0	8.0 6.0	12 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay C_{Dn} or S_{Dn} to Q_n or \bar{Q}_n	3.3 5.0	1.0 1.0	10.5 8.0	12 9.5	1.0 1.0	13.5 10.5	ns	3-6
t_{PLH}	Propagation Delay CP_n to Q_n or \bar{Q}_n	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10	1.0 1.0	16 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or \bar{Q}_n	3.3 5.0	1.0 1.0	8.0 6.0	14 10	1.0 1.0	14.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP _n	3.3 5.0	1.5 1.0	4.0 3.0	4.5 3.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP _n	3.3 5.0	-2.0 -1.5	0 0	0 0	ns	3-9	
t _w	CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns	3-6	
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	3.3 5.0	-2.5 -2.0	0 0	0 0	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	145	210		125		MHz	3-3
t _{PLH}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n	5.0	1.0	6.0	10	1.0	11.5	ns	3-6
t _{PLH}	Propagation Delay CP _n to Q _n or \overline{Q}_n	5.0	1.0	7.5	11	1.0	13	ns	3-6
t _{PHL}	Propagation Delay CP _n to Q _n or \overline{Q}_n	5.0	1.0	6.0	10	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP _n	5.0	1.0	3.0	3.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP _n	5.0	-0.5	1.0	1.0	ns	3-9	
t _w	CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width	5.0	3.0	5.0	6.0	ns	3-6	
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	5.0	-2.5	0	0	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
CPD	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V