

## 74AC/ACT11109

### Dual J-K̄ Flip-Flop with Set and Reset; Positive Edge-Triggered

#### Product Specification

#### ACL Products

#### FEATURES

- Output capability:  $\pm 24$  mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- $50\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: SSI

#### DESCRIPTION

The 74AC/ACT11109 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11109 provides two J-K̄ flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and  $\bar{Q}$  outputs.

Set ( $\bar{S}_n$ ) and Reset ( $\bar{R}_n$ ) are asynchronous active-Low inputs and operate independently of the Clock input.

Information at the J and  $\bar{K}$  inputs is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The J and  $\bar{K}$  inputs must be stable one set-

#### GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay $CP_n$ to $Q_n$ or $\bar{Q}_n$	$C_L = 50\text{pF}$	5.3	5.8	ns
$C_{PD}$	Power dissipation capacitance per flip-flop <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	32	31	pF
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	3.5	3.5	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50\text{pF}$	125	125	MHz

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O)$$
 where:

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

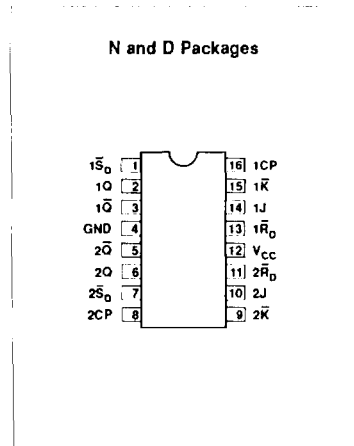
$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

#### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11109N 74ACT11109N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11109D 74ACT11109D

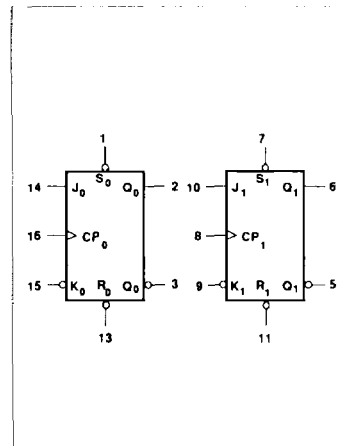
up time prior to the Low-to-High clock transition for predictable operation. The J and  $\bar{K}$  inputs may be tied together to allow operation as a D flip-flop.

#### PIN CONFIGURATION



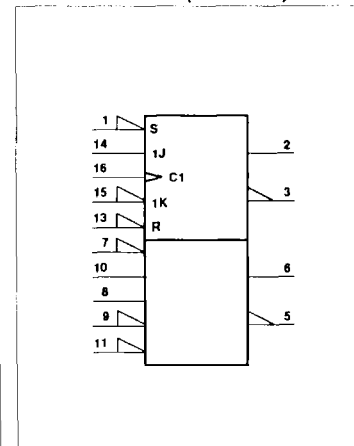
April 14, 1988

#### LOGIC SYMBOL



5-94

#### LOGIC SYMBOL (IEEE/IEC)



853-1341 92942

# Dual J-K Flip-Flop with Set and Reset; Positive Edge-Triggered

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 10	$J_0 - J_1$	Data inputs
15, 9	$\bar{K}_0 - \bar{K}_1$	Data inputs
2, 6	$Q_0 - Q_1$	Data outputs
3, 5	$\bar{Q}_0 - \bar{Q}_1$	Data outputs (complements of $Q_n$ outputs)
1, 7	$\bar{S}_0 - \bar{S}_1$	Set inputs (active Low)
13, 11	$\bar{R}_0 - \bar{R}_1$	Reset inputs (active Low)
16, 8	$CP_0 - CP_1$	Clock inputs
4	GND	Ground (0V)
12	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}$	$\bar{R}$	CP	J	$\bar{K}$	Q	$\bar{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined <sup>1</sup>	L	L	X	X	X	H	H
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Toggle	H	H	↑	h	l	$\bar{q}$	q
No change - hold	H	H	L	X	X	$Q_0$	$\bar{Q}_0$

H = High voltage level steady state

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level steady state

l = Low voltage level one set-up time prior to the Low-to-High clock transition

X = Don't care

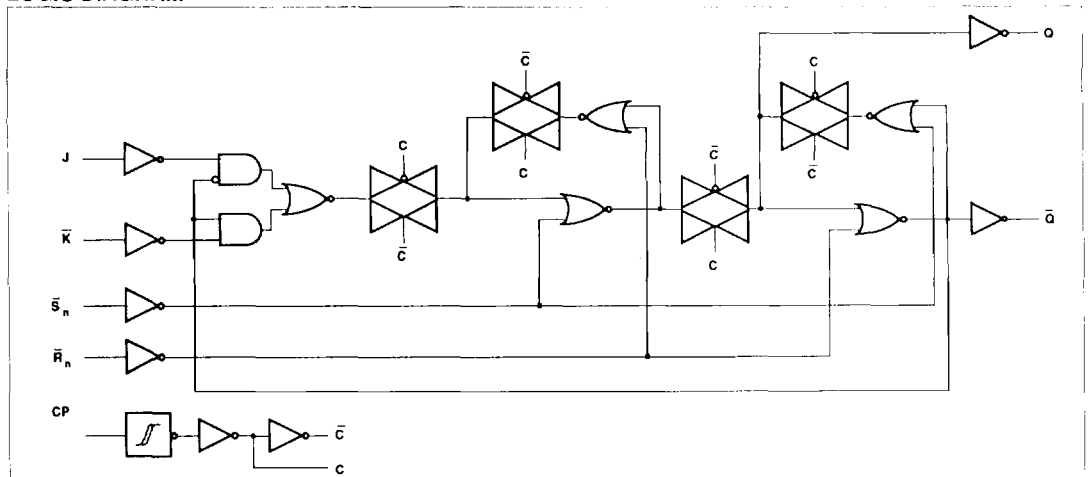
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition

↑ = Low-to-High clock transition

### NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

## LOGIC DIAGRAM



# Dual J-K̄ Flip-Flop with Set and Reset; Positive Edge-Triggered

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11109			74ACT11109			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$	Operating free-air temperature	-40		+85	-40		+85	°C

### NOTE:

1. No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		±100	mA
	DC ground current		±100	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package	Above 70°C: derate linearly by 6mW/K	400	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11109				74ACT11109				UNIT	
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
			I <sub>OH</sub> = -24mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
I <sub>OH</sub> = -75mA <sup>1</sup>	5.5			3.85				3.85					
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I <sub>OL</sub> = 24mA	3.0		0.36		0.44		0.36			0.44
				4.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5		4.0		40		4.0		40	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum clock frequency	1	70	100		70		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	1	1.5	8.0	11.4	1.5	12.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> , R̄ <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	2	1.5	6.5	9.0	1.5	9.9	ns
t <sub>S</sub>	Setup time, High or Low J <sub>n</sub> or R̄ <sub>n</sub> to CP <sub>n</sub>	1	5.5			5.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>n</sub> to J <sub>n</sub> or R̄ <sub>n</sub>	1	0			0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	7.2			7.2		ns
t <sub>W</sub>	S <sub>n</sub> or R̄ <sub>n</sub> pulse width, Low	2	5.0			5.0		ns
t <sub>REC</sub>	Recovery time S <sub>n</sub> or R̄ <sub>n</sub> to CP <sub>n</sub>	3	2.5			2.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum clock frequency	1	100	125		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	1	1.5	5.5	7.9	1.5	8.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> , R̄ <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	2	1.5	4.5	6.5	1.5	7.1	ns
t <sub>S</sub>	Setup time, High or Low J <sub>n</sub> or R̄ <sub>n</sub> to CP <sub>n</sub>	1	4.5			4.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>n</sub> to J <sub>n</sub> or R̄ <sub>n</sub>	1	0			0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.0			5.0		ns
t <sub>W</sub>	S <sub>n</sub> or R̄ <sub>n</sub> pulse width, Low	2	4.0			4.0		ns
t <sub>REC</sub>	Recovery time S <sub>n</sub> or R̄ <sub>n</sub> to CP <sub>n</sub>	3	2.0			2.0		ns

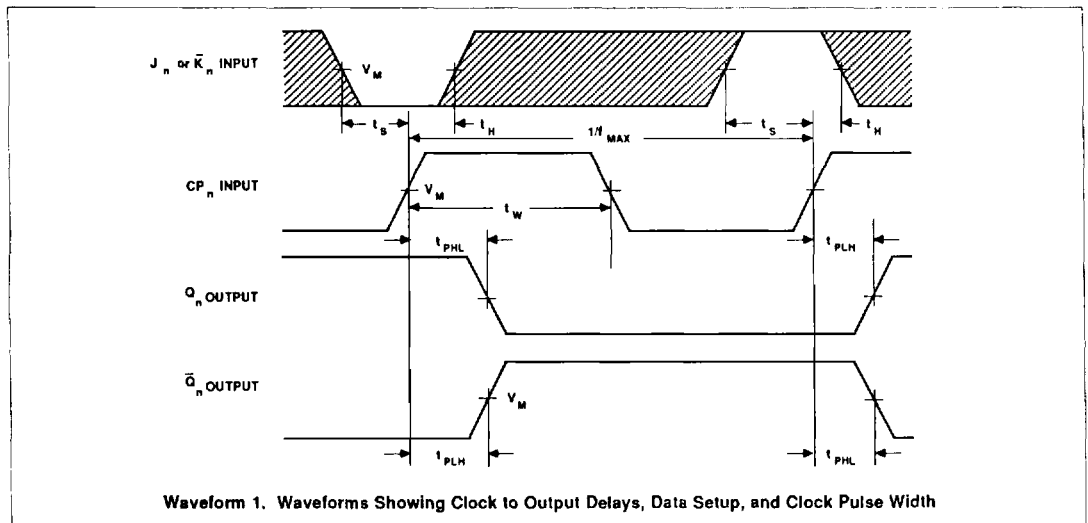
Dual J-K̄ Flip-Flop with Set and Reset;  
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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11109					UNIT
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum clock frequency	1	100	125		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	1	1.5 1.5	6.0 5.5	8.3 7.6	1.5 1.5	9.1 8.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S̄ <sub>n</sub> , R̄ <sub>n</sub> to Q <sub>n</sub> , Q̄ <sub>n</sub>	2	1.5 1.5	5.5 6.0	8.6 10.8	1.5 1.5	9.2 11.8	ns
t <sub>S</sub>	Setup time, High or Low J <sub>n</sub> or K̄ <sub>n</sub> to CP <sub>n</sub>	1	5.5			5.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>n</sub> to J <sub>n</sub> or K̄ <sub>n</sub>	1	0			0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.0			5.0		ns
t <sub>W</sub>	S̄ <sub>n</sub> or R̄ <sub>n</sub> pulse width, Low	2	5.5			5.5		ns
t <sub>REC</sub>	Recovery time S̄ <sub>n</sub> or R̄ <sub>n</sub> to CP <sub>n</sub>	3	2.0			2.0		ns

AC WAVEFORMS

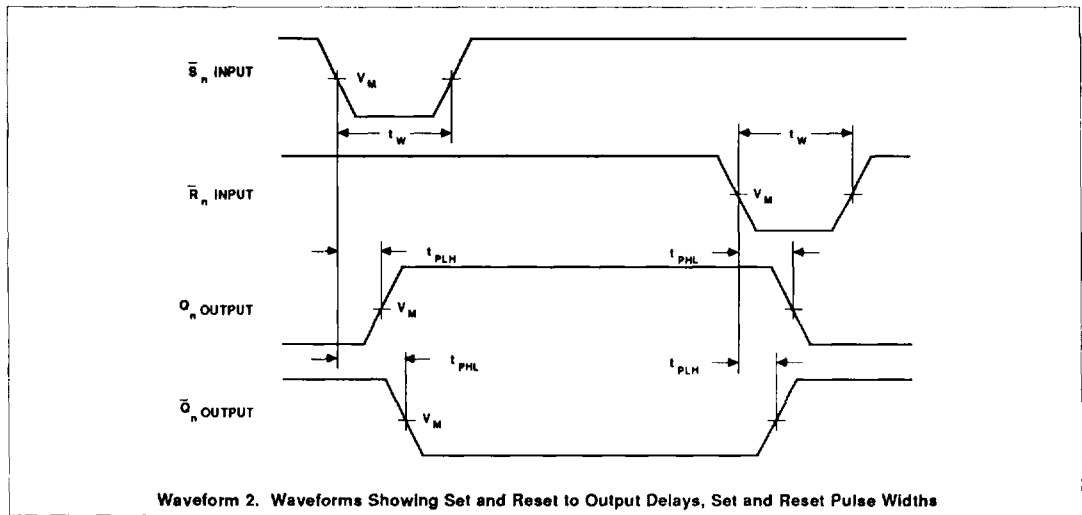


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

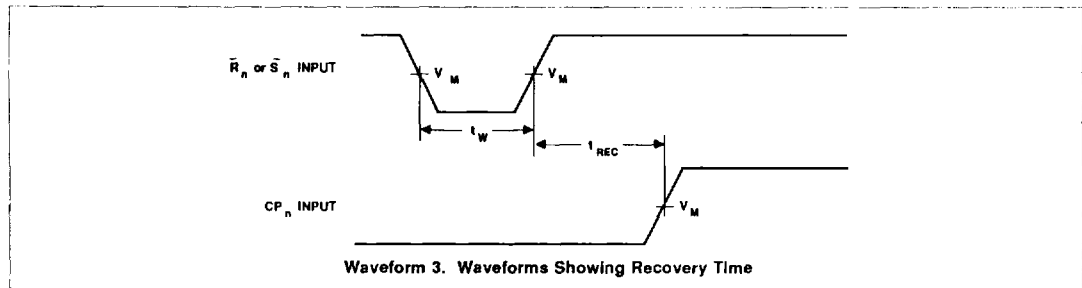
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AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths



Waveform 3. Waveforms Showing Recovery Time

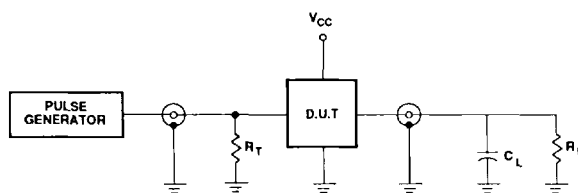
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0\text{V}$ $V_M = 1.5\text{V}$	$V_M = 50\% V_{CC}$

# Dual J- $\bar{K}$ Flip-Flop with Set and Reset; Positive Edge-Triggered

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## TEST CIRCUIT



Test Circuit

### DEFINITIONS

$C_L$  = Load capacitance, 50pF; includes jig and probe capacitance

$R_L$  = Load resistor, 500 $\Omega$

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators

Input pulses: PRR  $\leq$  10MHz

$t_r = t_f = 3ns$