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Low-Voltage 1:20 Differential ECL/PECL Clock Driver

MC100EP221

See Upgrade Product – MC100ES6221

LOW–VOLTAGE
1:20 DIFFERENTIAL
ECL/PECL CLOCK DRIVER

TB SUFFIX
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The MC100EP221 is a low skew 1–to–20 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The input signals can be either differential or single–ended if the V_{BB} output is used. The selected signal is fanned out to 20 identical differential outputs.

- 270ps max. Part–to–Part Skew
- 50ps max. Output–to–Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Supports 3.3V and 2.5V, ECL and PECL Operation
- Supports HSTL and PECL Clock Systems

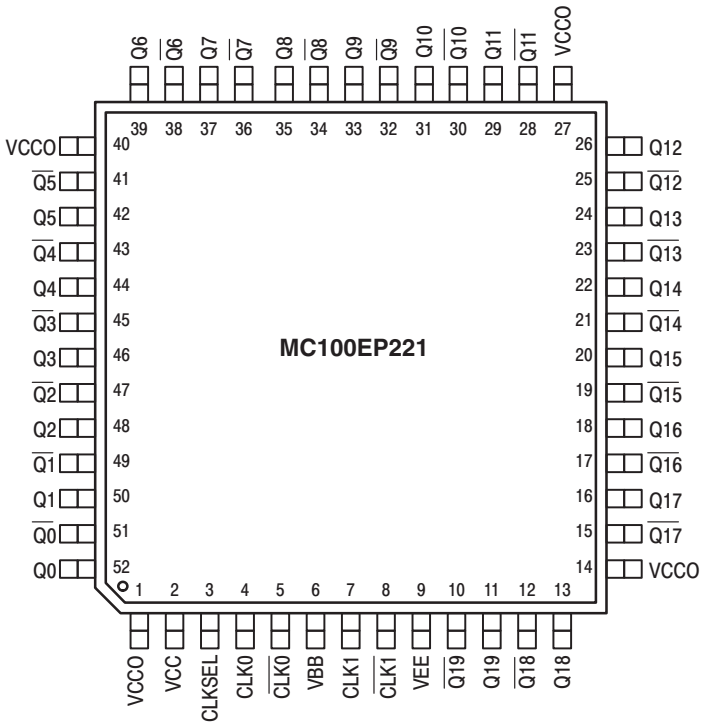
The EP221 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP221, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP221 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP221's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

Rev 1

Pinout: 52–Lead LQFP
(Top View)



FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{CLK0}$
1	CLK1, $\overline{CLK1}$

LOGIC SYMBOL

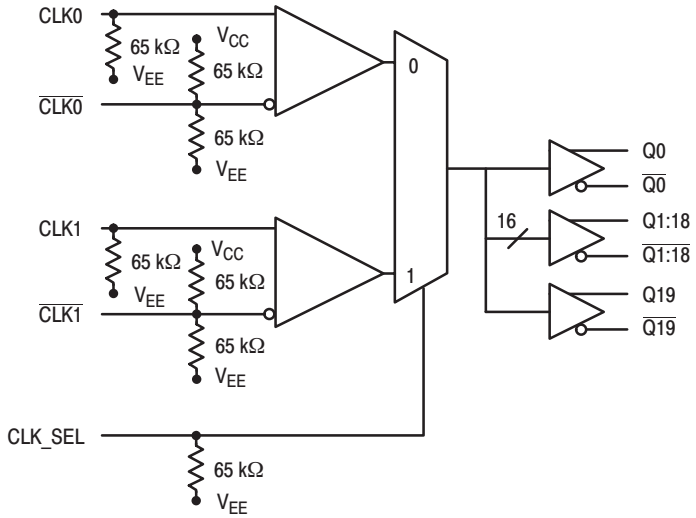


Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{CLK0}$	Input	ECL/LVPECL	Differential reference clock signal input
CLK1, $\overline{CLK1}$	Input	ECL/LVPECL or HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	LVPECL	Output frequency divider select
Q[0-19], $\overline{Q[0\text{-}19]}$	Output	LVPECL	Differential clock outputs
VEE[a]	Supply		Negative power supply
V_{CC}, V_{CCO}	Supply		Positive power supply. All V_{CC} and V_{CCO} pins must be connected to the positive power supply for correct DC and AC operation
VBB	Output		DC bias output for single ended input operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V.
In both modes, the input and output levels are referrenced to the most positive supply (VCC).

Table 2: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} - 2[a]		V	
MM	ESD Protection (Machine model)	75			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	500			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient	See application information[b]				
θ_{JC}	Thermal resistance junction to case	See application information				

a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase.
b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this data-sheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationsship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP221.

Table 4: PECL and HSTL DC Characteristics (V_{CCO} = V_{CC} = 2.375V to 3.8V, V_{EE} = GND)

Symbol	Characteristics	T_A = -40°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[a] (LVPECL differential signals)									
V_{PP}	Differential input voltage[b] V_{CC}=3.3V	0.10		0.10		0.10		V	
	V_{CC}=2.5V	0.15		0.15		0.15		V	
V_{CMR}	Differential cross point voltage[c] CLK0	1.0	V_{CC}-0.4	1.0	V_{CC}-0.4	1.0	V_{CC}-0.4	V	
	CLK1	0.1	V_{CC}-1.0	0.1	V_{CC}-1.0	0.1	V_{CC}-1.0	V	
Clock input pair CLK1, $\overline{CLK1}$[d] (HSTL differential signals)									
V_{DIF}	Differential input voltage[e] V_{CC}=3.3V	0.4	1.0	0.4	1.0	0.4	1.0	V	
	V_{CC}=2.5V	0.4	1.0	0.4	1.0	0.4	1.0	V	
V_X	Differential cross point voltage[f]	0.68	0.9	0.68	0.9	0.68	0.9	V	
V_{IH}	Input high voltage	V_X+0.2	V_X+0.5	V_X+0.2	V_X+0.5	V_X+0.2	V_X+0.5	V	
V_{IL}	Input low voltage	V_X-0.5	V_X-0.2	V_X-0.5	V_X-0.2	V_X-0.5	V_X-0.2	V	
All inputs (LVPECL single ended signals)									
V_{IH}	Input high voltage	V_{CC}-1.165	V_{CC}-0.880	V_{CC}-1.165	V_{CC}-0.880	V_{CC}-1.165	V_{CC}-0.880	V	
V_{IL}	Input low voltage	V_{CC}-1.810	V_{CC}-1.480	V_{CC}-1.810	V_{CC}-1.480	V_{CC}-1.810	V_{CC}-1.480	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{CC} to V_{EE}
LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$)									
V_{OH}	Output High Voltage	V_{CC}-1.20	V_{CC}-0.82	V_{CC}-1.15	V_{CC}-0.82	V_{CC}-1.15	V_{CC}-0.82	V	I_{OH}= -30mA[g]
V_{OL}	Output Low Voltage	V_{CC}-1.90	V_{CC}-1.40	V_{CC}-1.90	V_{CC}-1.40	V_{CC}-1.9	V_{CC}-1.40	V	I_{OL}= -5mA[g]
Supply current and V_{BB}									
I_{EE}	Max. Supply Current		190		190		190	mA	V_{EE} pin
I_{CC}	Max. Supply Current[h]		750		750		750	mA	V_{CC} pins
V_{BB}	Output reference voltage[i] V_{CC}=3.3V	V_{CC}-1.35	V_{CC}-1.24	V_{CC}-1.35	V_{CC}-1.24	V_{CC}-1.35	V_{CC}-1.24	V	
	V_{CC}=2.5V	V_{CC}-1.35	V_{CC}-1.24	V_{CC}-1.35	V_{CC}-1.22	V_{CC}-1.35	V_{CC}-1.22	V	

a. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL and LVPECL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
b. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
d. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
e. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality. Only applicable to CLK1, $\overline{CLK1}$.
f. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
g. Equivalent to an output termination of 50Ω to V_{TT}.
h. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
i. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 5: ECL DC Characteristics (V_{CC} = V_{CCO} = GND, V_{EE} = -3.8V to -2.375V)

Symbol	Characteristics	T_A = -40°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[a] for ECL differential signals									
V_{PP}	Differential input voltage[b]								
	V_{EE}=-3.3V	0.10		0.10		0.10		V	
	V_{EE}=-2.5V	0.15		0.15		0.15		V	
V_{CMR}	Differential cross point voltage[c]								
	CLK0	V_{EE}+1.0	-0.4	V_{EE}+1.0	-0.4	V_{EE}+1.0	-0.4	V	
	CLK1	V_{EE}+0.1	–1.0	V_{EE}+0.1	–1.0	V_{EE}+0.1	–1.0	V	
All inputs ECL single ended signals									
V_{IH}	Input high voltage	-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V	
V_{IL}	Input low voltage	-1.810	-1.480	-1.810	-1.480	-1.810	-1.480	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{EE} to V_{CC}
LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$)									
V_{OH}	Output High Voltage	-1.20	-0.82	-1.20	-0.82	-1.20	-0.82	V	I_{OH}= -30 mA[d]
V_{OL}	Output Low Voltage	-1.90	-1.40	-1.90	-1.40	-1.90	-1.40	V	I_{OL}= -5 mA[d]
Supply current and V_{BB}									
I_{EE}	Max. Supply Current		190		190		190	mA	V_{EE} pin
I_{CC}	Max. Supply Current[e]		750		750		750	mA	V_{CC} Pins
V_{BB}	Output reference voltage[f]								
	V_{EE}=-3.3V	-1.35	-1.24	-1.35	-1.24	-1.35	-1.24	V	
	V_{EE}=-2.5V	-1.35	-1.24	-1.35	-1.22	-1.35	-1.22	V	

a. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
b. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
d. Equivalent to an output termination of 50Ω to V_{TT}.
e. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
f. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

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Table 6: PECL/ECL/HSTL AC Characteristics[a] (V_{CC} = V_{CCO} = 2.375V to 3.8V, V_{EE} = GND) or (V_{EE} = -3.8V to -2.375V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristics	T_A = -40°C			T_A = 25°C			T_A = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[b] for PECL differential signals												
V_{PP}	Differential input voltage[c] (peak-to-peak)	0.5		1.0	0.5		1.0	0.5		1.0	V	
V_{CMR}	Differential cross point voltage[d] CLK0 CLK1	1.0 0.3		V_{CC}-0.4 V_{CC}-1.3	1.0 0.3		V_{CC}-0.4 V_{CC}-1.3	1.0 0.3		V_{CC}-0.4 V_{CC}-1.3	V V	
f_{CLK}	Input Frequency (PECL)	0		1.0			1.0			1.0	GHz	
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ for ECL differential signals												
V_{PP}	Differential input voltage (peak-to-peak)	0.5		1.0	0.5		1.0	0.5		1.0	V	
V_{CMR}	Differential cross point voltage CLK0 CLK1	V_{EE}+1.0 V_{EE}+0.3		-0.4 -1.3	V_{EE}+1.0 V_{EE}+0.3		-0.4 –1.3	V_{EE}+1.0 V_{EE}+0.3		-0.4 -1.3	V V	
f_{CLK}	Input Frequency (ECL)	0		1.0			1.0			1.0	GHz	
Clock input pair CLK1, $\overline{CLK1}$ for HSTL differential signals												
V_{DIF}	Differential input voltage[e] (peak-to-peak) CLK1	0.4		1.0	0.5		1.0	0.5		1.0	V	
V_X	Differential cross point voltage[f] CLK1	0.68		0.9	0.68		0.9	0.68		0.9	V	
f_{CLK}	Input Frequency (HSTL)	0		1.0			1.0			1.0	GHz	
PECL/ECL clock outputs (Q0-19, $\overline{Q0-19}$)												
t_{PD}	Propagation Delay CLK_0 to Qx CLK_1 to Qx	350 370	460 500	600 640	390 440	520 570	660 710	480 530	630 680	750 800	ps ps	Diff. Diff.
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) f_O < 50 MHz f_O < 0.8 GHz f_O < 1.0 GHz	450 400 375			550 500 400			550 500 400			mV mV mV	
$t_{sk(O)}$	Output-to-output skew (within device)		30	50		30	50		30	50	ps	Diff.
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			270			270			270	ps	Diff.
$t_{JIT(CC)}$	Output cycle-to-cycle jitter (RMS)			TBD			TBD			TBD	ps	
DC_O	Output duty cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%	DC_{fref}= 50%
t_r, t_f	Output Rise/Fall Time	100		500	100		500	100		500	ps	20% to 80%

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
c. V_{PP} (AC) is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. V_{CMR} (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay and part-to-part skew.
e. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics. Only applicable to CLK1.
f. V_X (AC) is the crosspoint of the differential HSTL input signal. AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay and part-to-part skew.

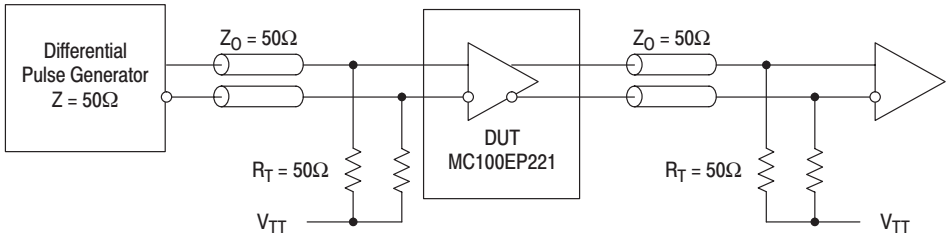

Figure 1. MC100EP221 AC test reference

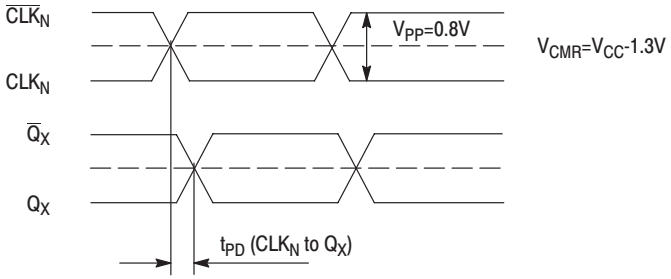

Figure 2. MC100EP221 AC reference measurement waveform

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APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP221

The MC100EP221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP221 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 3 “Recommended thermal land pattern”, providing an efficient heat removal path.

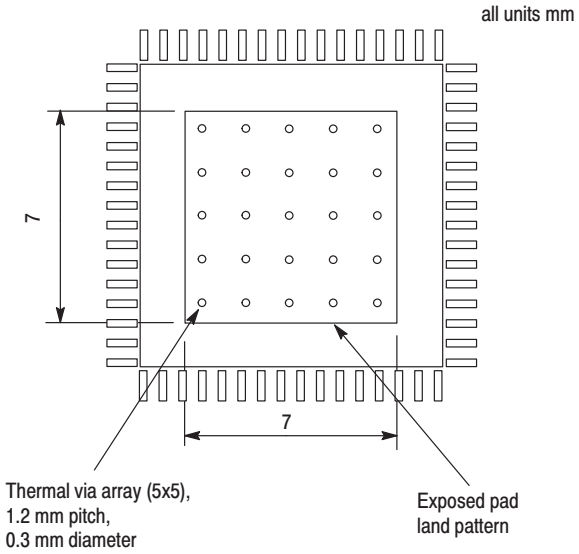

Figure 3. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 4 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 4 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

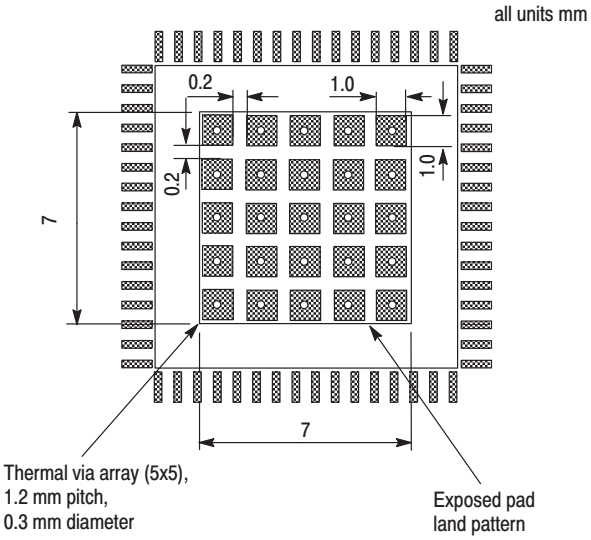

Figure 4. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 7: Thermal Resistance[a]

Convection-LFPM	R_{THJA}[b] °C/W	R_{THJA}[c] °C/W	R_{THJC}[d] °C/W	R_{THJB}[e] °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.