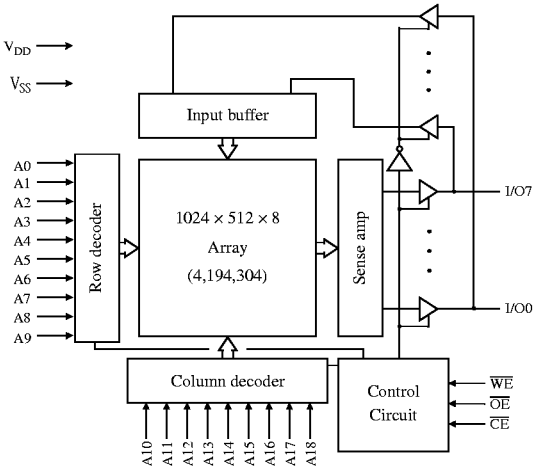
3.3V 512K×8 Intelliwatt™ low power CMOS SRAM

Features

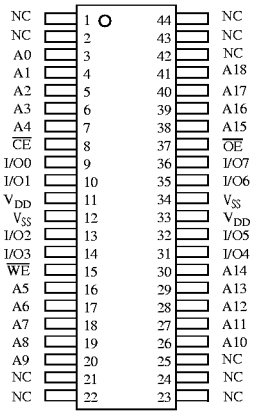
- Organization: 524,288 words × 8 bits
- Intelliwatt™ active power circuitry
- 2.7V to 3.6V operating range
- 25/35/55/70/100 ns address access time
- Low power consumption
  - Active: 126 mW max (100 ns cycle) at 3.6V
  - Standby: 288 µW max
  - Very low DC component in active power, 200 µA
- 1.5V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- Smallest footprint packages
  - 48 ball FBGA
  - 400 mil 44-pin TSOP II
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial temperature range available (-40 to +85 ℃)
- Other voltage versions available
  - 2.3V to 3.0V (AS7C254096LL)
  - 1.65V to 1.95V (AS7C184096LL)

Logic block diagram



Pin arrangement (top view)

TSOP II



48-CSP Ball-Grid-Array Package (shading indicates no ball)

	1	2	3	4	5	6
A	A_0	A_1	NC	A_3	A_6	A_8
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0
C	I/O_5		NC	A_5		I/O_1
D	V_{SS}					V_{DD}
E	V_{DD}					V_{SS}
F	I/O_6		A_{18}	A_{17}		I/O_2
G	I/O_7	$\overline{OE}$	$\overline{CE}$	A_{16}	A_{15}	I/O_3
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

Selection guide

	-25	-35	-55	-70	-100	Unit
Maximum address access time	25	35	55	70	100	ns
Maximum output enable access time	10	10	10	10	10	ns
Maximum operating current	110	80	50	45	35	mA
Maximum CMOS standby current	80	80	80	80	80	µA

Functional description

The AS7C34096LL is a high performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) organized as 524,288 words × 8 bits. It is designed for portable applications where fast data access, long battery life, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 25/35/55/70/100 ns with output enable access times (t_{OE}) of 10 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE}$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is HIGH, the device enters standby mode. The AS7C34096LL is guaranteed not to exceed 288 µW power consumption in standby mode. This device also returns data when V_{DD} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE}$ (Write waveform 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE}$), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

This device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. The 48-ball JEDEC registered package has a ball pitch of 0.75 mm and external dimensions of 8mm × 6mm.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby (I_{SB})
L	H	H	High-Z	Output disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = Low, H = High

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin	V_{tIN}	–0.5	+4.0	V
Voltage on any I/O pin	$V_{tI/O}$	–0.5	V_{DD} + 0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–55	+150	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operating conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{DD}	2.7	3.3	3.6	V
		V_{SS}	0.0	0.0	0.0	V
DC input voltage		V_{IH}	2.0	–	V_{DD} + 0.5	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	℃
	Industrial	T_A	-40	–	85	℃

† V_{IL} min = –3.0V for pulse width less than 10 ns.

DC input/output characteristics

Parameter	Symbol	Test conditions	-25 Min	-25 Max	-35 Min	-35 Max	-55 Min	-55 Max	-70 Min	-70 Max	-100 Min	-100 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	$0V \le V_{in} \le V_{DD}$	–	1	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	Outputs disabled, $0V \le V_{out} \le V_{DD}$	–	1	–	1	–	1	–	1	–	1	µA
Output voltage	V_{OL}	I_{OL} = 4 mA, V_{DD} = Min	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
		I_{OL} = 100 µA, V_{DD} = Min	–	0.1	–	0.1	–	0.1	–	0.1	–	0.1	
	V_{OH}	I_{OH} = - 4 mA, V_{DD} = Min	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V
		I_{OH} = -100 µA, V_{DD} = Min	V_{DD} - 0.1	–	V_{DD} - 0.1	–	V_{DD} - 0.1	–	V_{DD} - 0.1	–	V_{DD} - 0.1	–	

Power consumption characteristics

Condition	Symbol	Test conditions	-25 Min	-25 Max	-35 Min	-35 Max	-55 Min	-55 Max	-70 Min	-70 Max	-100 Min	-100 Max	Unit
Operating, active	I_{DD}	$\overline{CE} \le V_{IL}$, V_{DD} = Max, $f = f_{Max} = 1/t_{RC}$, I_{OUT} = 0 mA	–	110	–	80	–	50	–	45	–	35	mA
Operating, static	I_{DD1}	$\overline{CE} = V_{SS}$, V_{DD} = Max, f = 0, I_{OUT} = 0 mA	–	200	–	200	–	200	–	200	–	200	µA
Standby, address toggling	I_{SB}	$\overline{CE} \ge V_{IH}$, V_{DD} = Max, $f = f_{Max} = 1/t_{RC}$	–	200	–	200	–	200	–	200	–	200	µA
Standby, address static	I_{SB1}	$\overline{CE} \ge V_{DD}$–0.2V, V_{DD} = Max, $V_{in} \le V_{SS}$ + 0.2V or $V_{in} \ge V_{DD}$ - 0.2V, f = 0	–	80	–	80	–	80	–	80	–	80	µA

Capacitance [2]

(f = 1 MHz, T_a = Room temperature, V_{DD} = 3.3V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out}$ = 0V	7	pF

SRAM

Read cycle [3,9]

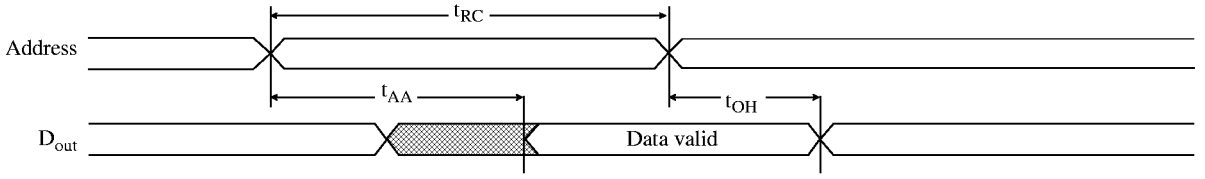
		-25		-35		-55		-70		-100			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	25	–	35	–	55	–	70	–	100	–	ns	
Address access time	t_{AA}	–	25	–	35	–	55	–	70	–	100	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	25	–	35	–	55	–	70	–	100	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	10	–	10	–	10	–	10	–	10	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in Low Z	t_{CLZ}	3	–	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ High to output in High Z	t_{CHZ}	–	10	–	10	–	10	–	10	–	10	ns	4, 5
$\overline{OE}$ Low to output in Low Z	t_{OLZ}	3	–	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{OE}$ High to output in High Z	t_{OHZ}	–	10	–	10	–	10	–	10	–	10	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	25	–	35	–	55	–	70	–	100	ns	4, 5

Key to switching waveforms

Rising input Falling input Undefined output/don't care

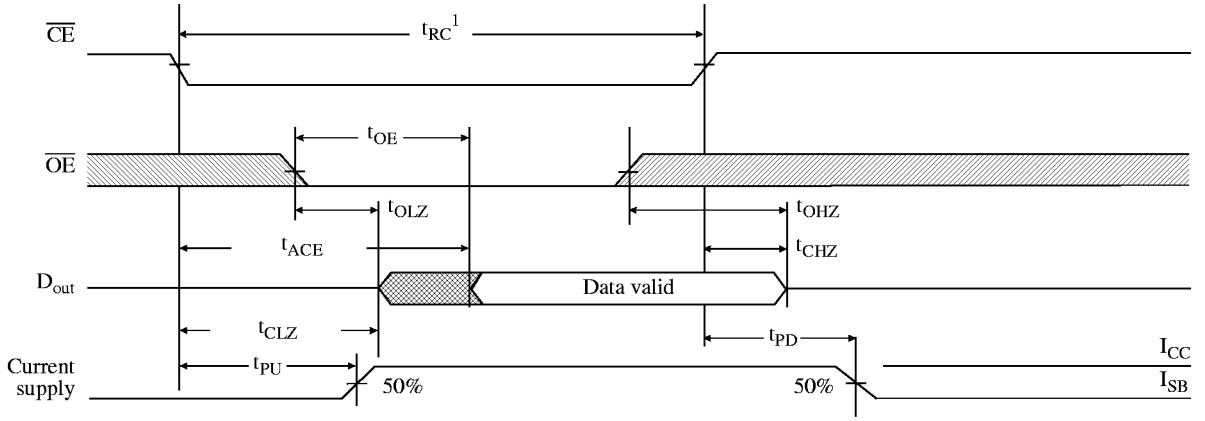
Read waveform 1 [3,6,7,9]

Address controlled



Read waveform 2 [3,6,8,9]

$\overline{CE}$ controlled

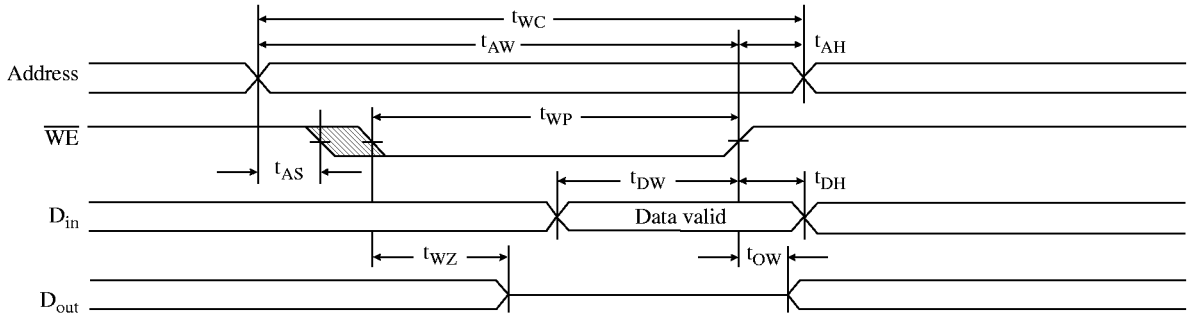


Write cycle

		25		35		55		70		100			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	25	–	35	–	55	–	70	–	100	–	ns	
Chip enable to write end	t_{CW}	15	–	15	–	15	–	15	–	15	–	ns	12
Address setup to write end	t_{AW}	15	–	15	–	15	–	15	–	15	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	15	–	15	–	15	–	15	–	15	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	10	–	10	–	10	–	10	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	5	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	1	–	1	–	ns	4, 5

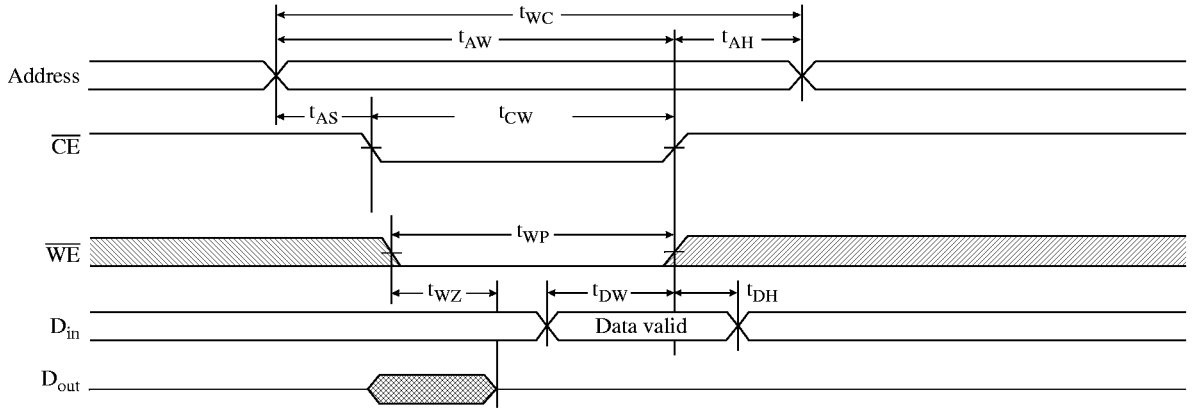
Write waveform 1 *10,11*

$\overline{WE}$ controlled



Write waveform 2 *10,11*

$\overline{CE}$ controlled

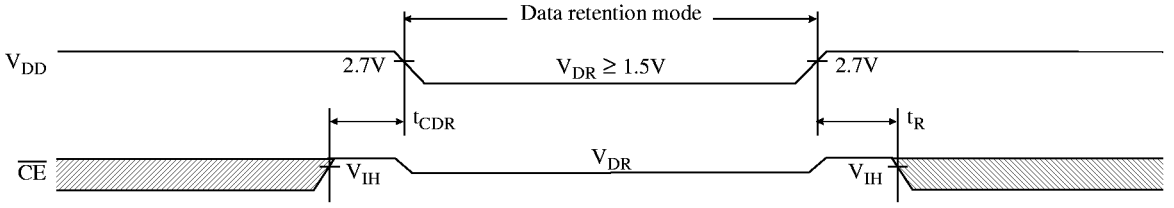


SRAM

Data retention characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit	Notes
V_{DD} for data retention	V_{DR}	V_{DD} = 1.5V	1.5	–	V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{DD}-0.2V$	–	20	µA	5
Chip deselect to data retention time	t_{CDR}	$V_{in} \geq V_{DD}-0.2V$ *or*	0	–	ns	5
Operation recovery time	t_R	$V_{in} \leq 0.2V$	t_{RC}	–	ns	5

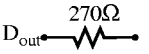
Data retention waveform



AC test conditions

- 3.3V output load: see Figure B, except as noted see Figure C.
- Input pulse level: V_{SS} to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 0.5 × V_{DD}.

Thevenin Equivalent:



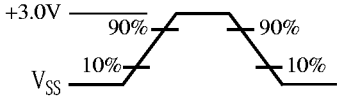


Figure A: Input waveform

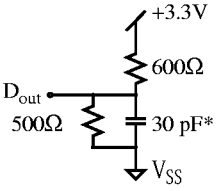
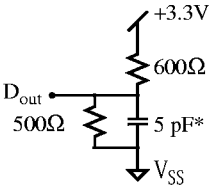


Figure B: Output load



*including scope and jig capacitance

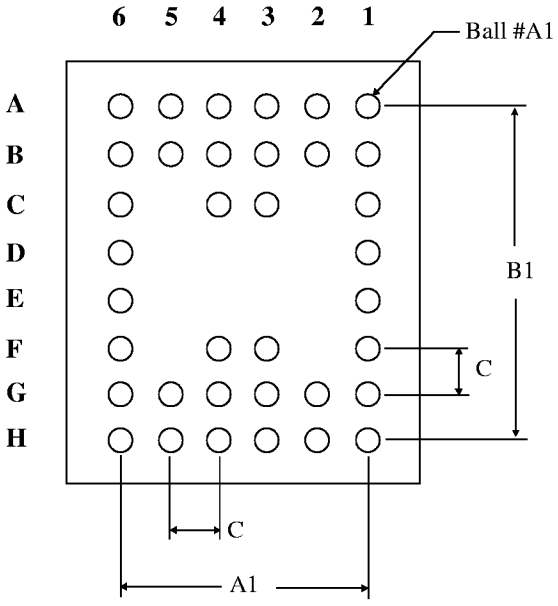
Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Notes

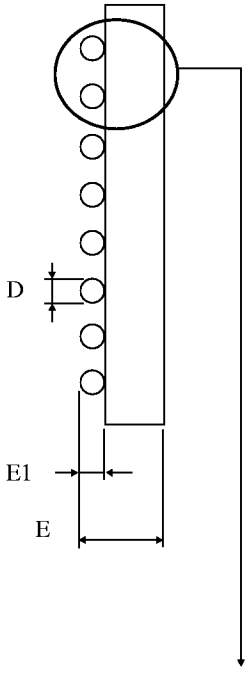
1 During V_{DD} power-up, a pull-up resistor to V_{DD} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see AC Test Conditions, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.

Package dimensions

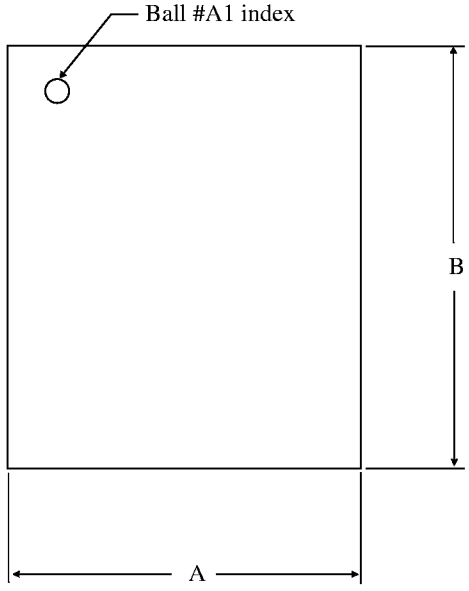
Bottom View



Side View

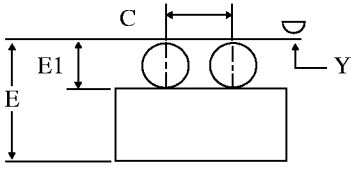


Top View



	Minimum	Typical	Maximum
A	5.90	6.00	6.10
A1	-	3.75	-
B	7.90	8.00	8.10
B1	-	5.25	-
C	-	0.75	-
D	-	0.35	-
E	-	-	1.20
E1	0.17	0.22	0.27
Y	-	0.10	-

Detail View



Notes

1. Units: mm
2. Pitch: (x,y)=0.75 mm × 0.75 mm (typ.)
3. Y is coplanarity: 0.10 mm

AS7C34096LL ordering codes

Package \ Access time	25 ns	35 ns	55 ns	70 ns	100 ns
TSOP 8×20	AS7C34096LL-25TC	AS7C34096LL-35TC	AS7C34096LL-55TC	AS7C34096LL-70TC	AS7C34096LL-100TC
	AS7C34096LL-25TI	AS7C34096LL-35TI	AS7C34096LL-55TI	AS7C34096LL-70TI	AS7C34096LL-100TI
CSP BGA	AS7C34096LL-25BC	AS7C34096LL-35BC	AS7C34096LL-55BC	AS7C34096LL-70BC	AS7C34096LL-100BC
	AS7C34096LL-25BI	AS7C34096LL-35BI	AS7C34096LL-55BI	AS7C34096LL-70BI	AS7C34096LL-100BI

AS7C34096LL part numbering system

AS7C	3	4096	LL	-XX	X	C
SRAM prefix	3=3.3V CMOS 25=2.5V CMOS 18=1.8V CMOS	Device number	Intelliwatt	Access time	Package:T=TSOP II B=CSP BGA	Temperature range, C =Commercial:0 ℃ to 70 ℃ I =Industrial:-40 ℃ to 85 ℃