



# High-Speed CMOS Bus Interface 10-Bit Latch

QS54/74FCT841T  
QS54/74FCT2841T

## FEATURES/BENEFITS

- Pin and function compatible to the Am29841 74FCT841 and 74FCT841T
- Industrial temperature  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- CMOS power levels:  $<7.5\text{mW}$  static
- Available in DIP, SOIC, QSOP, ZIP
- Undershoot Clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

### FCT-T 841T

- JEDEC-FCT spec compatible
- A, B, and C speed grades with 5.5ns  $t_{PD}$  for C
- $I_{OL} = 48\text{mA}$  Ind., 32mA Mil.

### FCT-T 2841T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5ns  $t_{PD}$  for C
- $I_{OL} = 12\text{mA}$  Ind.

## DESCRIPTION

The QSFCT841T is a 10-bit high-speed CMOS TTL-compatible buffered latch with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The device comes in A, B, and C speed grades with 5.5ns (Max.)  $t_{PLH}/t_{PLH}$  for the C grade. The 2841 devices is a  $25\Omega$  resistor output version useful for driving transmission lines and reducing system noise. The 2841 eliminates the need for external series resistor in high speed systems and can replace the 841 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

Figure 1. Functional Block Diagram

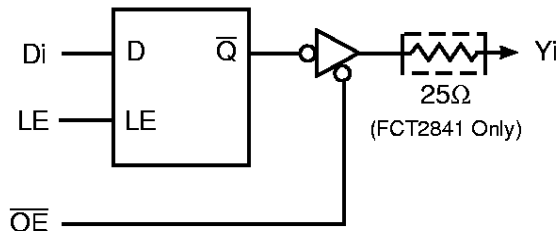


Figure 2. Pin Configurations (All Pins Top View)

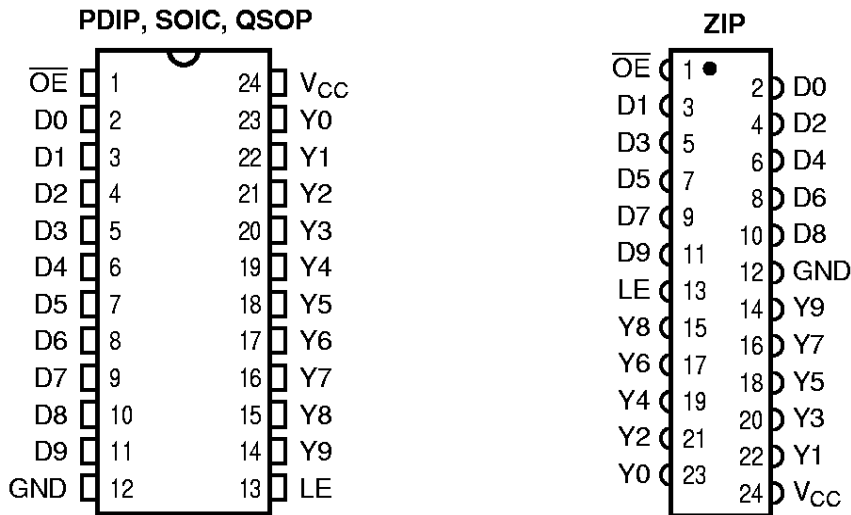


Figure 2. Logic Symbol

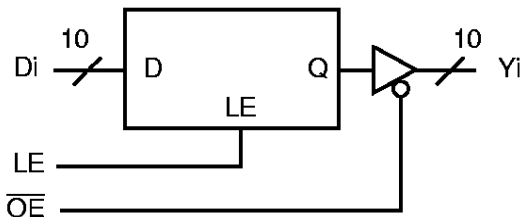


Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

Table 2. Function Tables

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	Di	Qi	Yi	
H	X	X	X	Z	Hi-Z
L	X	X	H	H	Output Enabled
L	X	X	L	L	Output Enabled
X	H	H	H	X	Transparent
X	H	L	L	X	Transparent
X	L	X	NC	X	Latched

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to 7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 4. Capacitance<sup>(1)</sup>**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins <sup>(2)</sup>	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13, 14, 23	4	4	5	7	pF
15-22	6	6	7	9	pF

**Notes:**

1. Capacitance is characterized but not tested.
2. Pin reference for 24-pin package

**Table 5. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , freq = 0 <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

## QS54/74FCT841T, 2841T

**Table 6. DC Electrical Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCT841)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2841 - $25\Omega$ )	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12\text{mA}$ (MIL) $I_{OH} = -15\text{mA}$ (IND)	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCT841)	$V_{CC} = \text{Min.}$ $I_{OL} = 32\text{mA}$ (MIL) $I_{OL} = 48\text{mA}$ (IND)	— —	— —	0.50 0.50	V
$V_{OL}$	Output LOW Voltage (FCT2841 - $25\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2841 - $25\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

## QS54/74FCT841T, 2841T

**Table 7. Switching Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		841A 2841A		841B 2841B		841C 2841C		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL}$	Data to Y Delay	IND	—	9.0	—	6.5	—	5.5	ns
$t_{PLH}$	$\overline{OE} = \text{LOW}$ , 841	MIL	—	10	—	7.5	—	6.3	ns
$t_{PHL}$	Data to Y Delay <sup>(2,3)</sup>	IND	—	13	—	13	—	13	ns
$t_{PLH}$	$\overline{OE} = \text{LOW}$ , 841	MIL	—	15	—	15	—	15	ns
$t_{PHL}$	Data to Y Delay	IND	—	9.5	—	6.5	—	5.5	ns
$t_{PLH}$	$\overline{OE} = \text{LOW}$ , 2841	MIL	—	11	—	7.5	—	6.3	ns
$t_{PHL}$	Data to Y Delay <sup>(2,3)</sup>	IND	—	20	—	13	—	13	ns
$t_{PLH}$	$\overline{OE} = \text{LOW}$ , 2841	MIL	—	20	—	15	—	15	ns
$t_S$	Data to LE Setup	IND	2.5	—	2.5	—	2.5	—	ns
		MIL	2.5	—	2.5	—	2.5	—	ns
$t_H$	Data to LE Hold Time	IND	2.5	—	2.5	—	2.5	—	ns
		MIL	3.0	—	2.5	—	2.5	—	ns
$t_{LEY}$	LE to Y Delay	IND	—	12	—	8.0	—	6.4	ns
	$\overline{OE} = \text{LOW}$ , 841	MIL	—	13	—	10.5	—	6.8	ns
$t_{LEY}$	LE to Y Delay <sup>(2,3)</sup>	IND	—	16	—	15.5	—	15	ns
	$\overline{OE} = \text{LOW}$ , 841	MIL	—	20	—	18	—	16	ns
$t_{LEY}$	LE to Y Delay	IND	—	12	—	8	—	8	ns
	$\overline{OE} = \text{LOW}$ , 2841	MIL	—	13	—	10.5	—	10.5	ns
$t_{LEY}$	LE to Y Delay <sup>(2,3)</sup>	IND	—	16	—	15.5	—	15	ns
	$\overline{OE} = \text{LOW}$ , 2841	MIL	—	20	—	18	—	16	ns

**Notes:**

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3.  $C_{LOAD} = 300\text{pF}$ .

## QS54/74FCT841T, 2841T

**Table 8. Switching Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$       Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$   
 $C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		841A 2841A		841B 2841B		841C 2841C		Unit
			Min	Max	Min	Max	Min	Max	
$t_{LEH}$	LE Pulse Width HIGH <sup>(2)</sup>	IND	6	—	4	—	4	—	ns
		MIL	6	—	4	—	4	—	
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $Y_i$ , 841	IND	—	11.5	—	8	—	6.5	ns
		MIL	—	13	—	8.5	—	8.5	
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(2,3)</sup> $\overline{OE}$ to $Y_i$ , 841	IND	—	23	—	14	—	12	ns
		MIL	—	25	—	15	—	13	
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $Y_i$ , 2841	IND	—	11.5	—	8	—	6.5	ns
		MIL	—	13	—	8.5	—	8.5	
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(2,3)</sup> $\overline{OE}$ to $Y_i$ , 2841	IND	—	23	—	14	—	12	ns
		MIL	—	25	—	15	—	13	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2,4)</sup> $\overline{OE}$ to $Y_i$	IND	—	7	—	6	—	5.7	ns
		MIL	—	9	—	6.5	—	6	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2)</sup> $\overline{OE}$ to $Y_i$	IND	—	8	—	7	—	6	ns
		MIL	—	10	—	7.5	—	6.3	

**Notes:**

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3.  $C_{LOAD} = 300\text{pF}$ .
4.  $C_{LOAD} = 5\text{pF}$ .