# W83194R-81

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## 1.  GENERAL DESCRINPTION

The W83194R-81 is a Clock Synthesizer for SiS chipset.  W83194R-81 provides all clocks required for high-speed RISC or CISC microprocessor such as AMD,Cyrix,Intel Pentium and also provides 16 different frequencies of CPU clocks frequency setting.  All clocks are externally selectable with smooth transitions.  The W83194R-81 makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

The W83194R-81 provides $I^2C$ serial bus interface to program the registers to enable or disable each clock outputs and W83194R-81 provides the 0.25%, 0.5% center type spread spectrum to reduce EMI.

The W83194R-81 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5%  duty cycle.  The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

## 2.   PRODUCT FEATURES

- Supports Pentium™, Pentium™ Pro, AMD and Cyrix CPUs with $I^2C$.
- 3 CPU clocks
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks.
- Optional single or mixed supply:
  (Vdd = Vddq4=Vddq3 = Vddq2b = 3.3V, Vddq2=2.5V) or
  (Vdd = Vddq4=Vddq3 = 3.3V, Vddq2=Vdq2b = 2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center  2.6 ns
- SDRAM frequency synchronous or asynchronous to CPU clocks
- Smooth frequency switch  with selections from 66 to 133mhz(including 90MHz)
- $I^2C$ 2-Wire serial interface and $I^2C$ read back
- 0.25%, 0.5% center type spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal )
- MODE pin for power Management
- 48 MHz for USB
- 24 MHz for super I/O
- 48-pin SSOP package

## 3. BLOCK DIAGRAM
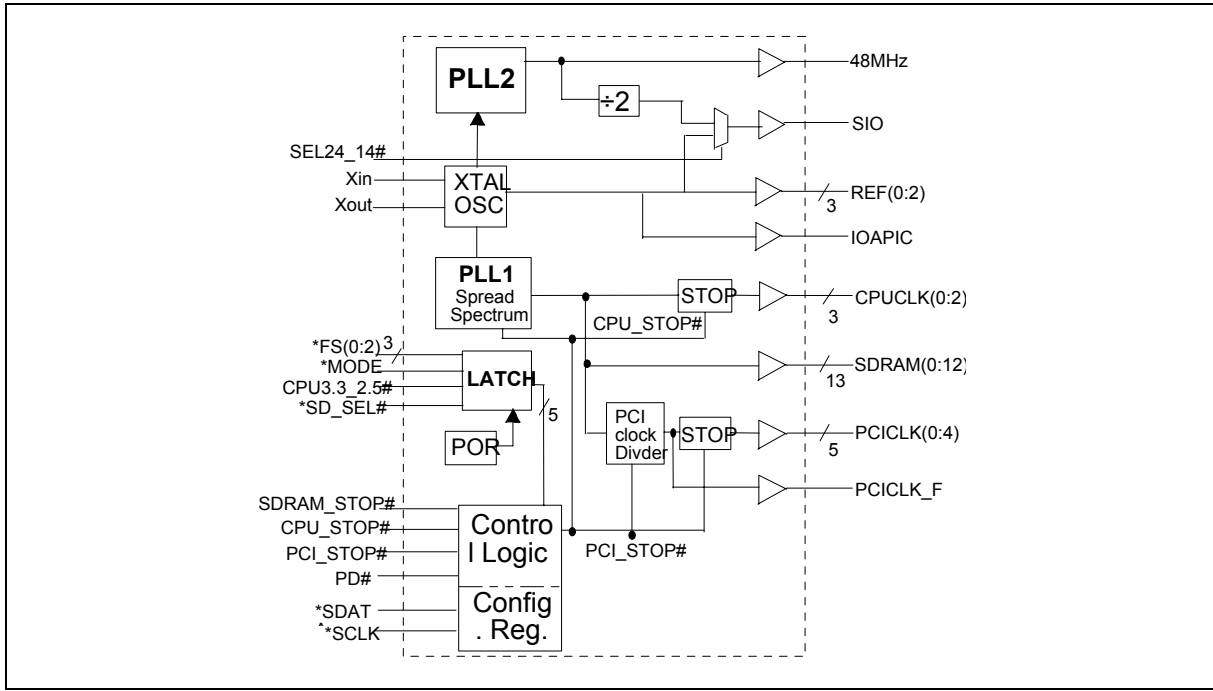


## 4. PIN CONFIGURATION
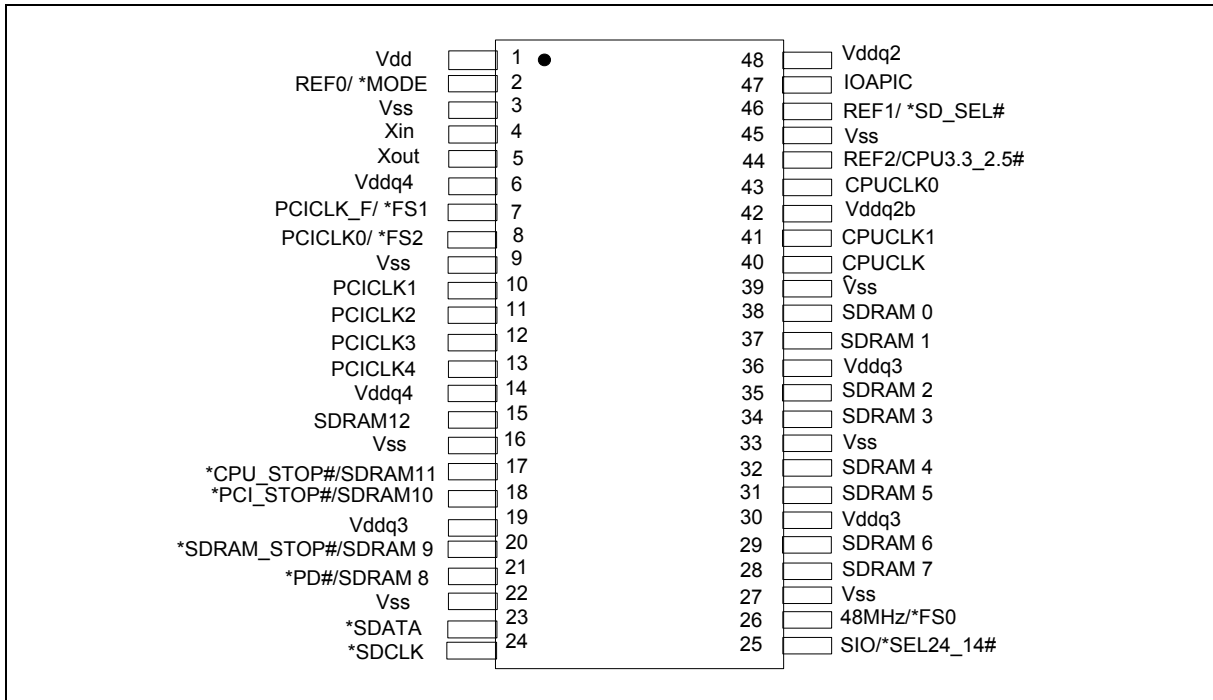
## 5.   PIN DESCRIPTION

IN - Input
OUT - Output
I/O - Bi-directional Pin
# - Active Low
* - Internal 250kΩ pull-up

### 5.1   Crystal I/O

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| Xin | 4 | IN | Crystal input with internal loading capacitors and feedback resistors. |
| Xout | 5 | OUT | Crystal output at 14.318MHz nominally. |

### 5.2   CPU, SDRAM,  PCI Clock Outputs

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| CPUCLK [ 0:2 ] | 40,41,43 | OUT | Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Vddq2b  is the supply voltage for these outputs. |
| SDRAM11/ *CPU_STOP# | 17 | I/O | If MODE =1 (default), then this pin is a SDRAM clock buffered output of the crystal. If MODE = 0 , then this pin is CPU_STOP#  input used in power management mode for synchronously stopping the all CPU clocks. |
| SDRAM10/ *PCI_STOP# | 18 | I/O | If MODE = 1 (default), then this pin is a SDRAM clock output. If MODE = 0 , then this pin is PCI_STOP #  and used in power management mode for synchronously stopping the all PCI clocks. |
| SDRAM9/ *SDRAM_STOP# | 20 | I/O | If MODE = 1 (default), then this pin is a SDRAM clock output. If MODE = 0 , then this pin is SDRAM_STOP #  and used in power management mode for stopping the all SDRAM clocks. |
| SDRAM8/ *PD# | 21 | I/O | If MODE = 1 (default), then this pin is a SDRAM clock output. If MODE = 0 , then this pin is PD # and used to power down the device into a power down state. |
| SDRAM[0:7], SDRAM12 | 28,29,31,32,34, 35,37,38,15 | O | SDRAM clock outputs which have the same frequency as CPU clocks. |
| PCICLK_F/ *FS1 | 7 | I/O | Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Free running PCI clock during normal operation. |

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5.2 CPU, SDRAM, PCI Clock Outputs, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| PCICLK 0 / *FS2 | 8 | I/O | Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.<br>PCI clock during normal operation. |
| PCICLK [ 1:4 ] | 10,11,12,13 | OUT | Low skew (< 250ps) PCI clock outputs. |

## 5.3   I2C Control Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| *SDATA | 23 | I/O | Serial data of I$^2$C 2-wire control interface |
| *SDCLK | 24 | IN | Serial clock of I$^2$C 2-wire control interface |

## 5.4   Fixed Frequency Outputs

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| IOAPIC | 47 | O | 2.5V fixed 14.318MHz |
| REF0 / *MODE | 2 | I/O | 3.3V, 14.318MHz reference clock output.<br>Internal 250kΩ pull-up.<br>Function select pin. |
| REF1 /*SD_SEL# | 46 | I/O | 3.3V, 14.318MHz reference clock output<br>Internal 250kΩ pull-up.<br>Latched input at Power On selects the frequencies for clock outputs. |
| REF2 / CPU3.3#_2.5 | 44 | I/O | Internal 250kΩ pull-up.<br>Latched input for CPU3.3#_2.5 at initial power up. Reference clock during normal operation.<br>Latched high - Vddq2b = 2.5V<br>Latched low   - Vddq2b = 3.3V |
| SIO / *SEL24_14# | 25 | I/O | *SEL24_14# controls the frequency of SIO. If logic 0 at power on, SIO=14.318.  If logic 1, SIO=24MHz for super I/O. |
| 48MHz / *FS0 | 26 | I/O | Internal 250kΩ pull-up.<br>Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.  48MHz output for USB during normal operation. |

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## 5.5  Power Pins

| SYMBOL | PIN | FUNCTION |
|---|---|---|
| Vdd | 1 | Power supply for REF0 crystal and core logic. |
| Vddq2 | 48 | Power supply for REF1,IOAPIC output, 2.5V. |
| Vddq2b | 42 | Power supply for REF2, CPUCLK[0:2], either 2.5V or 3.3V. |
| Vddq3 | 19, 30, 36 | Power supply for SDRAM and 48/24MHz outputs. |
| Vddq4 | 6,14 | Power supply for PCICLK outputs. |
| Vss | 3,9,16,22,27, 33,39,45 | Circuit Ground. |

## 6.  FREQUENCY SELECTION BY HARDWARE

| SD_SEL | FS2 | FS1 | FS0 | CPU (MHZ) | SDRAM (MHZ) | PCI (MHZ) | REF (MHZ) IOAPIC |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 66.70 | 100.05 | 33.35 | 14.318 |
| 0 | 0 | 0 | 1 | 90 | 90 | 30 | 14.318 |
| 0 | 0 | 1 | 0 | 95.25 | 63.4 | 31.7 | 14.318 |
| 0 | 0 | 1 | 1 | 100.2 | 66.8 | 33.4 | 14.318 |
| 0 | 1 | 0 | 0 | 100 | 75 | 30 | 14.318 |
| 0 | 1 | 0 | 1 | 112 | 74.7 | 37.3 | 14.318 |
| 0 | 1 | 1 | 0 | 124 | 82.7 | 31 | 14.318 |
| 0 | 1 | 1 | 1 | 133.3 | 88.9 | 33.3 | 14.318 |
| 1 | 0 | 0 | 0 | 66.8 | 66.8 | 33.4 | 14.318 |
| 1 | 0 | 0 | 1 | 75 | 75 | 30 | 14.318 |
| 1 | 0 | 1 | 0 | 83.3 | 83.3 | 33.32 | 14.318 |
| 1 | 0 | 1 | 1 | 95.25 | 95.25 | 31.7 | 14.318 |
| 1 | 1 | 0 | 0 | 100.2 | 100.2 | 33.4 | 14.318 |
| 1 | 1 | 0 | 1 | 112 | 112 | 37.3 | 14.318 |
| 1 | 1 | 1 | 0 | 124 | 124 | 31 | 14.318 |
| 1 | 1 | 1 | 1 | 133.3 | 133.3 | 33.3 | 14.318 |

## 7. CPU 3.3#_2.5 BUFFER SELECTION

| CPU 3.3#_2.5 ( PIN 44 )  INPUT  LEVEL | CPU OPERATE AT |
| --- | --- |
| 1 | VDD = 2.5V |
| 0 | VDD = 3.3V |

## 8. FUNTION DESCRIPTION

### 8.1 POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface.  On power up, external circuitry should allow 3 ms for the VCO    to stabilize prior to enabling clock outputs to assure correct pulse widths.   When MODE=0, pins 17, 18, 20 and 21 are inputs (PCI_STOP#), (CPU_STOP#), (SDRAM_STOP#), (PD#). when MODE=1, these functions are not available.  A particular  clock could be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enabled.

The W83194R-81 may be disabled in the low state according to the following table in order to reduce power consumption.  All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop.  The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

### Mode pin-power management input

| MODE(PIN2) | PIN17 | PIN18 | PIN20 | PIN21 |
| --- | --- | --- | --- | --- |
| 0 (Input) | CPU_STOP# | PCI_STOP# | SDRAM_STOP# | PD# |
| 1 (Output) | SDRAM11 | SDRAM10 | SDRAM9 | SDRAM8 |

| PD# | CPU_STOP# | PCI_STOP# | SDRAM _STOP# | PCI [0:4] | SDRAM [0:12] | CPU[1:2] | XTAL & VCOS |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | X | X | X | Low | Low | Low | Low |
| 1 | X | X | X | Running | Running | Running | Running |
| 1 | 1 | 1 | 1 | Running | Running | Running | Running |
| 1 | 1 | 1 | 0 | Running | Running | Running | Running |
| 1 | 1 | 0 | 1 | Low | Running | Running | Running |
| 1 | 1 | 0 | 0 | Low | Low | Running | Running |
| 1 | 0 | 1 | 1 | Running | Running | Low | Running |
| 1 | 0 | 1 | 0 | Running | Low | Low | Running |
| 1 | 0 | 0 | 1 | Low | Running | Low | Running |
| 1 | 0 | 0 | 0 | Low | Low | Low | Running |

## 8.2  2-WIRE I2C CONTROL INTERFACE

The clock generator is a  slave I2C component  which can be read back the data stored in the latches for verification.  All proceeding bytes must be sent to change one of the control bytes.  The 2-wire control interface allows each clock output individually enabled or disabled.  On power up, the W83194R-81 initializes with default register settings, and then it   ptional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer.  There are only two exceptions.  One is a high-to-low transition on SDATA while SDCLK is high  used to indicate the beginning of a data transfer cycle.  The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle.  Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address [1101  0010], command code checking [0000  0000], and byte count checking.  After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip.  Controller can start to write to internal $I^2C$ registers after the string of data.  The  sequence order is as follows:

Bytes sequence order for $I^2C$ controller :

| Clock Address A(6:0) & R/W | Ack | 8 bits dummy Command code | Ack | 8 bits dummy Byte count | Ack | Byte0,1,2... until Stop |
|---|---|---|---|---|---|---|

Set R/W to 1 when read back the data sequence is as follows, [1101 0011] :

| Clock Address A(6:0) & R/W | Ack | Byte 0 | Ack | Byte 1 | Ack | Byte2, 3, 4... until Stop |
|---|---|---|---|---|---|---|

## 8.3   SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up.  Registers are set to the values shown only on true power up.  "Command Code" byte and "Byte Count"  byte must be sent following the acknowledge of the Address Byte.  Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge.   After that, the below described sequence (Register 0, Register 1, Register 2, ....) will be valid and acknowledged.

## 8.3.1    Register 0: CPU Frequency Select Register

| BIT | @POWERUP | PIN | DESCRIPTION |
|---|---|---|---|
| 7 | 0 | - | 0 = ±0.25% Spread Spectrum Modulation<br>1 = ±0.5% Spread Spectrum Modulation |
| 6 | 0 | - | SSEL2 ( Frequency table selection by software via I$^2$C) |
| 5 | 0 | - | SSEL1 ( Frequency table selection by software via I$^2$C) |
| 4 | 0 | - | SSEL0 ( Frequency table selection by software via I$^2$C) |
| 3 | 0 | - | 0 = Selection by hardware<br>1 = Selection by software I$^2$C - Bit 6:4 and Bit2 |
| 2 | 0 | - | SSEL3 (Frequency table selection by software via I$^2$C ) |
| 1 | 0 | - | 0 = Normal<br>1 = Spread Spectrum enabled |
| 0 | 0 | - | 0 = Running<br>1 = Tristate all outputs |

**Frequency table selection by software via I2C**

| SSEL3 | SSEL2 | SSEL1 | SSEL0 | CPU (MHZ) | SDRAM (MHZ) | PCI (MHZ) | REF (MHZ) IOAPIC |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 66.70 | 100.05 | 33.35 | 14.318 |
| 0 | 0 | 0 | 1 | 90 | 90 | 30 | 14.318 |
| 0 | 0 | 1 | 0 | 95.25 | 63.4 | 31.7 | 14.318 |
| 0 | 0 | 1 | 1 | 100.2 | 66.8 | 33.4 | 14.318 |
| 0 | 1 | 0 | 0 | 100 | 75 | 30 | 14.318 |
| 0 | 1 | 0 | 1 | 112 | 74.7 | 37.3 | 14.318 |
| 0 | 1 | 1 | 0 | 124 | 82.7 | 31 | 14.318 |
| 0 | 1 | 1 | 1 | 133.3 | 88.9 | 33.3 | 14.318 |
| 1 | 0 | 0 | 0 | 66.8 | 66.8 | 33.4 | 14.318 |
| 1 | 0 | 0 | 1 | 75 | 75 | 30 | 14.318 |
| 1 | 0 | 1 | 0 | 83.3 | 83.3 | 33.32 | 14.318 |
| 1 | 0 | 1 | 1 | 95.25 | 95.25 | 31.7 | 14.318 |
| 1 | 1 | 0 | 0 | 100.2 | 100.2 | 33.4 | 14.318 |
| 1 | 1 | 0 | 1 | 112 | 112 | 37.3 | 14.318 |
| 1 | 1 | 1 | 0 | 124 | 124 | 31 | 14.318 |
| 1 | 1 | 1 | 1 | 133.3 | 133.3 | 33.3 | 14.318 |

### 8.3.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

| BIT | @POWERUP | PIN | DESCRIPTION |
| --- | --- | --- | --- |
| 7 | 1 | - | Reserved |
| 6 | 1 | - | Reserved |
| 5 | 1 | - | Reserved |
| 4 | 1 | - | Reserved |
| 3 | 1 | 40 | CPUCLK2 (Active / Inactive) |
| 2 | 1 | 41 | CPUCLK1 (Active / Inactive) |
| 1 | 1 | 43 | CPUCLK0 (Active / Inactive) |
| 0 | - | - | Latched FS0# |

### 8.3.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

| BIT | @POWERUP | PIN | DESCRIPTION |
| --- | --- | --- | --- |
| 7 | - | - | Latched FS1# |
| 6 | 1 | 7 | PCICLK_F (Active / Inactive) |
| 5 | 1 | - | Reserved |
| 4 | 1 | 13 | PCICLK4 (Active / Inactive) |
| 3 | 1 | 12 | PCICLK3 (Active / Inactive) |
| 2 | 1 | 11 | PCICLK2 (Active / Inactive) |
| 1 | 1 | 10 | PCICLK1 (Active / Inactive) |
| 0 | 1 | 8 | PCICLK0 (Active / Inactive) |

### 8.3.4 Register 3: SDRAM Clock Register (1 = Active, 0 = Inactive)

| BIT | @POWERUP | PIN | DESCRIPTION |
| --- | --- | --- | --- |
| 7 | 1 | 28 | SDRAM7 (Active / Inactive) |
| 6 | 1 | 29 | SDRAM6 (Active / Inactive) |
| 5 | 1 | 31 | SDRAM5 (Active / Inactive) |
| 4 | 1 | 32 | SDRAM4 (Active / Inactive) |
| 3 | 1 | 34 | SDRAM3 (Active / Inactive) |
| 2 | 1 | 35 | SDRAM2 (Active / Inactive) |
| 1 | 1 | 37 | SDRAM1 (Active / Inactive) |
| 0 | 1 | 38 | SDRAM0 (Active / Inactive) |

### 8.3.5  Register 4: Additional SDRAM Clock Register (1 = Active, 0 = Inactive)

| BIT | @POWERUP | PIN | DESCRIPTION |
|---|---|---|---|
| 7 | 1 | - | Reserved |
| 6 | 1 | 25 | 24/14MHz(Active / Inactive) |
| 5 | 1 | 26 | 48MHz(Active / Inactive) |
| 4 | 1 | 15 | SDRAM12 (Active / Inactive) |
| 3 | 1 | 17 | SDRAM11 (Active / Inactive) |
| 2 | 1 | 18 | SDRAM10 (Active / Inactive) |
| 1 | 1 | 20 | SDRAM9   (Active / Inactive) |
| 0 | 1 | 21 | SDRAM8   (Active / Inactive) |

### 8.3.6  Register 5: Peripheral Control (1 = Active, 0 = Inactive)

| BIT | @POWERUP | PIN | DESCRIPTION |
|---|---|---|---|
| 7 | 1 | - | Reserved |
| 6 | - | - | Latched FS2# |
| 5 | 1 | - | Reserved |
| 4 | 1 | 47 | IOAPIC (Active / Inactive) |
| 3 | - | - | Latched SD_SEL |
| 2 | 1 | 44 | REF2 (Active / Inactive) |
| 1 | 1 | 46 | REF1 (Active / Inactive) |
| 0 | 1 | 2 | REF0 (Active / Inactive) |

### 8.3.7  Register 6:  Winbond Chip ID Register  (Read Only)

| BIT | @POWERUP | PIN | DESCRIPTION |
|---|---|---|---|
| 7 | 0 | - | Winbond Chip ID |
| 6 | 1 | - | Winbond Chip ID |
| 5 | 0 | - | Winbond Chip ID |
| 4 | 1 | - | Winbond Chip ID |
| 3 | 0 | - | Winbond Chip ID |
| 2 | 1 | - | Winbond Chip ID |
| 1 | 0 | - | Winbond Chip ID |
| 0 | 0 | - | Winbond Chip ID |

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## 9. SPECIFICATIONS

### 9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

| SYMBOL | PARAMETER | RATING |
|---|---|---|
| Vdd , $V_{IN}$ | Voltage on any pin with respect to GND | - 0.5 V to + 7.0 V |
| $T_{STG}$ | Storage Temperature | - 65°C to + 150°C |
| $T_B$ | Ambient Temperature | - 55°C to + 125°C |
| $T_A$ | Operating Temperature | 0°C to + 70°C |

### 9.2 AC CHARACTERISTICS

| Vddq4 = Vdd = Vddq3 = 3.3V ± 5 %, Vddq2=Vddq2b = 2.375V~2.9V , $T_A$ = 0°C to +70°C | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
| Output Duty Cycle | | 45 | 50 | 55 | % | Measured at 1.5V |
| CPU/SDRAM to PCI Offset | $t_{OFF}$ | 1 | | 4 | ns | 15 pF Load Measured at 1.5V |
| Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM) | $t_{SKEW}$ | | | 250 | ps | 15 pF Load Measured at 1.5V |
| CPU/SDRAM Cycle to Cycle Jitter | $t_{CCJ}$ | | | ±250 | ps | |
| CPU/SDRAM Absolute Jitter | $t_{JA}$ | | | 500 | ps | |
| Jitter Spectrum 20 dB Bandwidth from Center | $BW_J$ | | | 500 | KHz | |
| Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time | $t_{TLH}$ $t_{THL}$ | 0.4 | | 1.6 | ns | 15 pF Load on CPU and PCI outputs |
| Overshoot/Undershoot Beyond Power Rails | $V_{over}$ | | | 1.5 | V | 22 Ω at source of 8 inch PCB run to 15 pF load |
| Ring Back Exclusion | $V_{RBE}$ | | | 2.1 | V | Ring Back must not enter this range. |

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## 9.3 DC CHARACTERISTICS

| *Vddq4 = Vdd = Vddq3 = 3.3V ± 5 %, Vddq2=Vddq2b = 2.375V~2.9V , $T_A$ = 0°C to +70°C* | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | $V_{dc}$ | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | $V_{dc}$ | |
| Input Low Current | $I_{IL}$ | | | -66 | μA | |
| Input High Current | $I_{IH}$ | | | 5 | μA | |
| Output Low Voltage $I_{OL}$ = 4 mA | $V_{OL}$ | | | 0.4 | $V_{dc}$ | All outputs |
| Output High Voltage $I_{OH}$ = 4mA | $V_{OH}$ | 2.4 | | | $V_{dc}$ | All outputs using 3.3V power |
| Tri-State leakage Current | Ioz | | | 10 | μA | |
| Dynamic Supply Current for Vdd + Vddq3 | $I_{dd3}$ | | | | mA | CPU = 66.6 MHz PCI = 33.3 Mhz with load |
| Dynamic Supply Current for Vddq2 + Vddq2b | $I_{dd2}$ | | | | mA | Same as above |
| CPU Stop Current for Vdd + Vddq3 | $I_{CPUS3}$ | | | | mA | Same as above |
| CPU Stop Current for Vddq2 + Vddq2b | $I_{CPUS2}$ | | | | mA | Same as above |
| PCI Stop Current for Vdd + Vddq3 | $I_{PD3}$ | | | | mA | |

### 9.4 BUFFER CHARACTERISTICS

#### 9.4.1 TYPE 1 BUFFER FOR CPU (0:2)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $I_{OH(min)}$ | -27 | | | mA | Vout = 1.0 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -27 | mA | Vout = 2.0V |
| Pull-Down Current Min | $I_{OL(min)}$ | | | | mA | Vout = 1.2 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 27 | mA | Vout = 0.3 V |
| Rise/Fall Time Min Between 0.4 V and 2.0 V | $T_{RF(min)}$ | 0.4 | | | ns | 10 pF Load |
| Rise/Fall Time Max Between 0.4 V and 2.0 V | $T_{RF(max)}$ | | | 1.6 | ns | 20 pF Load |

#### 9.4.2 TYPE 2 BUFFER FOR IOAPIC

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $I_{OH(min)}$ | | | | mA | Vout = 1.4 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -29 | mA | Vout = 2.7V |
| Pull-Down Current Min | $I_{OL(min)}$ | | | | mA | Vout = 1.0 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 28 | mA | Vout = 0.2 V |
| Rise/Fall Time Min Between 0.7 V and 1.7 V | $T_{RF(min)}$ | 0.4 | | | ns | 10 pF Load |
| Rise/Fall Time Max Between 0.7 V and 1.7 V | $T_{RF(max)}$ | | | 1.8 | ns | 20 pF Load |

### 9.4.3 TYPE 3 BUFFER FOR REF(0:2), 24MHZ, 48MHZ

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $I_{OH(min)}$ | -29 | | | mA | Vout = 1.0 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -23 | mA | Vout = 3.135V |
| Pull-Down Current Min | $I_{OL(min)}$ | 29 | | | mA | Vout = 1.95 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | | mA | Vout = 0.4 V |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 1.0 | | | ns | 10 pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 4.0 | ns | 20 pF Load |

### 9.4.4 TYPE 4 BUFFER FOR SDRAM(0:12)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $I_{OH(min)}$ | | | | mA | Vout = 1.65V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -46 | mA | Vout = 3.135V |
| Pull-Down Current Min | $I_{OL(min)}$ | | | | mA | Vout = 1.65 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 53 | mA | Vout = 0.4 V |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 0.5 | | | ns | 20 pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 1.3 | ns | 30 pF Load |

### 9.4.5 TYPE 5 BUFFER FOR PCICLK(0:4, F)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $I_{OH(min)}$ | -33 | | | mA | Vout = 1.0 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -33 | mA | Vout = 3.135 V |
| Pull-Down Current Min | $I_{OL(min)}$ | 30 | | | mA | Vout = 1.95 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 38 | mA | Vout = 0.4 V |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 0.5 | | | ns | 15 pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 2.0 | ns | 30 pF Load |

## 10. POWER MANAGEMENT TIMING

### 10.1 CPU_STOP# Timing Diagram
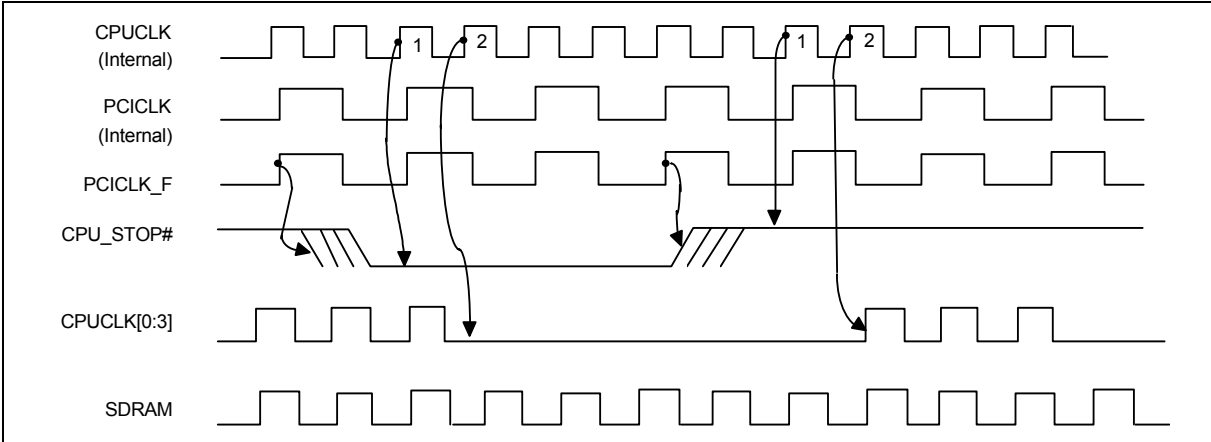


For synchronous Chipset, CPU_STOP# pin is a synchronous "active low "input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU locks on latency" is less than 2 CPU clocks and locks off latency is less then 2 CPU clocks.

### 10.2 PCI_STOP# Timing Diagram
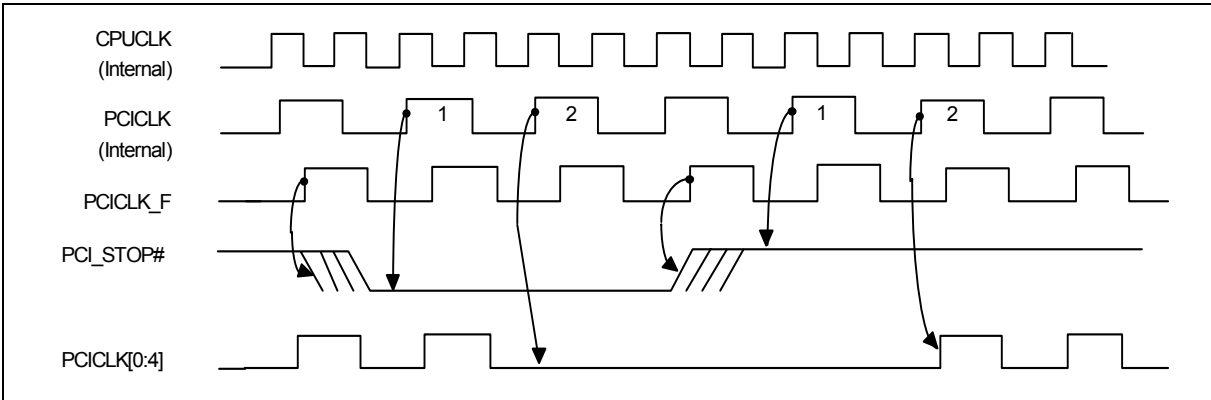


For synchronous Chipset, PCI_STOP# pin is a synchronous ctive low" input pin used to stop the PCICLK [0:4] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI locks on latency" is less than 1 PCI clocks and locks off latency is less then 1 PCI clocks.

## 11. ORDERING INFORMATION

| Part Number | Package Type | Production Flow |
|---|---|---|
| W83194R-81 | 48 PIN SSOP | Commercial, 0°C to +70°C |

## 12. HOW TO READ THE TOP MARKING

```
W83194R-81
28051234
814GBB
```
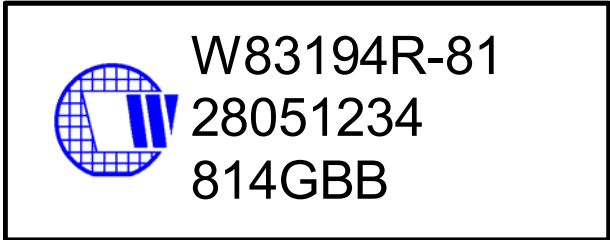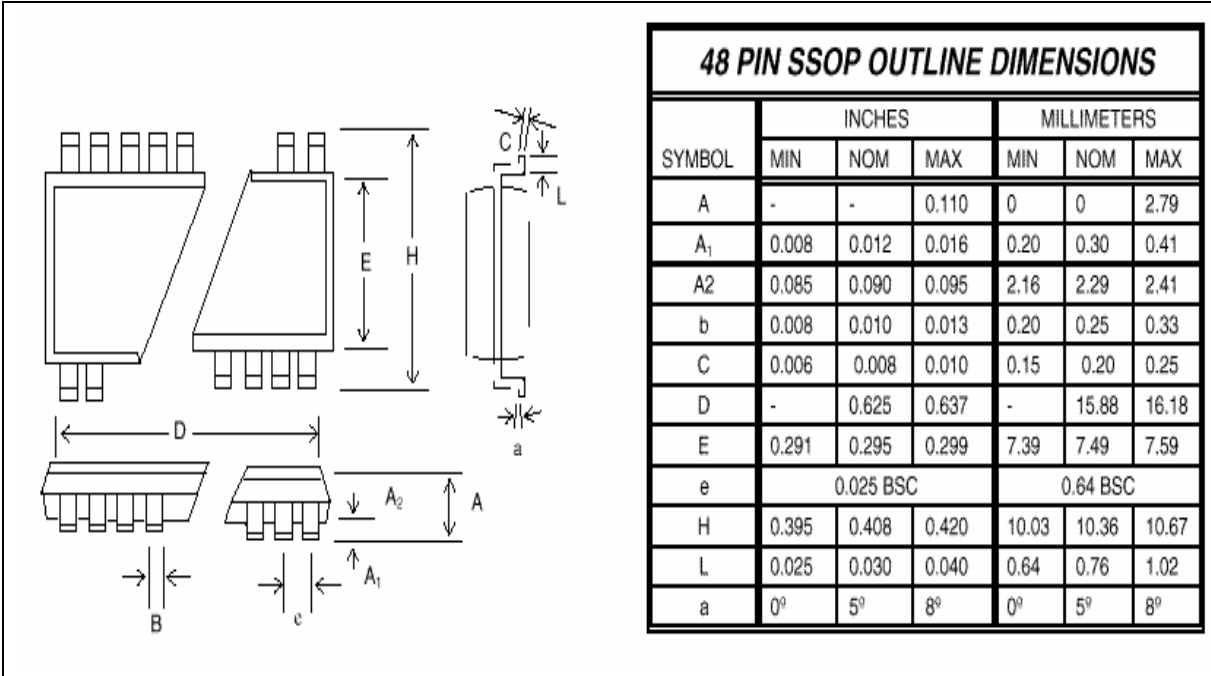
   1st line: Winbond logo and the type number: W83194R-81

   2nd line: Tracking code 2 8051234

             **2**: wafers manufactured in Winbond FAB 2

      **8051234**: wafer production series lot number

   3rd line: Tracking code   814 G B B

       **814**: packages made in '98, week 14

       **G**: assembly house ID; A means ASE, S means SPIL, G means GR

     **BB**: IC revision

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## 13. PACKAGE DRAWING AND DIMENSIONS

| 48 PIN SSOP OUTLINE DIMENSIONS | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOL | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | - | - | 0.110 | 0 | 0 | 2.79 |
| $A_1$ | 0.008 | 0.012 | 0.016 | 0.20 | 0.30 | 0.41 |
| A2 | 0.085 | 0.090 | 0.095 | 2.16 | 2.29 | 2.41 |
| b | 0.008 | 0.010 | 0.013 | 0.20 | 0.25 | 0.33 |
| C | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| D | - | 0.625 | 0.637 | - | 15.88 | 16.18 |
| E | 0.291 | 0.295 | 0.299 | 7.39 | 7.49 | 7.59 |
| e | 0.025 BSC | | | 0.64 BSC | | |
| H | 0.395 | 0.408 | 0.420 | 10.03 | 10.36 | 10.67 |
| L | 0.025 | 0.030 | 0.040 | 0.64 | 0.76 | 1.02 |
| a | $0^o$ | $5^o$ | $8^o$ | $0^o$ | $5^o$ | $8^o$ |

## 14. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|------|------|-------------|
| A1 | May 17, 2005 | 18 | ADD Important Notice |

## Important Notice

**Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.**

**Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.**

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