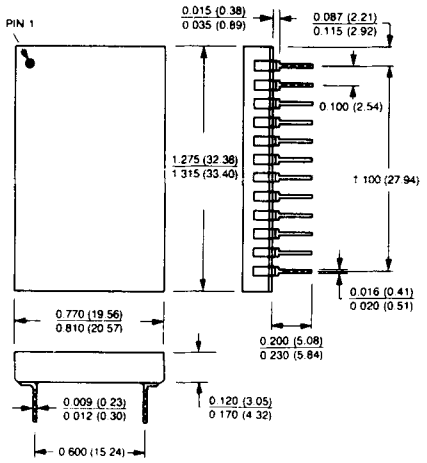
12-bit D/A Converter with Input Register

FEATURES

- Complete With Internal:
  Input Register
  Output Op Amp
  Low-Drift Reference
- ±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature
- 40nsec Data Setup Time
- ±0.1% FSR Unadjusted Absolute Accuracy
- 7μsec Max Settling Time (20V step to ±1/2LSB)
- Small 24-Pin Side-Brazed DIP
- Full MIL Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN3860 is a 12-bit digital-to-analog converter with a fast, internal, TTL input register. It is packaged in a hermetically sealed, ceramic, 24-pin dual-in-line package and is complete with internal reference and output amplifier. Three user selectable output ranges are available (0 to +10V, ±5V and ±10V), and performance features include the following: fast output settling (7μsec for a 20V change), ±0.1%FSR maximum absolute accuracy, and ±½LSB linearity and monotonicity guaranteed over the full operating temperature range. Maximum power consumption is 730mW.

The MN3860 is functionally laser trimmed for linearity, gain and offset, eliminating the need for external potentiometers. Units are available for two operating temperature ranges (0°C to +70°C and −55°C to +125°C). Linearity and accuracy are tested 100% and guaranteed both at room and temperature extremes. For military/aerospace or harsh-environment commercial/industrial application, "H/B CH" models are fully screened to MIL-PRF-38534.

The MN3860 is TTL compatible, and its internal input register facilitates interfacing to microprocessor and minicomputer data buses. Applications include microprocessor-based data-distribution systems, programmable power supplies and servo drivers.

Model Number	Temperature Range	Input Coding	Max.Power Consumption
MN3860	0°C to +70°C	CSB/COB	730mW
MN3860H	−55°C to +125°C	CSB/COB	730mW
MN3860H/B	−55°C to +125°C	CSB/COB	730mW
MN3860H/BCH	−55°C to +125°C	CSB/COB	730mW

MN3860 12-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN3860	0°C to +70°C
MN3860H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 22)	0 to +18 Volts
Negative Supply (−Vcc, Pin 14)	0 to −18 Volts
Logic Supply (+Vdd, Pin 13)	−0.5 to +7 Volts
Register Enable (Pin 19)	−0.5 to +5.5 Volts
Digital Inputs (Pins 1-12)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER——— MN3860H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-PRF-38534.

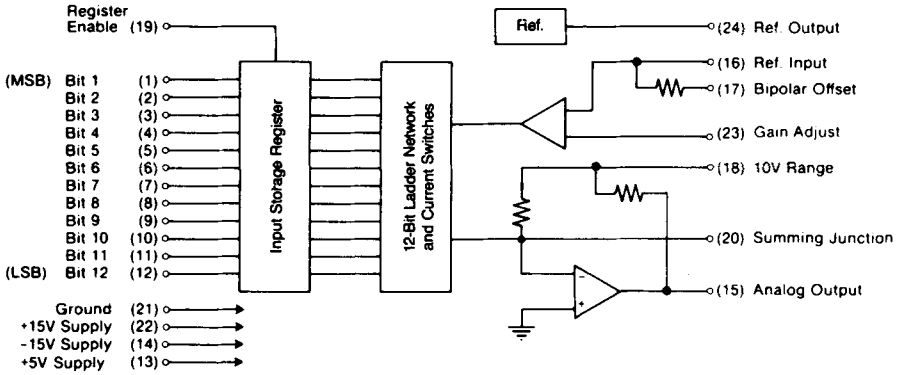
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V +Vdd = +5V unless otherwise indicated) (Note 1)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.7	Volts
Input Currents: Data Inputs: Logic "1" (V_{IH} = +2.4V)			+30	µA
Logic "0" (V_{IL} = +0.4V)			−0.6	mA
Register Enable: Logic "1" (V_{IH} = +2.4V)			+60	µA
Logic "0" (V_{IL} = +0.4V)			−1.2	mA
Register Enable (Note 2): Pulse Width	60			nsec
Setup Time Digital Data to Enable	40			nsec
Logic Coding: Unipolar Range	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar		0 to +10		Volts
Bipolar		±5, ±10		Volts
Output Impedance		0.5		Ω
Output Current	±4	±5		mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 8)			±½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 4, 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 8)		±0.15	±0.3	%FSR
Zero Error (Notes 4, 6): Initial (+25°C)		±0.025	±0.05	%FSR
Over Temperature (Note 8)		±0.05	±0.1	%FSR
Gain Error (Notes 4, 7)		±0.1		%
Gain Drift		±10		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ±0.01% for 20V Step		5	7	µsec
Output Slew Rate		±20		V/µsec
REFERENCE OUTPUT				
Internal Reference: Voltage		+6.3		Volts
Accuracy		±2		%
Tempco		±10		ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
+5V Supply	+4.75	+5.00	+5.25	Volts
Power Supply Rejection: +15V Supply		±0.01	±0.04	%FSR/%Supply
−15V Supply		±0.001	±0.004	%FSR/%Supply
Current Drain: +15V Supply		+8	+12	mA
−15V Supply		−15	−20	mA
+5V Supply		+30	+50	mA
Power Consumption		495	730	mW

SPECIFICATIONS

1. Unless otherwise indicated, listed specifications apply for all MN3860 models.
2. The analog output will follow its digital input when Register Enable is a logic "0". Digital input data will be latched and analog output voltage constant when Register Enable is logic "1". The minimum Register Enable pulse width to latch new digital input data is 60nsec. See Timing Diagram.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ±10V output range, FSR is 20 Volts, and 1LSB is ideally equal to 4.88mV. For the 0 to +10V and ±5V ranges, FSR is 10 Volts, and 1LSB is ideally equal to 2.44mV.
4. Initial zero and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Full Scale Absolute Accuracy Error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. For unipolar output ranges, Full Scale Absolute Accuracy Error refers to the deviation between the actual and the ideal output with an all "0's" digital input applied. For bipolar output ranges, the spec. refers to the deviation between the actual and the ideal output with either all "0's" (positive full scale) or all "1's" (negative full scale) applied.
6. Zero error is defined as the difference between the actual and the ideal output voltage for the input code which ideally produces 0 Volts out. For the 0 to +10V range, zero error is measured with a digital input of 11111 1111 1111. For ±5V and ±10V ranges, zero error is measured with a digital input of 0111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output span from the 1111 1111 1111 output to the 0000 0000 0000 output.
8. Listed specifications apply over the 0°C to +70°C temperature range for standard products, and over the −55°C to +125°C range for "H" products.

BLOCK DIAGRAM



PIN DESIGNATIONS

1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	Register Enable
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. In
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply
12	Bit 12 (LSB)	13	+5V Supply

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN3860. The units' Ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used.

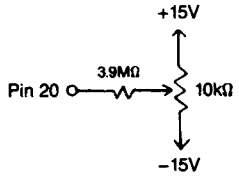
Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16) and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

REFERENCE OUTPUT—The MN3860 contains an internal +6.3V ±2% voltage reference, and the units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 2.5mA.

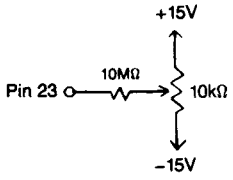
OPTIONAL GAIN AND OFFSET ADJUSTMENTS—The MN3860 will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced to ±1LSB by following the trimming procedure described below. Adjustments should be made following warmup and, to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be grounded.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for the unipolar output ranges or minus full scale for bipolar output ranges.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Coding table.



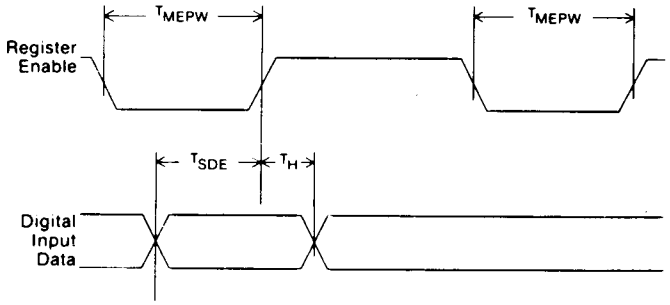
OFFSET ADJUST



GAIN ADJUST

REGISTER ENABLE—When the Register Enable (pin 19) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nsec and digital input data must be valid for a minimum of 40nsec prior to Register Enable going high again. See Timing Diagram.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW} Minimum Enable Pulse Width is 60nsec.
T_{SDE} Minimum Setup Time Digital Data to Enable is 40nsec.
T_H Digital Data Hold Time from Register Enable is 0nsec.

OUTPUT RANGE SELECTION

Pin Connections	Analog Output		
Output Range	**0 to +10V**	**±5V**	**±10V**
Connect Pin 24 to	16	16	16
Connect Pin 17 to Connect Pin 15 to	21 18	20 18	20 N.C.
Connect Pin 20 to	N.C.	17	17

INPUT LOGIC CODING

Digital Input		Analog Output		
MSB	**LSB**	**0 to +10V**	**±5V**	**±10V**
0000 0000 0000		+9.9976V	+4.9976V	+9.9951V
0000 0000 0001		+9.9951V	+4.9951V	+9.9902V
0111 1111 1111		+5.0000V	0.0000V	0.0000V
1000 0000 0000		+4.9976V	−0.0024V	−0.0049V
1111 1111 1110		+0.0024V	−4.9976V	−9.9951V
1111 1111 1111		0.0000V	−5.0000V	−10.0000V

CODING NOTES:

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR=20V, 1LSB=4.88mV.
4. For FSR=10V, 1LSB≈2.44mV.

MICROPROCESSOR INTERFACING

Interfacing the MN3860 to 8, 12 and 16-bit microprocessors is simplified by the MN3860's internal 12-bit register. External address and control decoding will be required, however.

Interfacing to 12 and 10-bit processors is fairly direct and can usually be accomplished by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line and using the output to drive the MN3860's Register Enable input. For most processors, valid data remains on the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the MN3860 immediately after one of the address or control signals changes but before valid data goes away.

Interfacing to 8-bit processors is slightly more complicated and an 8-bit external register is needed as shown in the sketch below.

Address decoding must be organized such that the 8-bit intermediate register and the MN3860's internal 12-bit register appear at two different addresses. The 12 bits of digital data are sent to the MN3860 via two data transfers. First, the 8 least significant bits of digital data are written to the intermediate latch. Then, the 4 most significant bits of digital data are written to the MN3860's 12-bit latch. The result is that the 4 MSB's on the data bus and the 8 LSB's held in the intermediate latch are all latched into the MN3860's latch simultaneously. This technique is called double buffering and it avoids the analog output slewing to an undesirable state determined by the LSB's of the new digital data and the MSB's of the previous digital data.