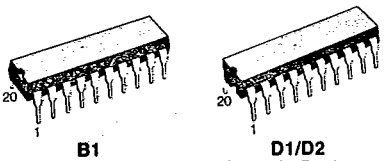
LOW POWER SCHOTTKY INTEGRATED CIRCUITS

T54LS373
T74LS373

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

DESCRIPTION

The T54LS373/T74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asyncronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus outputs is in the high impedance state.



B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

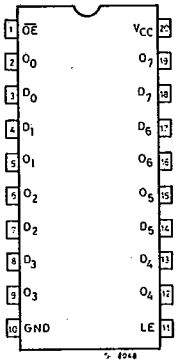
ORDERING NUMBERS:

T54LS373 D2
T74LS373 D1
T74LS373 B1
T74LS373 C1
T74LS373 M1

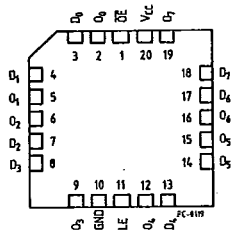
- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING
- HYSTERESIS ON LATCH ENABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



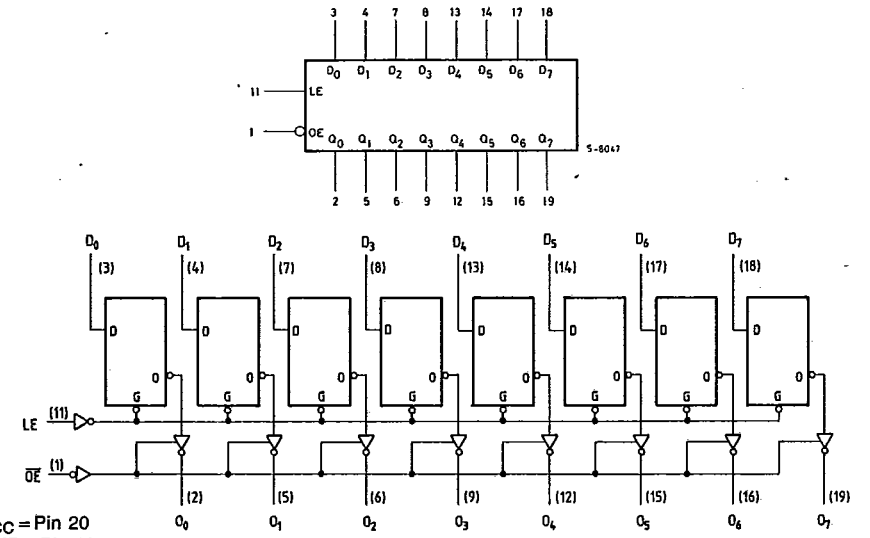
NC = No Internal Connection

PIN NAMES

D_0-D_7	Data Inputs
LE	Latch Enable (Active HIGH) Input
$\overline{OE}$	Output Enable (Active LOW) Input
O_0-O_7	Outputs

T54LS373
T74LS373

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS373D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS373XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		I_{OH} = 0.1mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per truth table	V
		74	2.4	3.1		I_{OL} = 2.6mA		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per truth table	V
		74		0.35	0.5	I_{OL} = 24mA		
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.4V, V_E = 2.0V		μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V, V_E = 2.0V		μA
I_{IH}	Input HIGH Current				20	V_{CC} = MAX, V_{IN} = 2.7V		μA
	Input HIGH Current at MAX Input Voltage				0.1	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−30		−130	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current Outputs Off			24	40	V_{CC} = MAX, V_{IN} = 0V, V_E = 4.5V		mA

AC CHARACTERISTICS: (T_A = 25°C)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions		Units
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18	Fig. 1	C_L = 15pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock or LE to Output		20 18	30 30	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		15	28	Figs. 3,4	C_L = 15pF R_L = 2 kΩ	ns
t_{PZL}	Output Enable Time to LOW Level		25	36	Figs. 2,4		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	Figs. 2,4	C_L = 5pF R_L = 2 kΩ	ns
t_{PHZ}	Output Disable Time from HIGH Level		12	20	Figs. 3,4		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "wrost case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

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AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_sD	Set-up Time Data to Negative Going LE	20	11		Fig. 1	$V_{CC} = 5.0V$	ns
t_hD	Hold Time Data to Negative Going LE	20	11				ns
t_WLE	Minimum LE Pulse Width HIGH to LOW	15	10				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input to LE transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following LE transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.

AC WAVEFORMS

Fig. 1

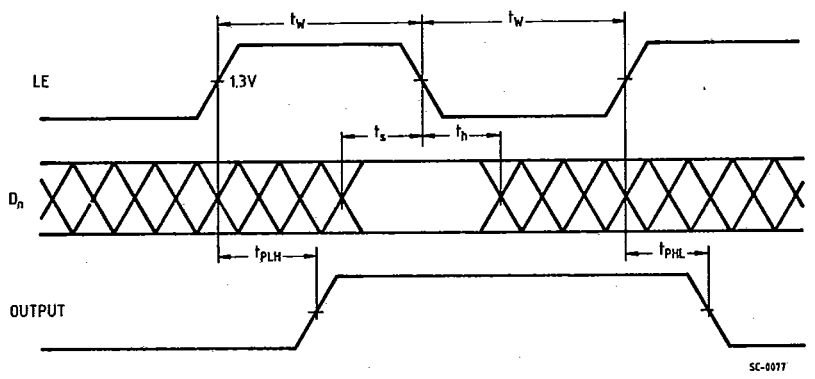


Fig. 2

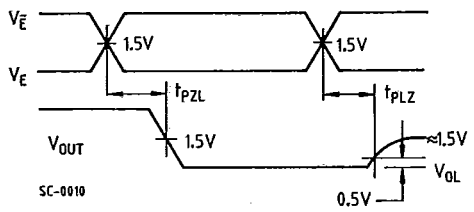
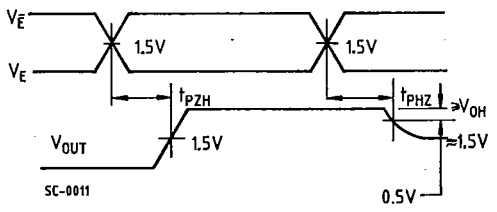


Fig. 3



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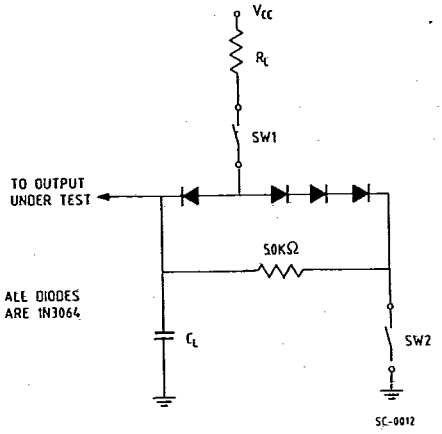
AC LOAD CIRCUIT

Fig. 4

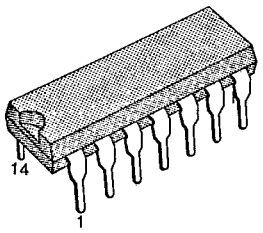


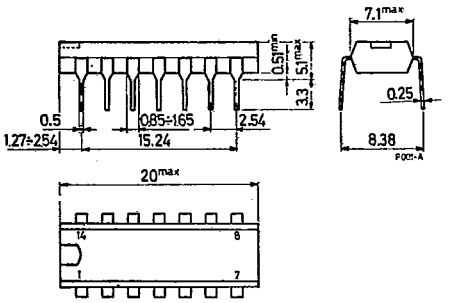
SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

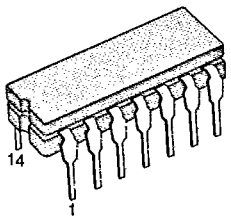
Packages

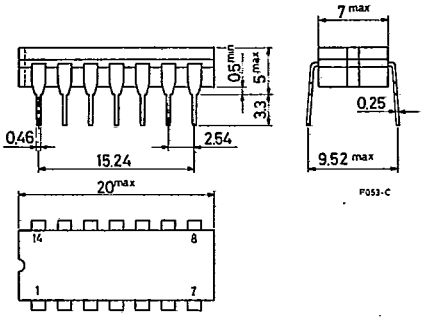
14-LEAD PLASTIC DIP



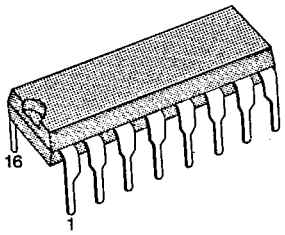


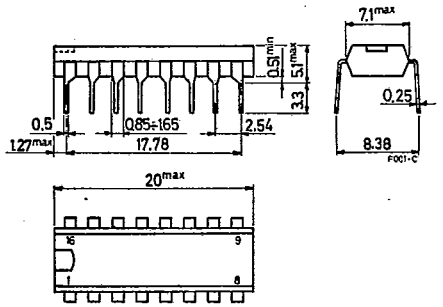
14-LEAD CERAMIC DIP





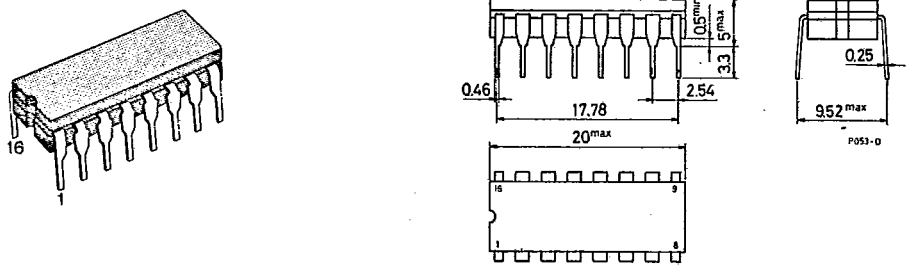
16-LEAD PLASTIC DIP



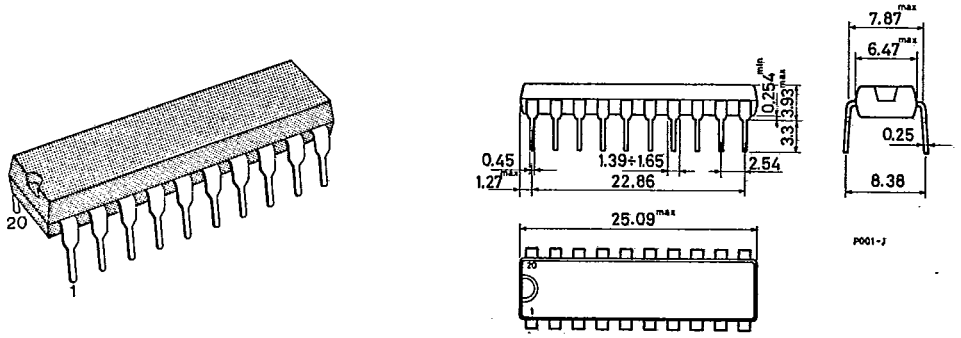


Packages

16-LEAD CERAMIC DIP



20-LEAD PLASTIC DIP



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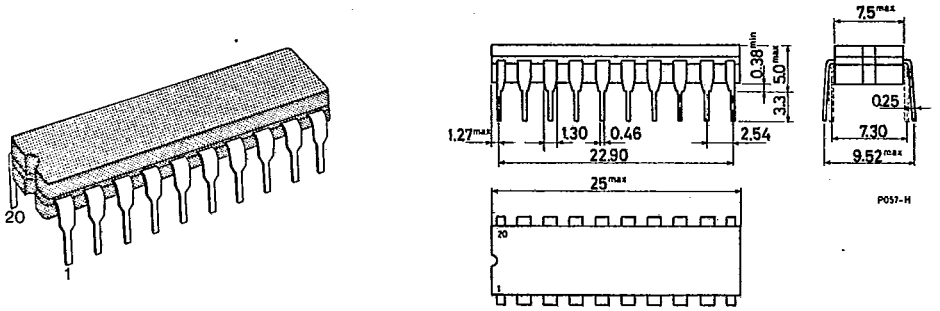
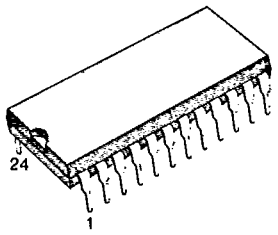
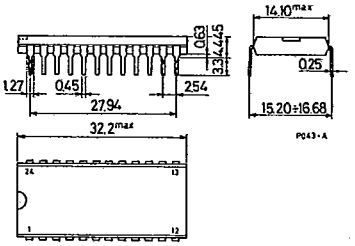


Packages

24-LEAD PLASTIC DIP





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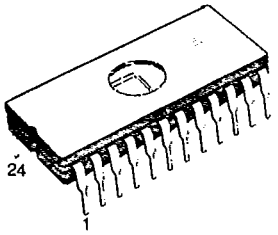
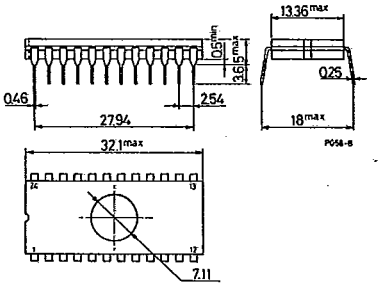
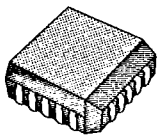
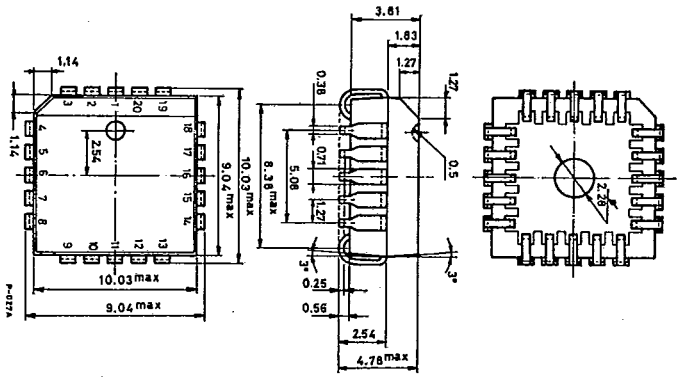




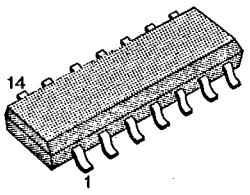
CHIP CARRIER 20 LEAD PLASTIC

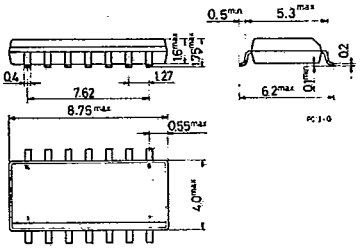




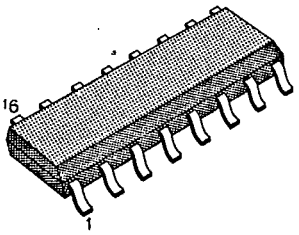
Packages

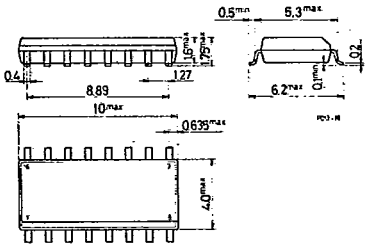
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.