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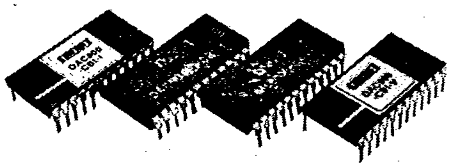
BURR-BROWN®

DAC800
DAC800P



Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR INDUSTRY STANDARD DAC80
- 12-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- DUAL-IN-LINE PACKAGE WITH INDUSTRY STANDARD (DAC80) PINOUT
- HERMETIC PACKAGE (optional)
- TWO PACKAGE OPTIONS: hermetic side-brazed and molded plastic
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES

DESCRIPTION

The DAC800 is a third-generation monolithic Integrated Circuit that is a pin-for-pin equivalent to the industry-standard DAC80 first introduced by Burr-Brown. It has all of the functions of its predecessor plus faster settling time and enhanced reliability because of its monolithic construction.

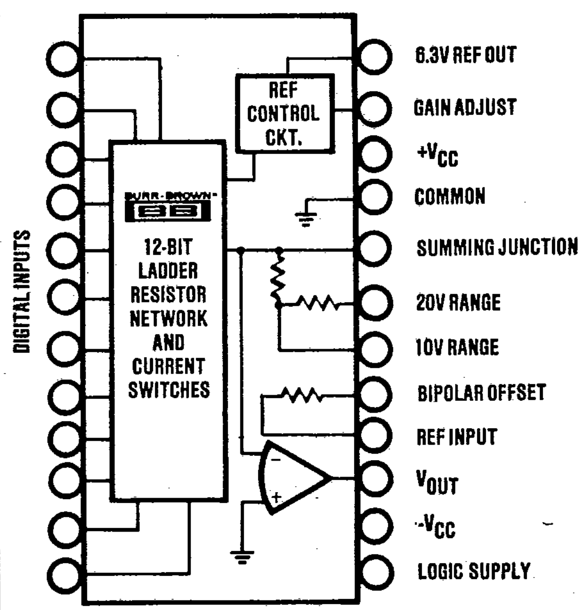
The current output model of the DAC800 is a single-chip integrated circuit containing a subsurface zener reference diode, high speed current switches, and laser-trimmed thin-film resistors. The DAC800 provides output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to −2.35mA (I model).

This high accuracy converter offers a maximum nonlinearity error of ±1/2LSB, ±30ppm/°C maximum gain drift and guaranteed monotonicity, all over 0°C to +70°C. In the bipolar configuration, total drift is guaranteed to be less than 25ppm of FSR/°C.

The DAC800 is in a 24-pin dual-in-line package with the popular DAC80 pinout. Two package options are available: a hermetic ceramic side-brazed package and a low-cost molded plastic package.

For designs that require a wide temperature range, see Burr-Brown models DAC850 and DAC851.

VOLTAGE MODEL



Patents pending may apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and ±V_{CC} = 12V or 15V unless otherwise noted.

MODEL	DAC800, DAC800P			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	bits
Logic Levels (over spec. temp. range)[1]				
V_{IH} (Logic "1")	+2		16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	μA
I_{IL} (V_{IN} = +0.4V)			−0.36	mA
ACCURACY				
Linearity Error at 25°C		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
POWER SUPPLY SENSITIVITY				
+15V and +5V Supplies		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (0°C to +70°C)				
Bipolar Drift (±full-scale drift for the bipolar connection)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.05	±0.12	% of FSR
Gain		±10	±30	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, −7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
Monotonicity Temp. Range, min	0		+70	°C
CONVERSION SPEED, V models				
Settling Time to ±0.01% of FSR				
For FSR Change				
20V range, 2kΩ load		3	5	μs
10V range, 2kΩ load		2.5	4	μs
For 1LSB Change, Major Carry, 2kΩ load		1.5		μs
Slew Rate, 2kΩ load	10	15		V/μs
CONVERSION SPEED, I model				
Settling Time to ±0.01% of FSR				
For FSR Change				
10Ω to 100Ω load		300		nsec
1kΩ load		1		μsec
ANALOG OUTPUT, V models				
Ranges (±V_{CC} = 15V)	±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current[6]	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration		Indefinite		
ANALOG OUTPUT, I model				
Ranges: Bipolar	±0.88	±1.175	±1.47	mA
Unipolar	0 to −1.76	0 to −2.35	0 to −2.94	mA
Output Impedance: Bipolar		3.1		kΩ
Unipolar		7.2		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
Current (for external loads), Source	1.5	2.5		mA
Tempco of Drift		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
±V_{CC}	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5.0	+16.5	VDC
Supply Drain				
+15V, −15V (no load)		+8, −20	+12, −25	mA
+5V (logic supply)		+7	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating[8]	−25		+85	°C
Storage, DAC800P	−60		+100	°C
DAC800	−65		+150	°C

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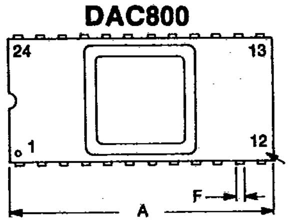
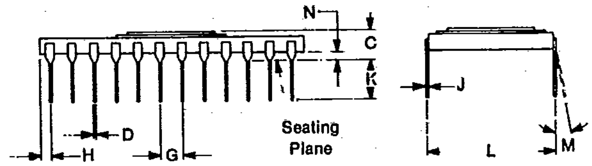
MECHANICAL

DAC800



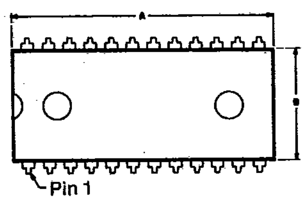
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on kage. package.



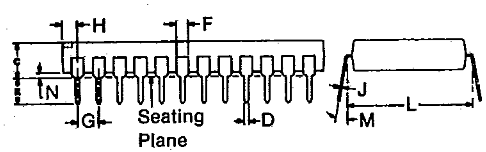
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	–	10°	–	10°
N	.025	.060	0.64	1.52

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 4.1 grams (0.15 oz.)

DAC800P



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



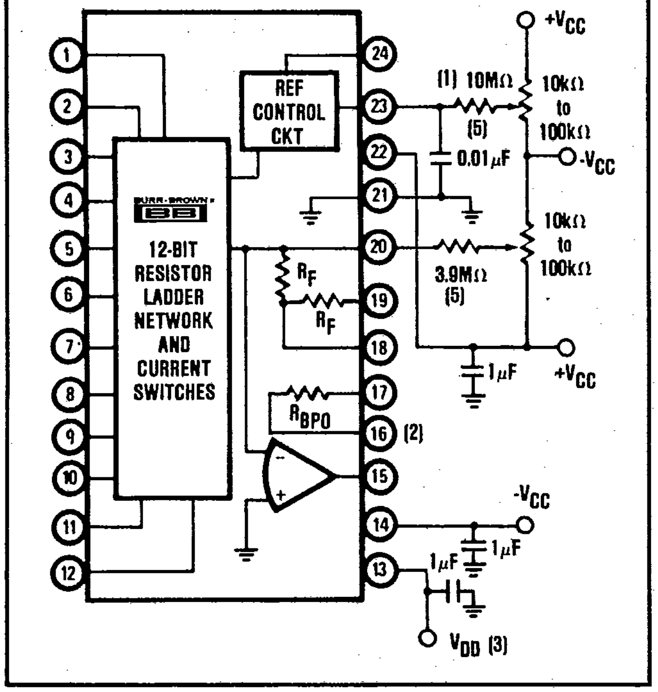
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

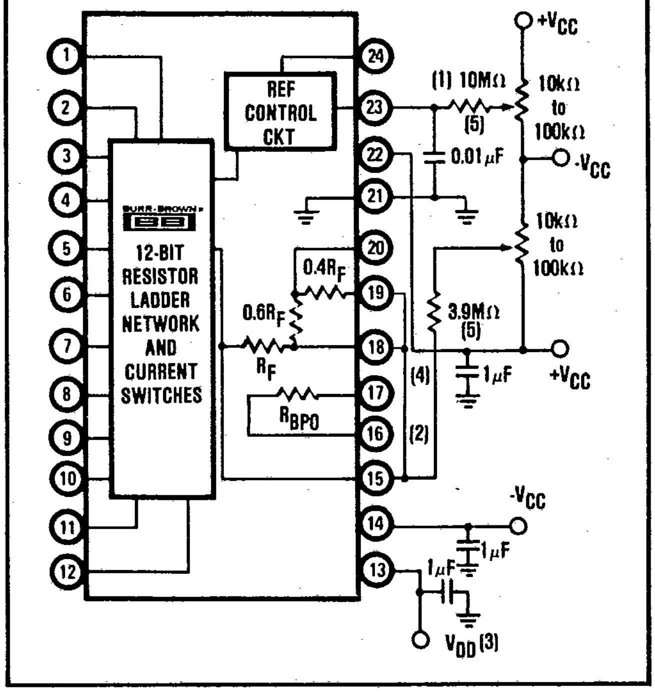
NOTES:
(1) Refer to Logic Input Compatibility.
(2) Adjustable to zero with external trim potentiometer.
(3) FSR means "Full-Scale Range" and is 20V for ±10V range, ±10V for ±5V range, etc.
(4) To maintain drift spec internal feedback resistors must be used for current output models.
(5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
(6) For operation of V models with supply voltages of less than ±13VDC, load current must be limited to ±1mA max.
(7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.
(8) Max operating temperature for DAC800P is +70°C.

CONNECTION DIAGRAMS

Voltage Models



Current Model



PIN ASSIGNMENTS

I MODEL	PIN NO.	V MODELS
(MSB) BIT 1	1	BIT 1 (MSB)
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
(LSB) BIT 12	12	BIT 12 (LSB)
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
$-V_{CC}$	14	$-V_{CC}$
I_{OUT}	15	V_{OUT}
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
$+V_{CC}$	22	$+V_{CC}$
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

NOTES:

1. DAC80 which may be replaced by DAC800 requires a 33MΩ resistor. DAC800 requires a 10MΩ resistor. DAC80's may also be operated with a 10MΩ resistor resulting in increased trim range.
2. Pin 16 of DAC800 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC800 as is possible with DAC80.
3. If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ, 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10mΩ.

ORDERING INFORMATION

Model	Output	Package
DAC800-CBI-I	Current	Side-braze
DAC800-CBI-V	Voltage	Side-braze
DAC800P-CBI-I	Current	Molded plastic
DAC800P-CBI-V	Voltage	Molded plastic

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC800 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes; CSB, CTC, or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC800 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC800 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain Drift is established by: 1) testing the end point differences for each DAC800 model at 0°C, +25°C and +70°C; 2) calculating the gain change with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C.

Offset Drift is a measure of the change in output with all "1"s on the inputs over the specified temperature range. The Offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Bipolar Drift is a measure of the change in plus or minus full-scale output over the specification temperature range for the bipolar connection. Because Bipolar Offset Drift and Gain Drift have canceling interactions, Bipolar Drift is not simply the sum of the two. Total bipolar error over temperature is calculated using Bipolar Drift, then adding ±1/2LSB of linearity error.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Model: Two settling times are specified to ±0.01% of FSR. Each is given for the current model connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

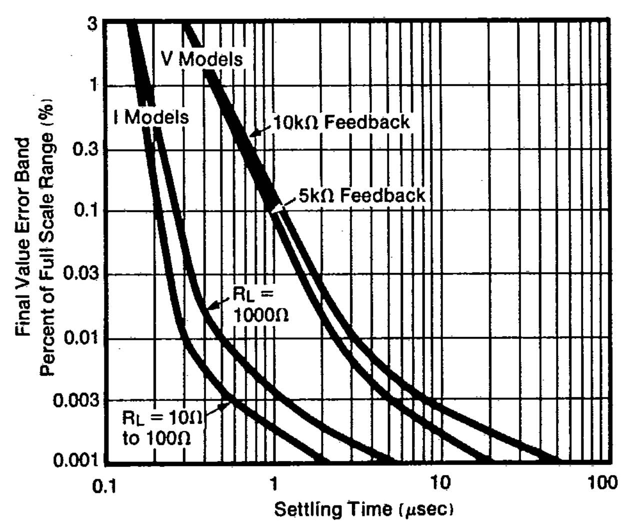


FIGURE 1. Full-Scale Range Settling Time vs Final Value Error Band.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is -2.5V to +2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

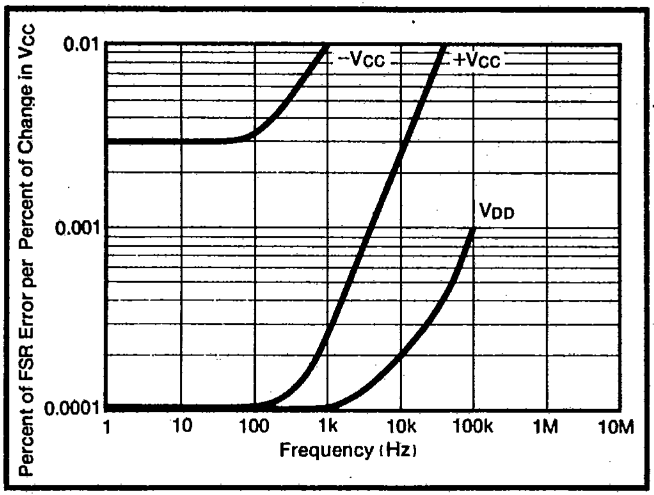


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC800 models have an on-chip +6.3 volt reference. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. Pin 16 is used only to connect the bipolar offset resistor. An external reference mav not be used with DAC800. See Connection Diagrams. The reference voltage may be used to supply external circuits with 2.5mA of current (typical) in addition to the 1mA required by the bipolar offset circuit.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC800. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

±12V OPERATION

The DAC800 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC800 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 4 and 5 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

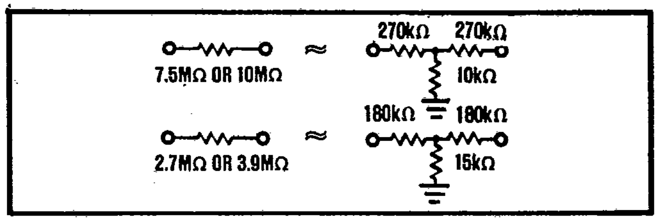


FIGURE 3. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

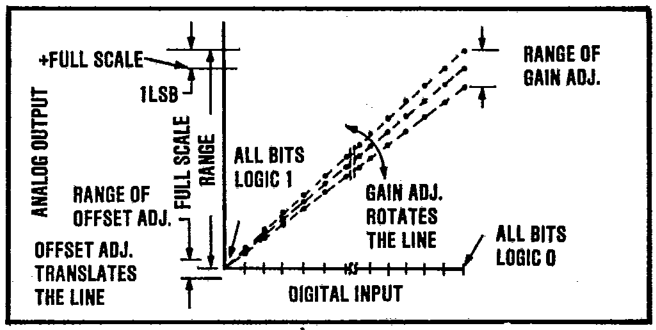


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

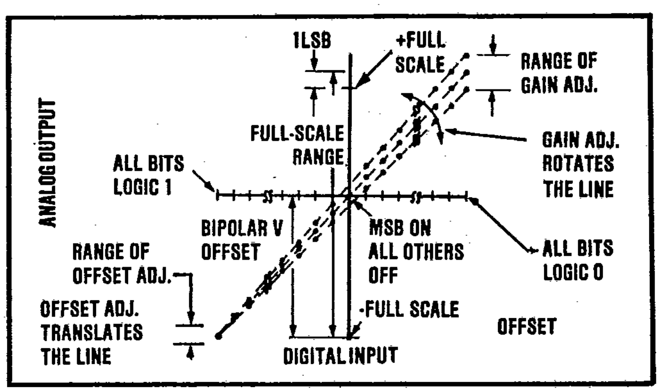


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections. Offset should be adjusted prior to gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

Digital Input	Analog Output: Voltage*		Analog Output: Current	
MSB LSB	0 to +10V	±10V	0 to −2mA	±1mA
000000000000	+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
011111111111	+5.0000V	0.0000V	−1.0000mA	0.0000mA
100000000000	+4.9976V	−0.0049V	−0.9995mA	+0.0005mA
111111111111	0.0000V	−10.0000V	0.0000mA	+1.0000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC800 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

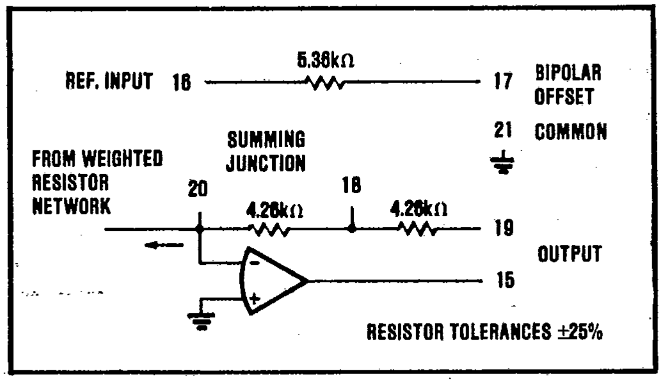


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Voltage Range Connections - Voltage Model DAC800.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 3μsec for the 20-volt range and 2.5μsec for the 10-volt range.

CURRENT OUTPUT MODEL

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

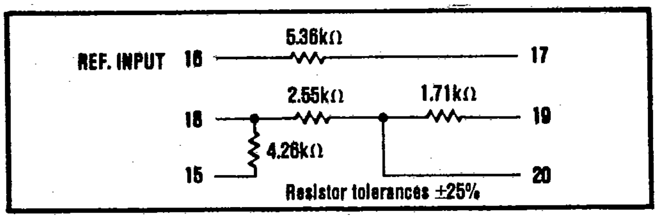


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of

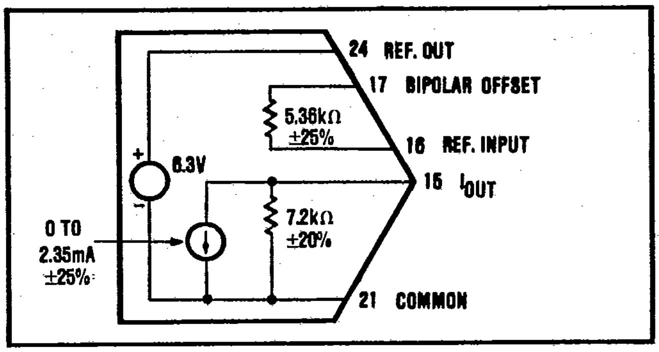


FIGURE 8. Current Output Model Equivalent Output Circuit.

±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

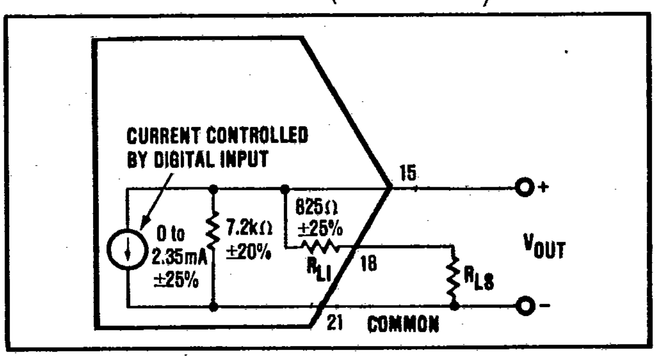


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full-scale output voltage range of 0 to −2V. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175\text{mA}\left(\frac{R_L \times 3.07\text{k}\Omega}{R_L + 3.07\text{k}\Omega}\right)$$

To achieve specified drift, connect 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full-scale output range of ±1V. The tolerances on the internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

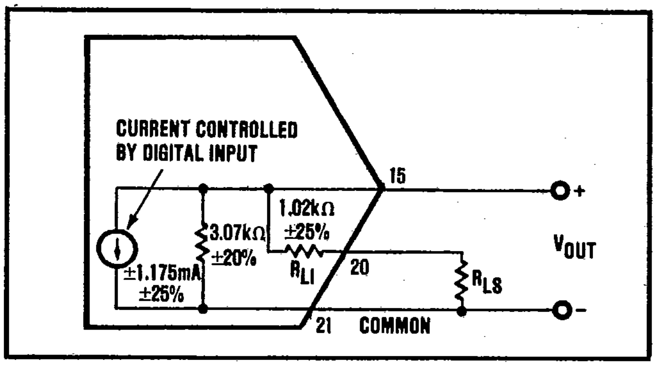


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

Driving An External Op Amp

The current output model DAC800 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 11.

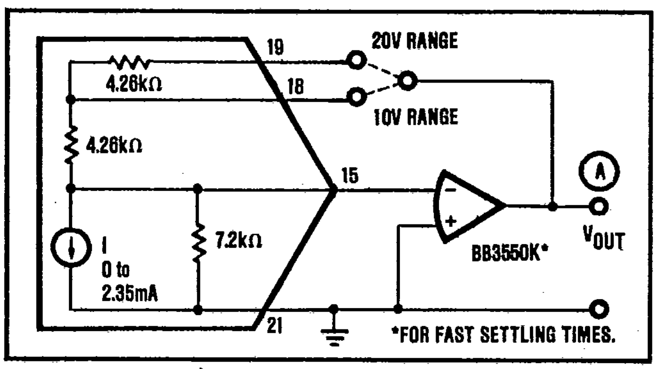


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC800 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC800 provides output voltage ranges the same as the voltage model DAC800. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output DAC800.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA ±25% for bipolar voltage ranges and -2.35mA ±25% for unipolar voltage ranges. See Figure 12. Use protection diodes when a high voltage op amp is used.

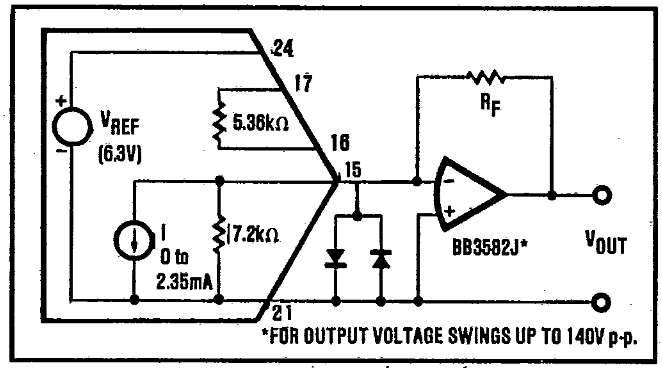


FIGURE 12. External Op Amp - Using External Feedback Resistors.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

LOGIC INPUT COMPATIBILITY

DAC800 digital inputs are TTL, LSTTL and 54/74HC CMOS compatible over the operating range of V_{DD}, +5 to +15V. The input switching threshold remains at the TTL threshold over supply range of V_{DD}, +5V to +15V.

Logic "0" input current over temperature is low enough to permit driving DAC800 directly from outputs of 4000B and 54/74C CMOS devices over the logic power supply range of +5V to +15V.