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ECL Products	

100150

Hex D–Type Latch

FEATURES

- **Typical propagation delay: 0.85ns for the data inputs, 1.2ns for the enable inputs**
- **Typical supply current ($-I_{EE}$): 102mA**

DESCRIPTION

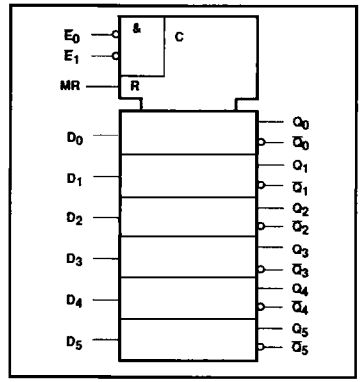
The 100150 contains six D–type latches, with True and Complementary outputs, a pair of common enables ($\overline{E}_0$, $\overline{E}_1$) and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_0$ or $\overline{E}_1$ are Low. When either $\overline{E}_0$ or $\overline{E}_1$ (or both) are High, a latch stores the last valid data present on its D input before $\overline{E}_0$ or $\overline{E}_1$ goes High. The MR input overrides all other inputs and makes the Q output Low.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$\overline{E}_0$, $\overline{E}_1$	Common Enable Inputs
MR	Master Reset Input
$Q_0 - Q_5$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_5$	Complementary Data Outputs

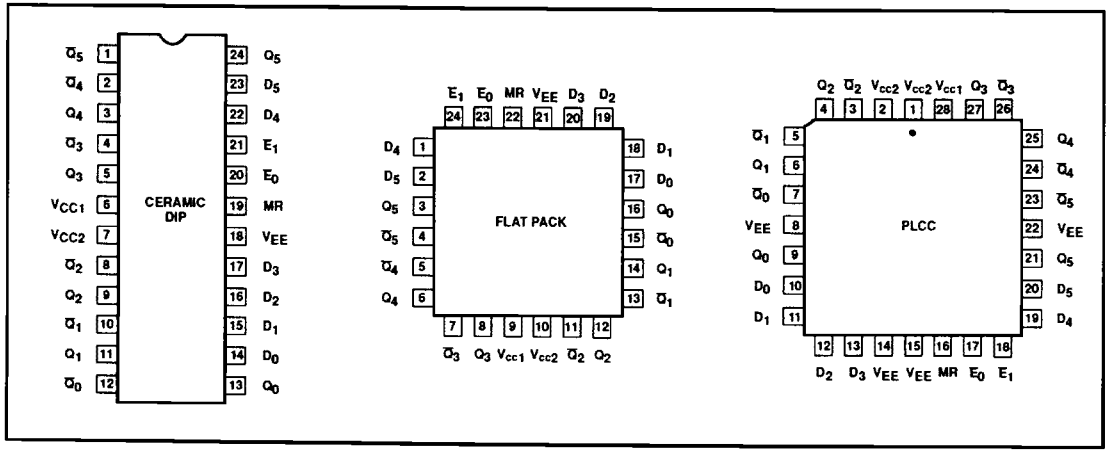
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100150F
24–Pin Ceramic Flat Pack	100150Y
28–Pin PLCC	100150A

PIN CONFIGURATIONS



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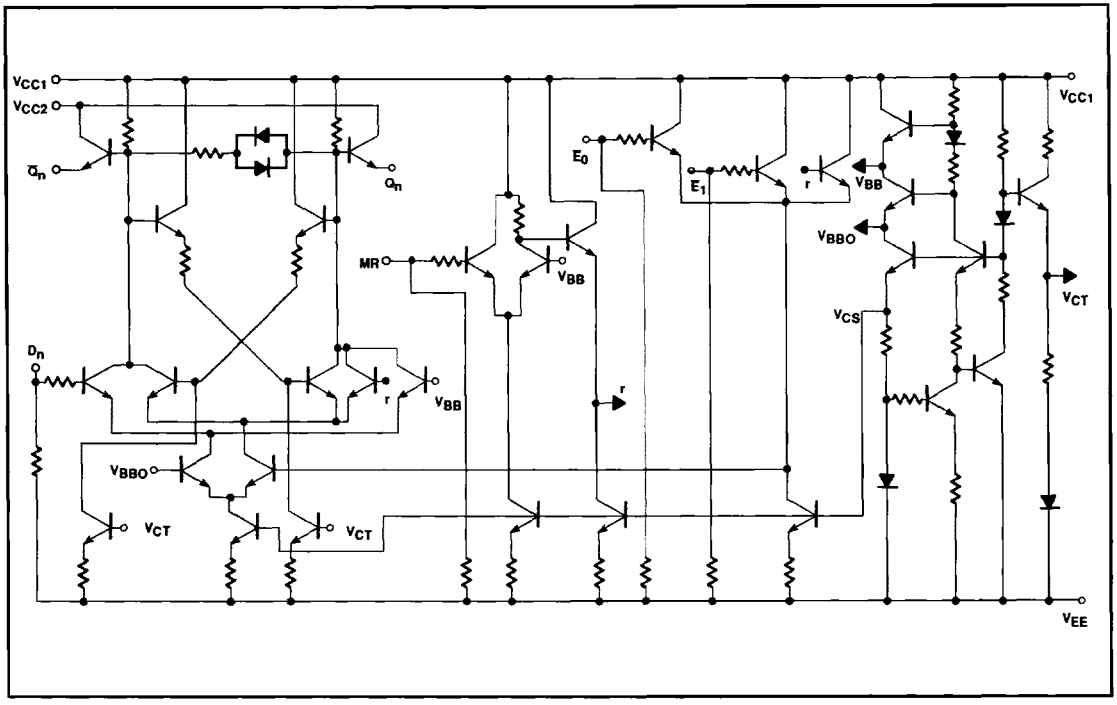
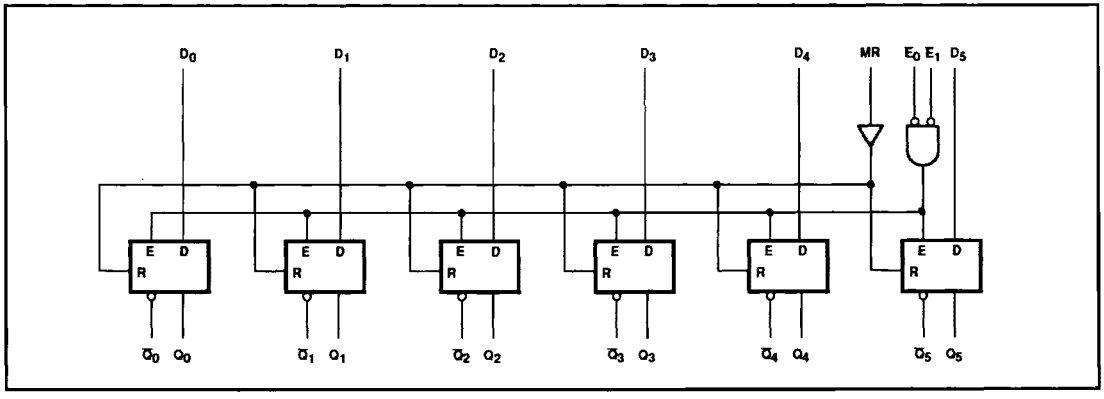
SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



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FUNCTION TABLE (Each Latch)

INPUTS				OUTPUTS	
D_n	$\overline{E}_0$	$\overline{E}_1$	MR	Q_n	$\overline{Q}_n$
H L	L L	L L	L L	H L	L H
X X	X H	H X	L L	Latched* Latched*	Latched* Latched*
X	X	X	H	L	H

NOTES:
* MR signal level present on latch outputs just before rising transition of enable line is held on latch outputs.
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	MR	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.				450	µA
		D_n					340	µA
		$\overline{E}_n$					520	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			79	102	159	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.50 1.50	0.50 0.50	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	2.05 2.05	0.75 0.75	1.85 1.85	0.75 0.75	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.40 2.40	0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.70		0.70		0.70		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.70		0.70		0.70		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.10		2.10		2.10		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.50 1.50	0.50 0.50	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	2.05 2.05	0.75 0.75	1.85 1.85	0.75 0.75	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.40 2.40	0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.70		0.70		0.70		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.70		0.70		0.70		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.10		2.10		2.10		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.30 1.30	0.50 0.50	1.20 1.20	0.50 0.50	1.30 1.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	1.85 1.85	0.75 0.75	1.65 1.65	0.75 0.75	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.60		0.60		0.60		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.60		0.60		0.60		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.00		2.00		2.00		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

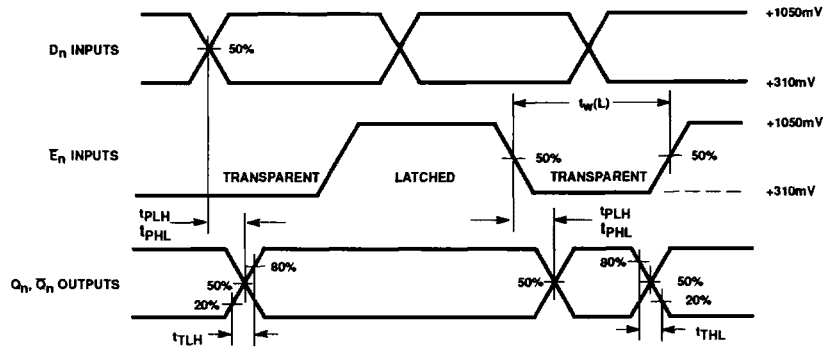
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

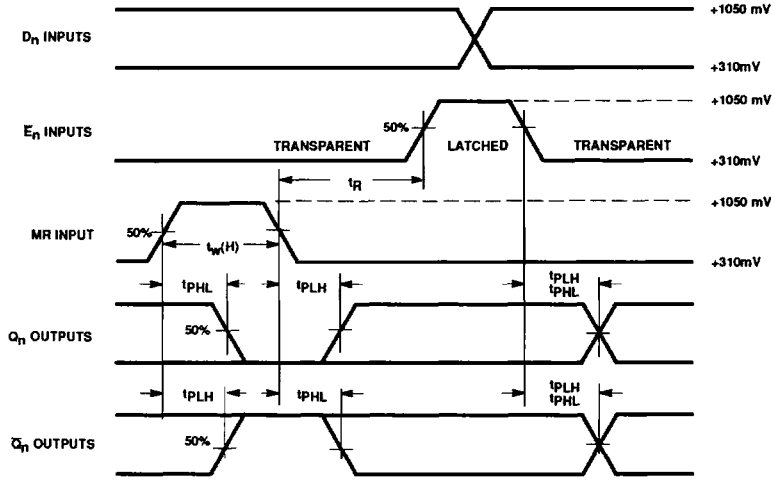
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.30 1.30	0.50 0.50	1.20 1.20	0.50 0.50	1.30 1.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	1.85 1.85	0.75 0.75	1.65 1.65	0.75 0.75	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.60		0.60		0.60		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.60		0.60		0.60		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.00		2.00		2.00		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

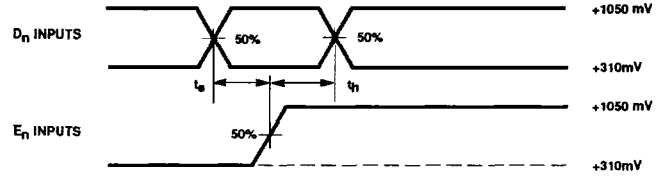
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset Timing



Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.