ADVANCED INFORMATION

CY27C020

256K x 8 CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **—t_{AA} = 70 ns max.**
- **Low power**
  - **—140 mW max.**
  - **—Less than 550 µW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **—32-pin PLCC**
  - **—32-pin TSOP-I**
  - **—32-pin, 600-mil plastic or hermetic DIP**
  - **—32-pin hermetic LCC**

Functional Description

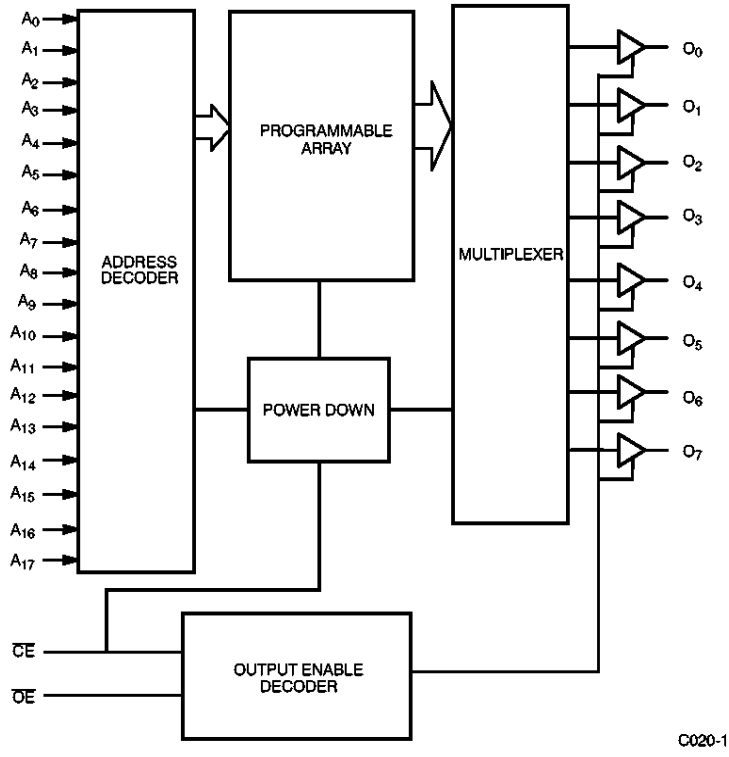
The CY27C020 is a high-performance, 2-megabit CMOS EPROM organized in 256 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C020 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C020 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

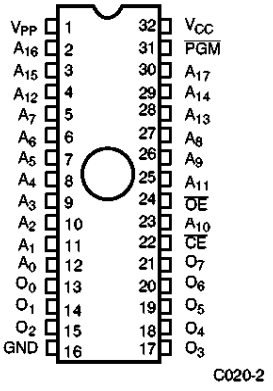
The CY27C020 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{17}-A_0$ will appear at the outputs O_7-O_0.

Logic Block Diagram

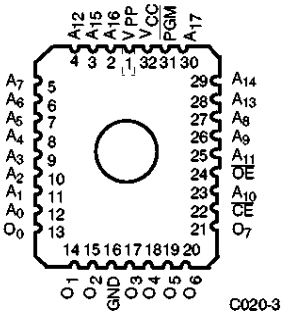


Pin Configurations

DIP
Top View

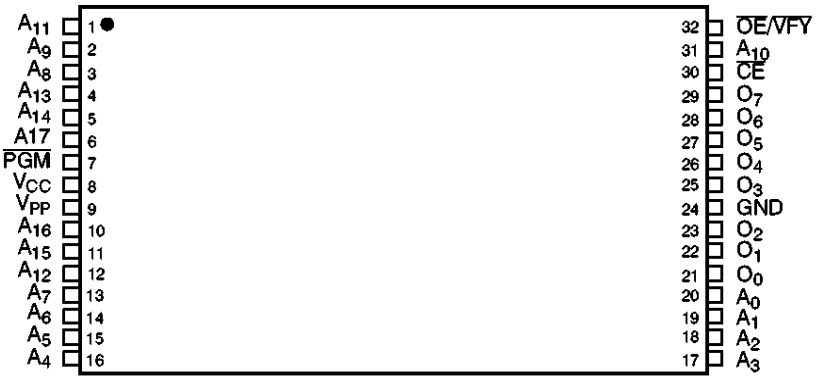


LCC/PLCC
Top View



Pin Configurations (continued)

TSOP
Top View



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Selection Guide

		27C020–70	27C020–90	27C020–120	27C020–150	27C020–200
Maximum Access Time (ns)		70	90	120	150	200
$\overline{CE}$ Access Time (ns)		70	90	120	150	200
$\overline{OE}$ Access Time (ns)		30	35	40	50	60
I_{CC}[1] (mA) Power Supply Current	Com'l	25	25	25	25	25
	Mil		30	30	30	30
I_{SB}[2] (μA) CMOS Stand-by Current		100	100	100	100	100
I_{SB}[3] (mA) TTL Stand-by Current		1	1	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{CC} − 0.3V to V_{CC} + 1.0V.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

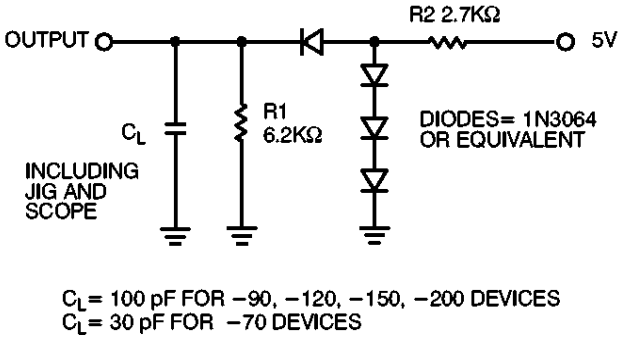
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		25	mA
			Mil		30	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		1	mA
			Mil		1	mA

Capacitance[7]

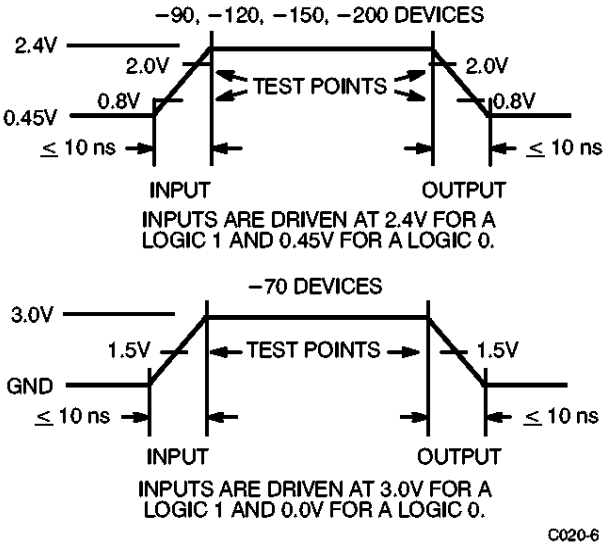
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms



C020-5



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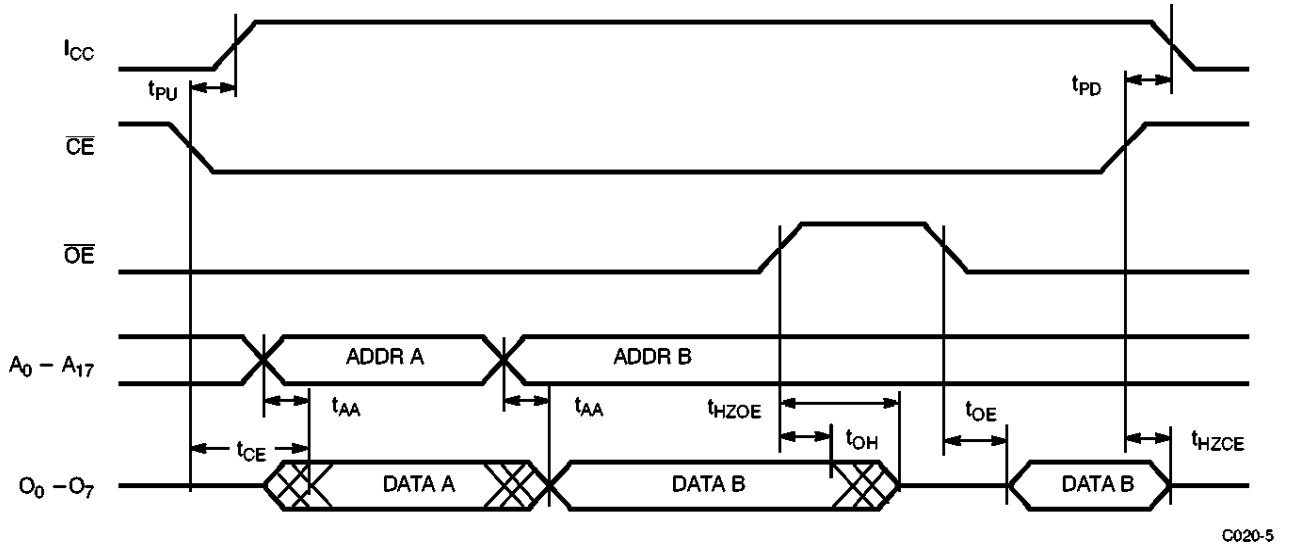
Switching Characteristics Over the Operating Range

Parameter	Description	27C020–70		27C020–90		27C020–120		27C020–150		27C020–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		30		35		40		50		60	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		25		25		30		30		40	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		25		25		30		30		40	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		60		65		65		65		70	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C020 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C020 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function[8]						
	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A_0	A_9	Data
Read	V_{IL}	V_{IL}	X	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	X	V_{IH}	A_0	A_9	High Z
Stand-by (CMOS)	V_{CC} − 0.3V	X	X	V_{IH}	X	X	High Z
Stand-by (TTL)	V_{IH}	X	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{HV}[8]	Note 10

Note:
8. X can be V_{IL} or V_{IH}.
9. V_{HV}=12V±0.5V
10. To be determined.

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C020–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C020–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–70ZC	Z32	32-Lead Thin Small Outline Package	
90	CY27C020–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C020–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C020–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C020–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

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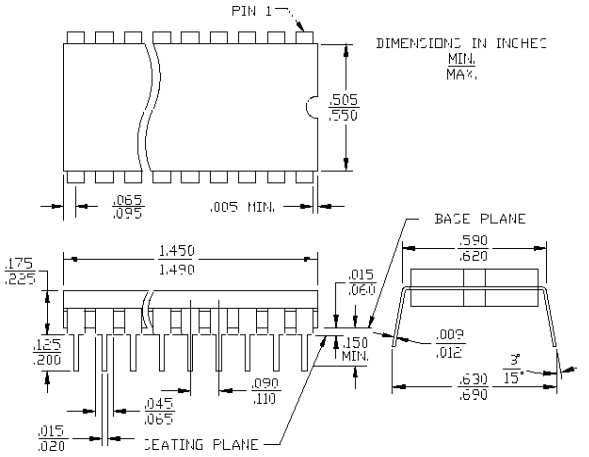
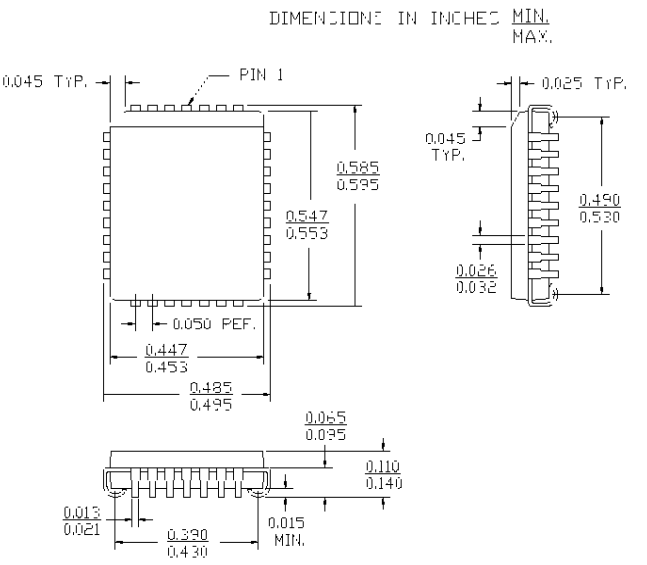
Package Diagrams (continued)

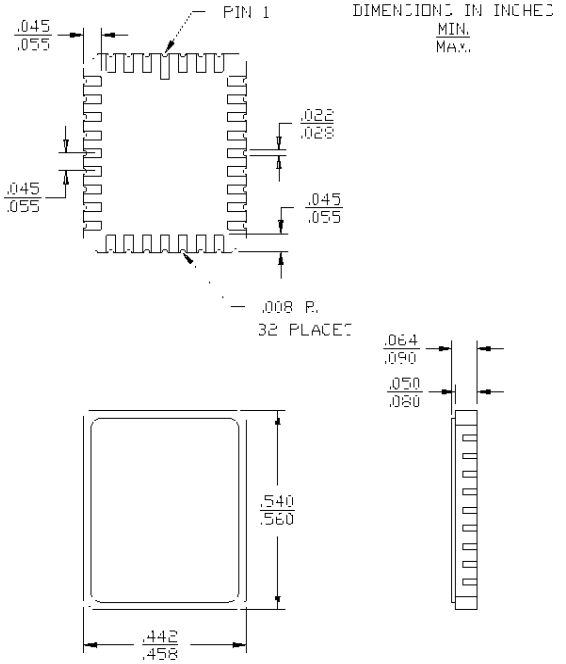
32-Lead (600-Mil) CerDIP D20
MIL−STD−1835 D−10 Config. A



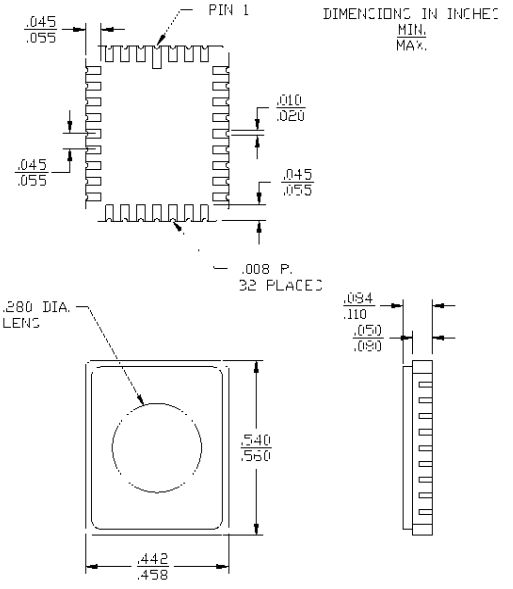
32-Lead Plastic Leaded Chip Carrier J65



32-Pin Rectangular Leadless Chip Carrier L55
MIL−STD−1835 C−12

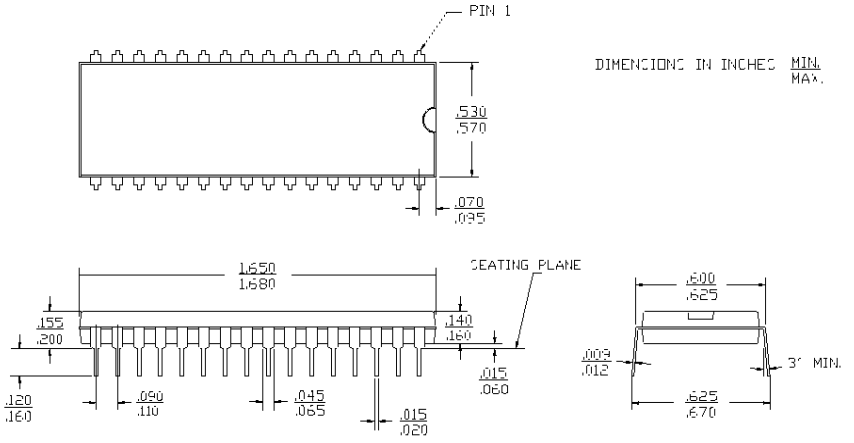


32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL−STD−1835 C−12

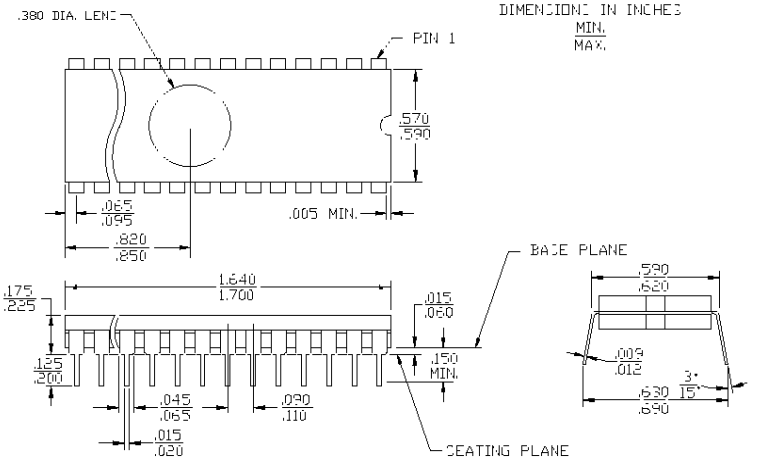


Package Diagrams

32-Lead (600-Mil) Molded DIP P19



32-Lead (600-Mil) Windowed CerDIP W20



Package Diagrams

32-Lead Thin Small Outline Package Z32