Integrated Device Technology, Inc.

FAST CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT16543T/AT/CT/ET
IDT54/74FCT162543T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical tSK(o) (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - VCC = 5V ±10%
- **Features for FCT16543T/AT/CT/ET:**
  - High drive outputs (-32mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
  - Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C
- **Features for FCT162543T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

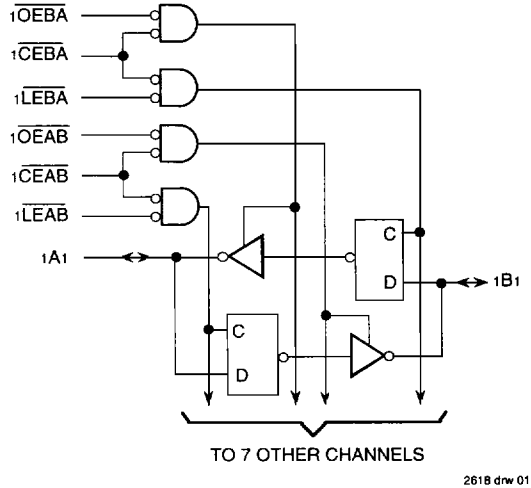
DESCRIPTION:

The FCT16543T/AT/CT/ET and FCT162543T/AT/CT/ET 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW in order to enter data from the A port or to output data from the B port. $x\overline{LEAB}$ controls the latch function. When $x\overline{LEAB}$ is LOW, the latches are transparent. A subsequent LOW-to-HIGH transition of $x\overline{LEAB}$ signal puts the A latches in the storage mode. $x\overline{OEAB}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $x\overline{CEBA}$, $x\overline{LEBA}$, and $x\overline{OEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16543T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162543T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162543T/AT/CT/ET are plug-in replacements for the FCT16543T/AT/CT/ET and 54/74ABT16543 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



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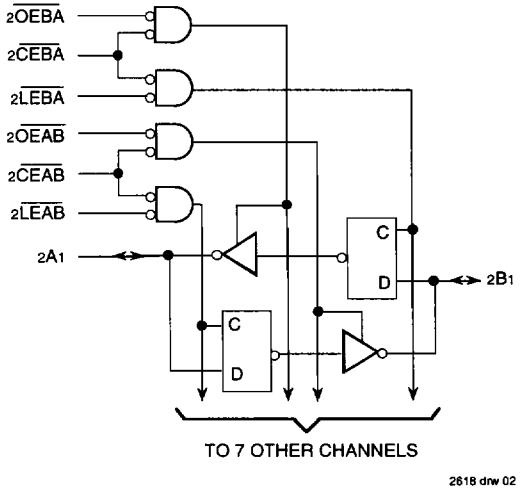

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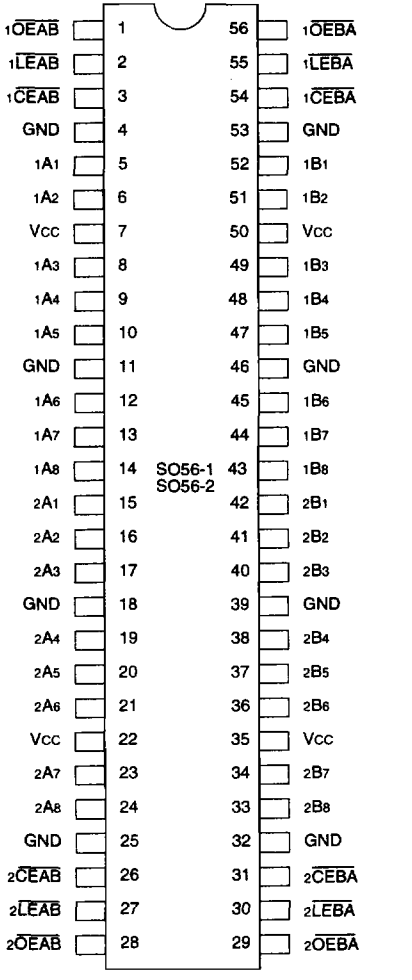
PIN CONFIGURATIONS



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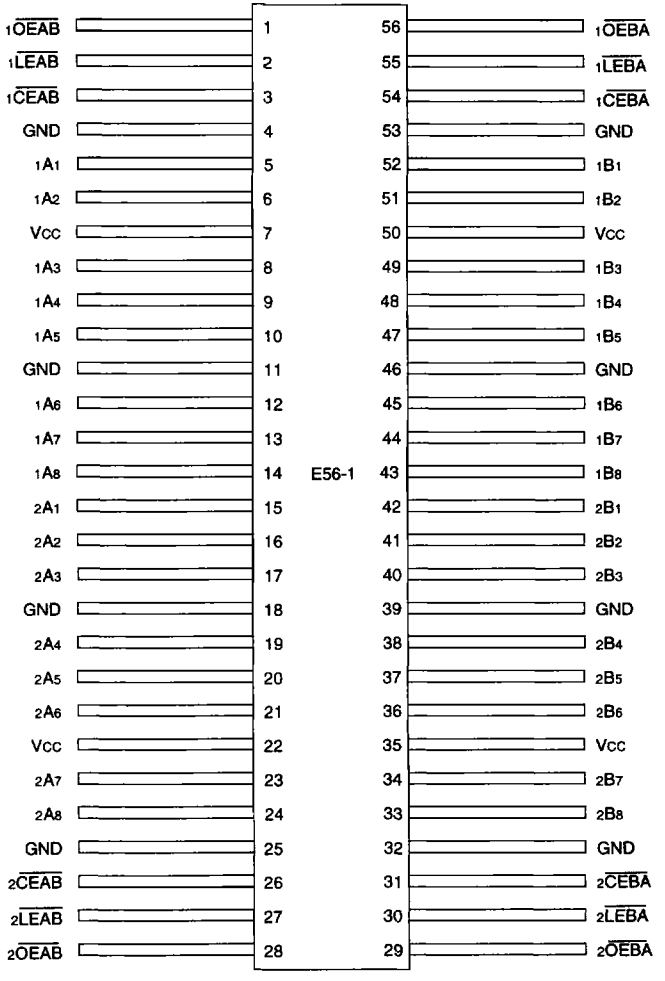
SSOP
TSSOP
TOP VIEW



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CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$x\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$x\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

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FUNCTION TABLE[1, 2]

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$x\overline{CEAB}$	$x\overline{LEAB}$	$x\overline{OEAB}$	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES: 2618 tbl 02

1. * Before $x\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown; B-to-A flow control is the same, except using $x\overline{CEBA}$, $x\overline{LEBA}$ and $x\overline{OEBA}$.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2618 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2618 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2618 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2618 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{CEAB}$ and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$ and $x\overline{OEAB}$= GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$ and $x\overline{OEAB}$= GND $x\overline{CEBA}$ = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16543T/162543T				FCT16543AT/162543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

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Symbol	Parameter	Condition[1]	FCT16543CT/162543CT				FCT16543ET/162543ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		1.5	7.0	1.5	8.0	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	8.0	1.5	9.0	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	6.5	1.5	7.5	1.5	4.0	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.0	—	—	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.0	—	—	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

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NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

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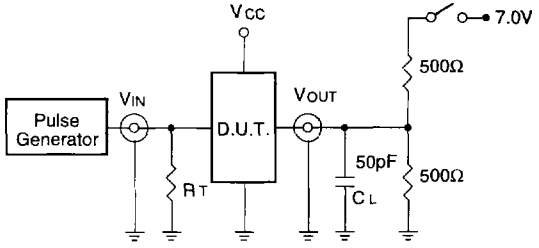
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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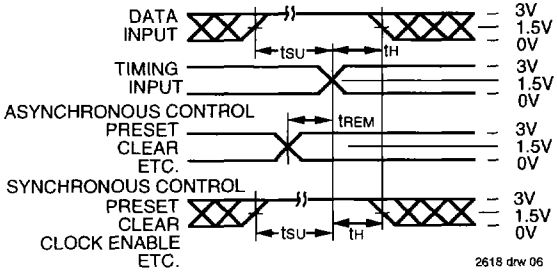
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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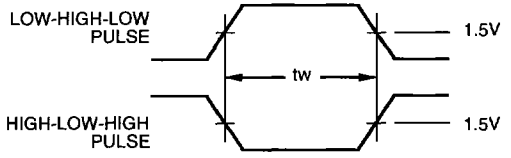
PULSE WIDTH



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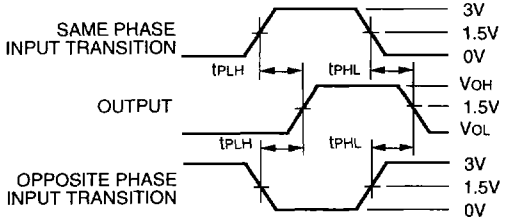
PROPAGATION DELAY



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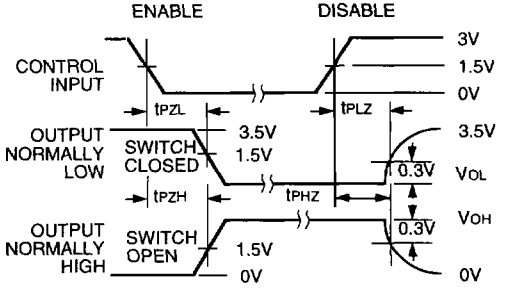
ENABLE AND DISABLE TIMES



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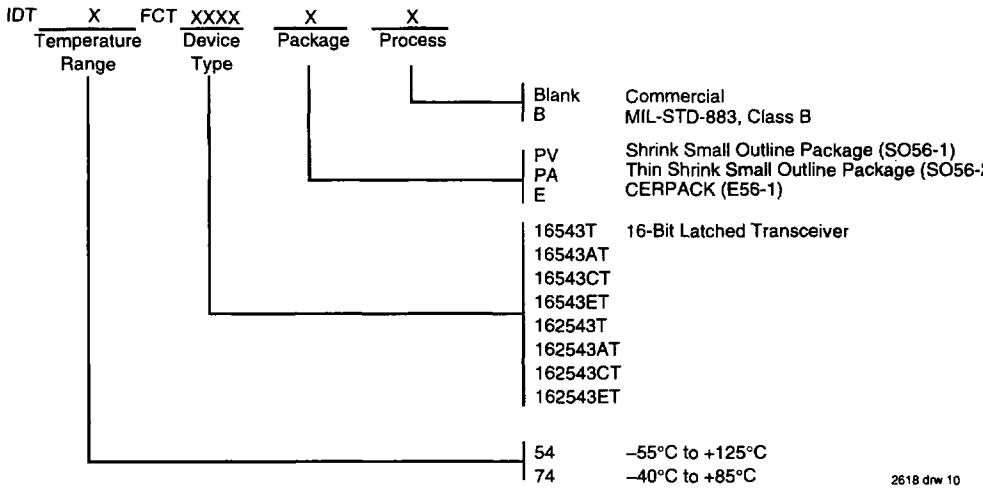
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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