

SN54ABT245, SN74ABT245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS081E – JANUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Plastic (N) and Ceramic (J) DIPs

description

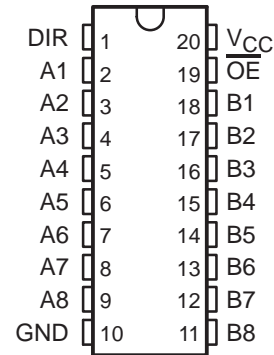
These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

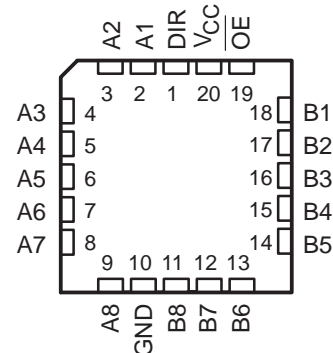
The SN74ABT245A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT245A is characterized for operation from -40°C to 85°C .

SN54ABT245 . . . J OR W PACKAGE
SN74ABT245A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

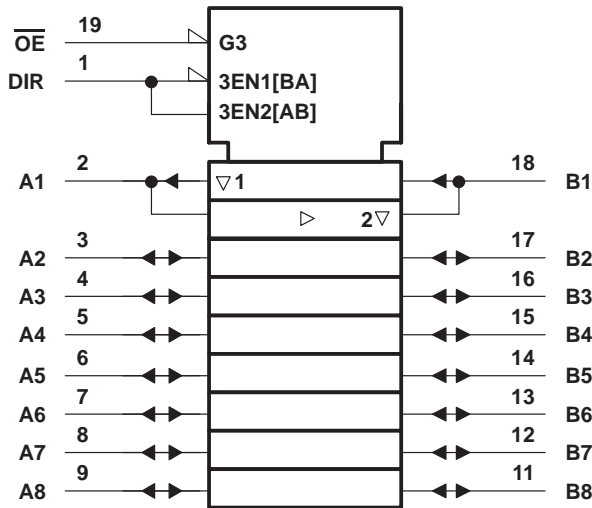
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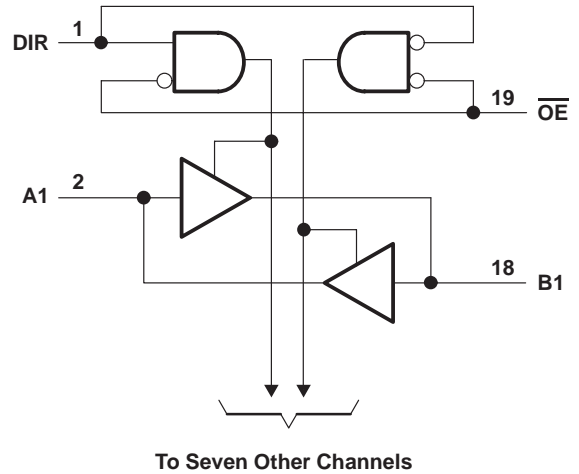
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | -0.5 V to 7 V |
| Voltage applied to any output in the high state or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT245 | 96 mA |
| SN74ABT245A | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package | 0.6 W |
| DW package | 1.6 W |
| N package | 1.3 W |
| PW package | 0.7 W |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

| | SN54ABT245 | | SN74ABT245A | | UNIT |
|--|------------|----------|-------------|----------|--------------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -24 | | -32 | mA |
| I_{OL} Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 5 | | 5 | ns/V |
| $\Delta t/\Delta V_{CC}$ Power-up ramp rate | | | 200 | | μ s/V |
| T_A Operating free-air temperature | -55 | 125 | -40 | 85 | $^{\circ}$ C |

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | SN54ABT245 | | SN74ABT245A | | UNIT | |
|--------------------------|--|--|------------------|------|------------|-------|-------------|------|------|----|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V | |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -3 mA | | | 2.5 | | 2.5 | | 2.5 | V | |
| | V _{CC} = 5 V, I _{OH} = -3 mA | | | 3 | | 3 | | 3 | | |
| | V _{CC} = 4.5 V | I _{OH} = -24 mA | | | 2 | | 2 | | | |
| I _{OH} = -32 mA | | | | 2* | | | | 2 | | |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 48 mA | | | | 0.55 | | 0.55 | V | |
| | | I _{OL} = 64 mA | | | | 0.55* | | 0.55 | | |
| I _I | Control inputs | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | | | | ±1 | | ±1 | μA | |
| | A or B ports | V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND | | | | ±20 | | ±100 | | |
| I _{OZPU} | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | | | ±50 | μA | |
| I _{OZPD} | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | | | ±50 | μA | |
| I _{OZH} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V | | | 10 | | 10 | | 10 | μA | |
| I _{OZL} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V | | | -10 | | -10 | | -10 | μA | |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±100 | | | | ±100 | μA | |
| I _{CEX} | Outputs high | V _{CC} = 5.5 V, V _O = 5.5 V | | | | 50 | | 50 | μA | |
| I _O § | | V _{CC} = 5.5 V, V _O = 2.5 V | | | -50 | -140 | -180 | -50 | -180 | mA |
| I _{CC} | A or B ports | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | | 5 | 250 | 250 | 250 | μA |
| | | | Outputs low | | | 22 | 30 | 30 | 30 | mA |
| | | | Outputs disabled | | | 1 | 250 | 250 | 250 | μA |
| ΔI _{CC} ¶ | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | | 1.5 | | 1.5 | 1.5 | mA |
| | | | Outputs disabled | | | 50 | | 50 | 50 | μA |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | | 1.5 | | 1.5 | | 1.5 | mA |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | | | 4 | | | | pF | |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | | | 8 | | | | pF | |

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

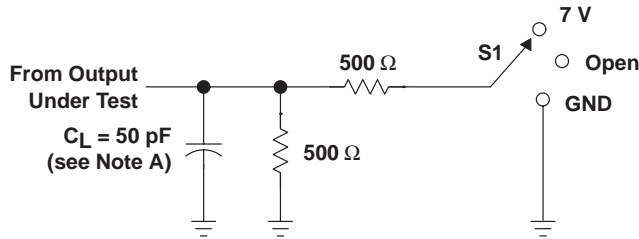
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT245 | | | | SN74ABT245A | | | | UNIT | | |
|-----------|-----------------|-------------|---|-----|-----|-----|-------------|---|-----|-----|------|-----|-----|
| | | | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | MIN | MAX | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | | MIN | MAX |
| | | | MIN | TYP | MAX | | | MIN | TYP | MAX | | | |
| t_{PLH} | A or B | B or A | 1 | 2.6 | 4.1 | 1 | 4.8 | 1 | 2 | 3.2 | 1 | 3.6 | ns |
| t_{PHL} | | | 1 | 2.9 | 4.2 | 1 | 4.8 | 1 | 2.6 | 3.5 | 1 | 3.9 | |
| t_{PZH} | \overline{OE} | A or B | 1.3 | 3.3 | 4.8 | 1 | 5.9 | 2 | 3.5 | 4.5 | 2 | 5.6 | ns |
| t_{PZL} | | | 2.3 | 4.3 | 5.8 | 2 | 7.5 | 1.9 | 4 | 5.3 | 1.9 | 6.2 | |
| t_{PHZ} | \overline{OE} | A or B | 1.7 [†] | 4.7 | 6.2 | 1.7 | 7.4 | 2.2 | 4.4 | 5.4 | 2.2 | 5.9 | ns |
| t_{PLZ} | | | 1.7 [†] | 4.3 | 5.8 | 1.7 | 6.5 | 1.5 | 3 | 4 | 1.5 | 4.5 | |

[†] This data sheet limit may vary among suppliers.

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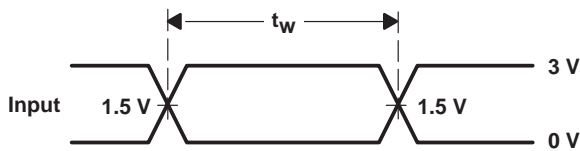
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PARAMETER MEASUREMENT INFORMATION

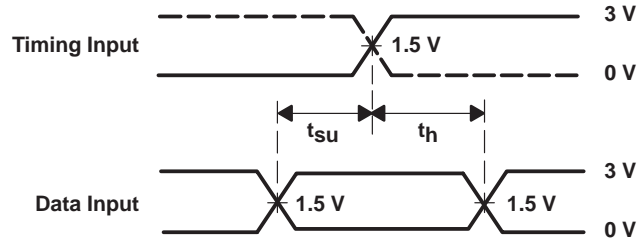


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

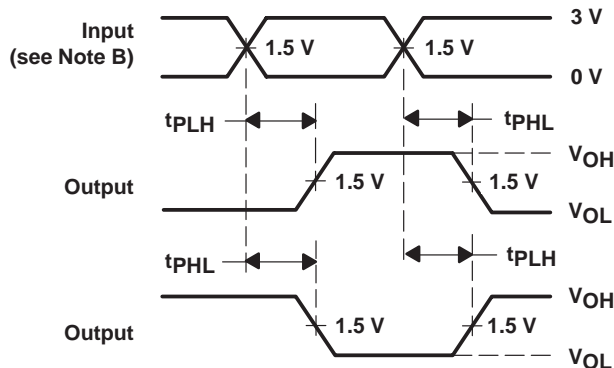
LOAD CIRCUIT FOR OUTPUTS



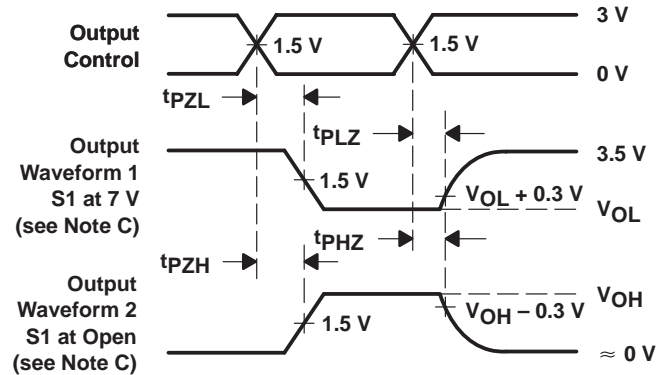
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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