CY2XL12

Low RMS Phase Jitter Programmable LVDS Clock Generator

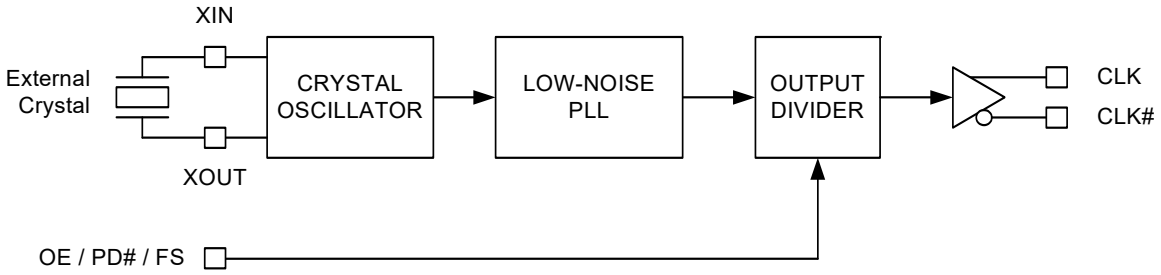
Features

- Programmable LVDS clock generator
- Low RMS Phase Jitter
- Available output frequencies: 50 MHz to 700 MHz
- Package: Pb-free 8-pin thin shrunk small outline package (TSSOP)
- Supply voltage: 3.3 V or 2.5 V
- Temperature: Industrial

Functional Description

The CY2XL12 is a phase locked loop (PLL)-based high-performance clock generator that uses Cypress's low-noise voltage control oscillator (VCO) technology to achieve less than 1 ps typical RMS phase jitter. The CY2XL12 uses an external crystal reference input and drives one LVDS output pair having programmable drive strength. CY2XL12 can be programmed as Output Enable (OE), or Power Down (PD#), or Frequency Select (FS) device by configuring the pin 5. The device can be programmed either to operate at 3.3 V or at 2.5 V.

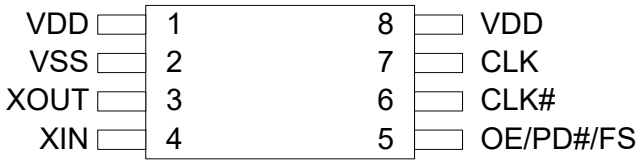
Logic Block Diagram



Contents

Pinouts

Figure 1. 8-pin TSSOP pinout



Pin Definitions

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	OE / PD# / FS	CMOS input	Output enable pin: Active HIGH. If OE=1, CLK is enabled. When LOW, the output is high impedance Power-down pin: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. Frequency Select pin: One of the two stored frequencies can be selected.
6, 7	CLK#, CLK	LVDS output	Differential clock output; drives one or two LVDS loads

Frequency Table

Part Number	Crystal Frequency	Output Frequency	Drive Strength	Pin 5 Function	RMS Phase Jitter (Random)	
					Offset Range	Jitter (Typical)
CY2XL12ZXI01	25 MHz	108 MHz	High	OE	637 kHz to 10 MHz	0.55 ps
CY2XL12ZXI02	25 MHz	100 MHz	High	OE	637 kHz to 10 MHz	0.53 ps
CY2XL12ZXI03	25 MHz	150 MHz	High	OE	637 kHz to 10 MHz	0.48 ps
CY2XL12ZXI06	25 MHz	50 MHz	Normal	PD#	12 kHz to 20 MHz	1.0 ps

Functional Overview

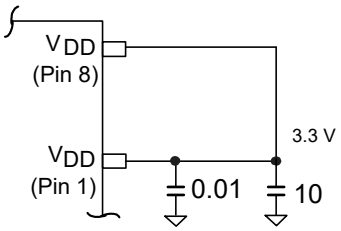
The CY2XL12 device with external crystal option has OE or PD# or FS feature of Pin 5. The OE function is used to enable or disable CLK output. PD# function can quickly put the device in low-power state, but it takes longer time to wake-up because of reacquire of PLL lock. FS feature is used to select two different output frequencies for multirate serializer application.

Application Information

Power Supply Filtering Techniques

As in any high-speed analog circuitry, noise at the power-supply pins can degrade performance. To achieve optimum jitter performance, use good power-supply isolation practices. Figure 2 illustrates a typical filtering scheme. Because all the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low-impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

Figure 2. Power Supply Filtering



Board Layout and OE Pin

If the Output Enable (OE) function on pin 5 is not needed, it may be connected directly to the V_{DD} plane by a wide trace and multiple vias. This improves heat dissipation. A resistor between OE and V_{DD} is not necessary.

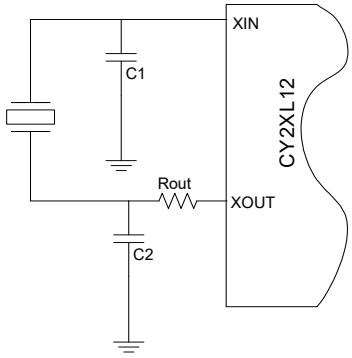
Termination for LVDS Output

The CY2XL12 is designed with programmable output drive-strength. When it is configured with High-drive, it can drive two standard LVDS loads, each one with a 100 Ω termination resistor. Figure 5 on page 5 shows the standard termination scheme. When it is programmed for Normal-drive, it can drive only one standard LVDS load (100 Ω termination resistor) as shown in Figure 6. The termination resistors should always be located very close to the receivers, and the trace branches should be located close to the CY2XL12 output. To minimize signal reflections from the receivers, the differential impedance (Z_0) of each trace pair should be 100 Ω to match the termination resistor.

Crystal Interface

CY2XL12 should have minimum 8 pF load capacitor parallel to the resonant crystal. The capacitors C1 and C2 as shown in Figure 3 are chosen to minimize the ppm error. These optimum values of C1 and C2 can be derived based on the parasitic trace capacitance (Cp), and capacitance of the CY2XL12 device pins (XIN and XOUT). Values of C1 and C2 are layout dependant and can be calculated as C1 = C2 = 2 × (CL – Cp). When the drive level of the crystal is low and the drive level of CY2XL12 is high, the application may need an additional resistor Rout. When Rout is added, C2 is also required to be readjusted for the precise frequency calculation.

Figure 3. Crystal Input Interface



Termination Circuits

Figure 4. Test Load

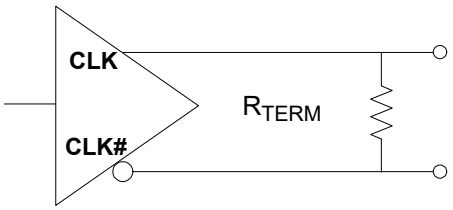


Figure 5. Application Load (High drive strength device)

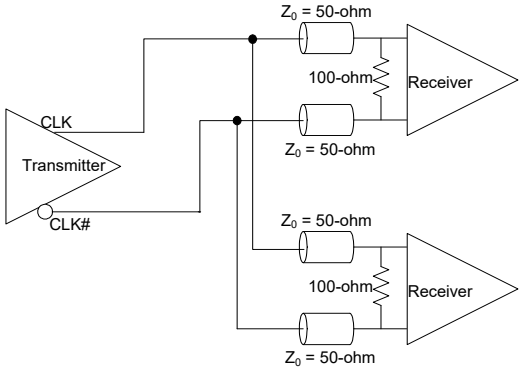
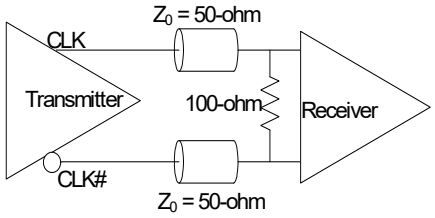
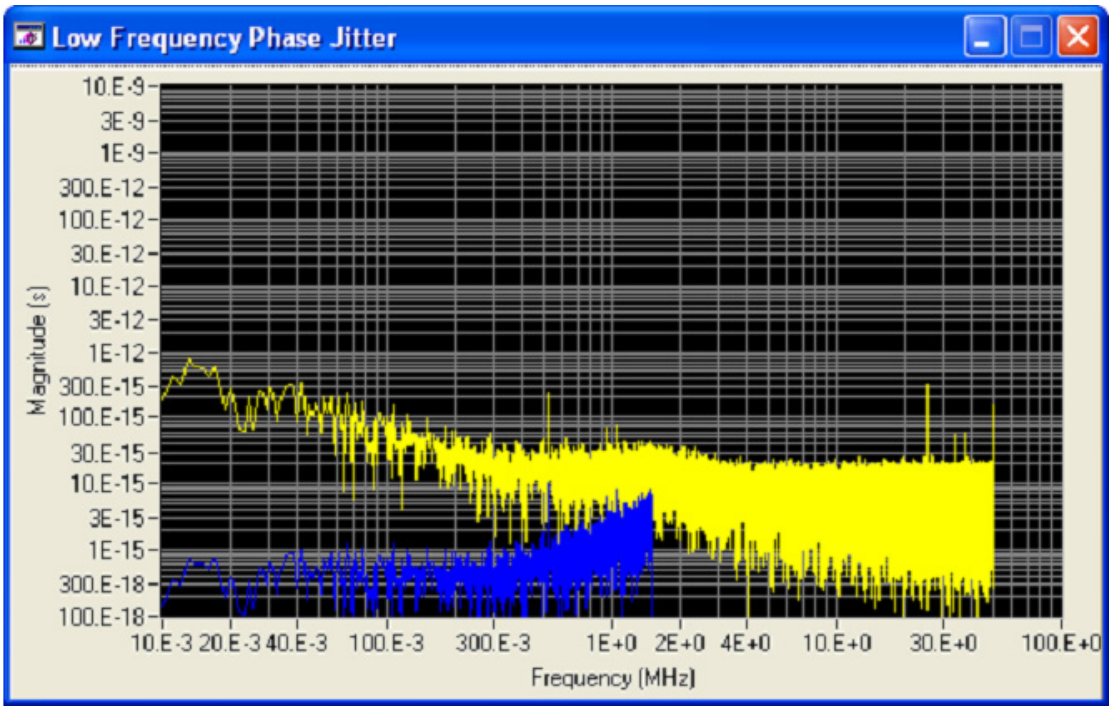


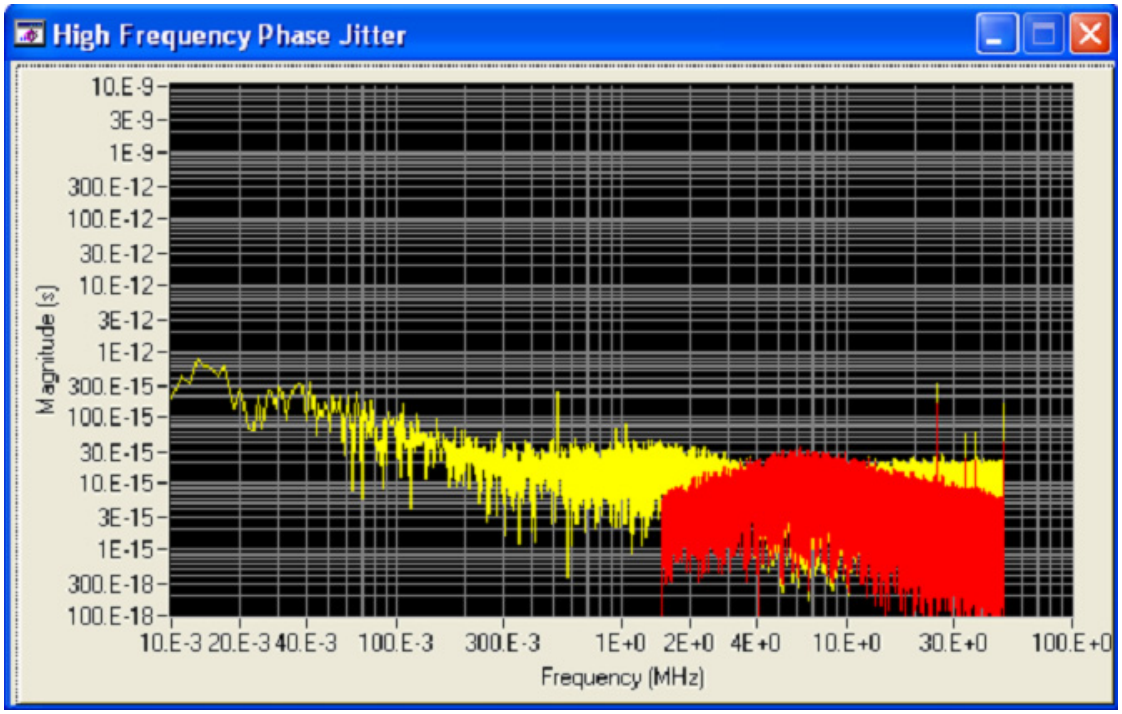
Figure 6. Application Load (Nominal drive strength device)



Phase Jitter

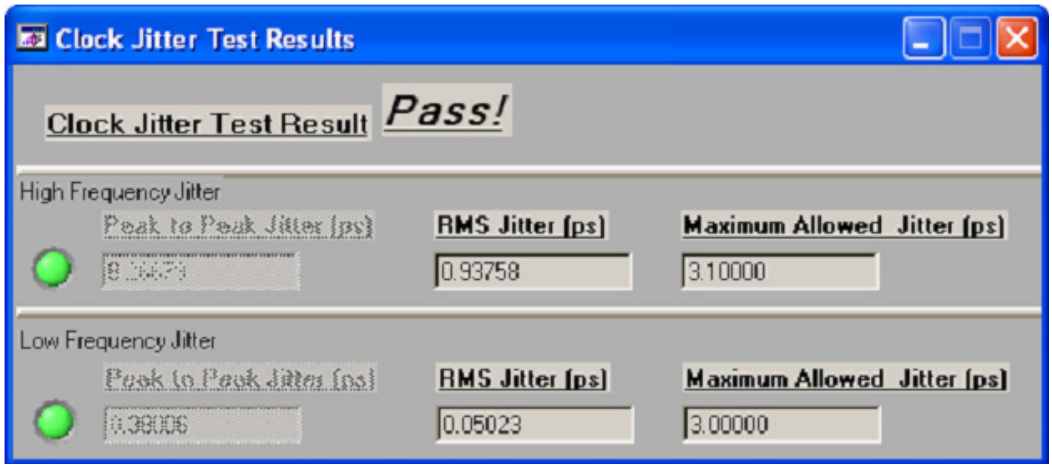
(PCIe 2.0 Check using Clock Jitter 1.3 Tool)





Phase Jitter (continued)

(PCIe 2.0 Check using Clock Jitter 1.3 Tool)



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[1]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–65	150	°C
T_J	Temperature, Junction		–	135	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (human body model)	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability rating	At 1/8 in.	V–0		–
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3 V supply voltage	3.135	3.465	V
	2.5 V supply voltage	2.375	2.625	V
T_A	Ambient temperature, industrial	–40	85	°C
T_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (ensure power ramp is monotonic)	0.05	500	ms

Notes
1. The voltage on any input or I/O pin cannot exceed the V_{DD} pins during power-up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 × 114 × 1.6 mm and has four layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metallization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}[3]	Power supply current with output terminated	V_{DD} = 3.465 V, OE = V_{DD}, output terminated	–	–	125	mA
		V_{DD} = 2.625 V, OE = V_{DD}, output terminated	–	–	120	mA
V_{OD}[4]	LVDS differential output voltage	V_{DD} = 3.3 V or 2.5 V. R_{TERM} = 50 Ω between CLK and CLK#, High Drive Strength R_{TERM} = 100 Ω between CLK and CLK#, Normal Drive Strength	247	–	454	mV
ΔV_{OD}[4]	Change in V_{OD} between complementary output states	V_{DD} = 3.3 V or 2.5 V. R_{TERM} = 50 Ω between CLK and CLK#, High Drive Strength R_{TERM} = 100 Ω between CLK and CLK#, Normal Drive Strength	–	–	50	mV
V_{OS}[5]	LVDS offset output voltage	V_{DD} = 3.3 V or 2.5 V. R_{TERM} = 50 Ω between CLK and CLK#, High Drive Strength R_{TERM} = 100 Ω between CLK and CLK#, Normal Drive Strength	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	V_{DD} = 3.3 V or 2.5 V. R_{TERM} = 50 Ω between CLK and CLK#, High Drive Strength R_{TERM} = 100 Ω between CLK and CLK#, Normal Drive Strength	–	–	50	mV
I_{OZ}	Output leakage current	Three-state output, unterminated, measured on one pin while floating the other pin, OE = V_{SS}	–35	–	35	µA
I_{SB}	Standby supply current.	PD# = Vss			200	µA
V_{IH}	Input high voltage, pin 5		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage, pin 5		-0.3	–	0.3 × V_{DD}	V
I_{IH}	Input high current, pin 5	Input = V_{DD}	–	–	115	µA
I_{IL}	Input low current, pin 5	Input = V_{SS}	–50	–	–	µA
C_{IN}	Input capacitance, pin 5		–	15	–	pF
C_{INX}	Pin capacitance, XIN & XOUT		–	4.5	–	pF

Notes
3. I_{DD} includes ~8 mA of current that is dissipated externally in the output termination resistor.
4. Refer to Figure 7 on page 11.
5. Refer to Figure 8 on page 11 and Figure 9 on page 11.

AC Electrical Characteristics

Parameter [6, 7]	Description	Test Conditions	Min	Typ	Max	Unit
F_{OUT}[8]	Output frequency			See note 8		MHz
T_R, T_F[9]	Output rise or fall time	20% to 80% of full output swing	–	0.5	1.0	ns
$T_{Jitter(\phi)}$[8, 10]	RMS phase jitter (Random)			See note 8		ps
T_{DC}[11]	Duty cycle	Measured at zero crossing point	45	–	55	%
T_{OHZ}[12]	Output disable time	Time from falling edge on OE to stopped outputs (asynchronous)	–	–	100	ns
T_{OE}[12]	Output enable time	Time from rising edge on OE to outputs at a valid frequency (asynchronous)	–	–	120	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time $V_{DD} = V_{DD(min)}$	–	–	5	ms

Crystal Characteristics

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
F_{IN}	Crystal frequency	8–14	14–28	28–48	MHz
R1	Maximum motional resistance (ESR)	135	50	30	Ω
CL	Parallel load capacitance (see Note 6 below)	8–18	8–14	8–12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

Notes
6. Not 100% tested, guaranteed by design and characterization.
7. Outputs are terminated with 50 Ω between CLK and CLK#. Refer to Figure 4 on page 5.
8. Crystal frequency, output frequency, and typical phase jitter are listed in Frequency Table on page 3.
9. Refer to Figure 9 on page 11.
10. Refer to Figure 13 on page 12.
11. Refer to Figure 10 on page 11.
12. Refer to Figure 11 on page 11.

Switching Waveforms

Figure 7. Output Voltage Swing

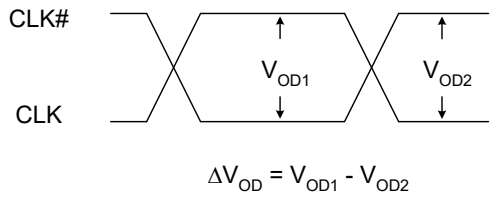


Figure 8. Output Offset Voltage (High Drive Strength)

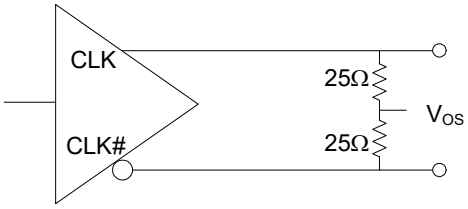


Figure 9. Output Rise or Fall Time (Normal Drive Strength)

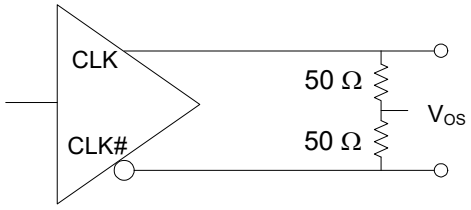


Figure 10. Duty Cycle Timing

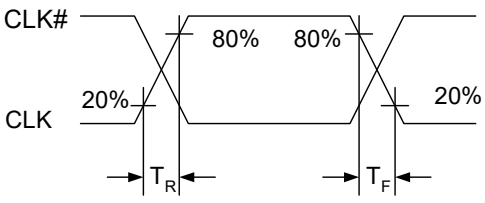
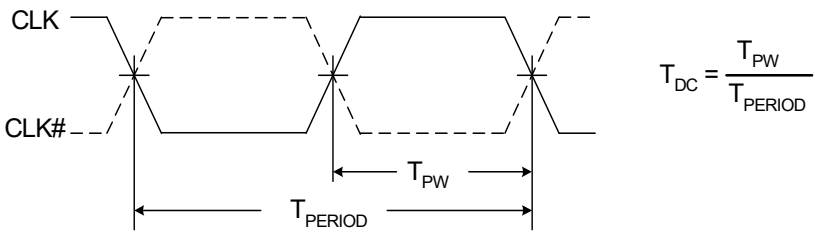


Figure 11. Output Enable and Disable Timing



Switching Waveforms (continued)

Figure 12. Output Enable and Disable Timing

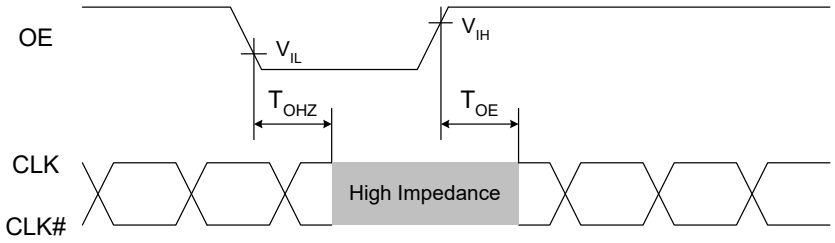
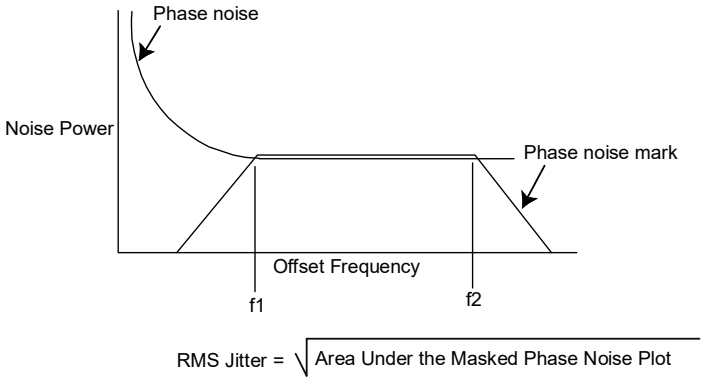


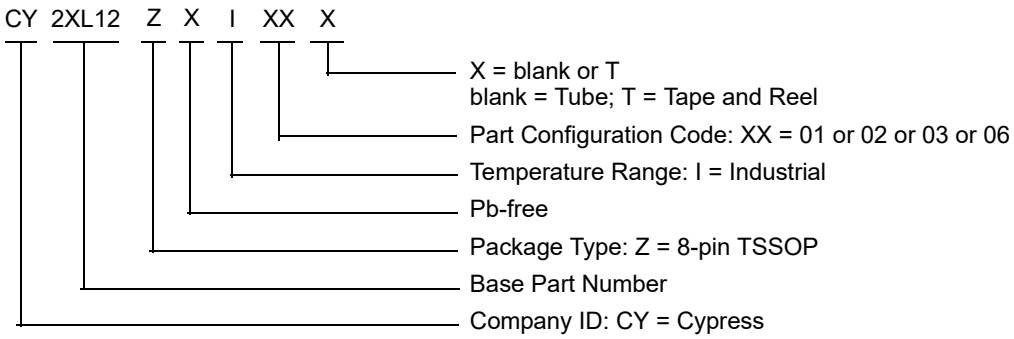
Figure 13. RMS Phase Jitter



Ordering Information

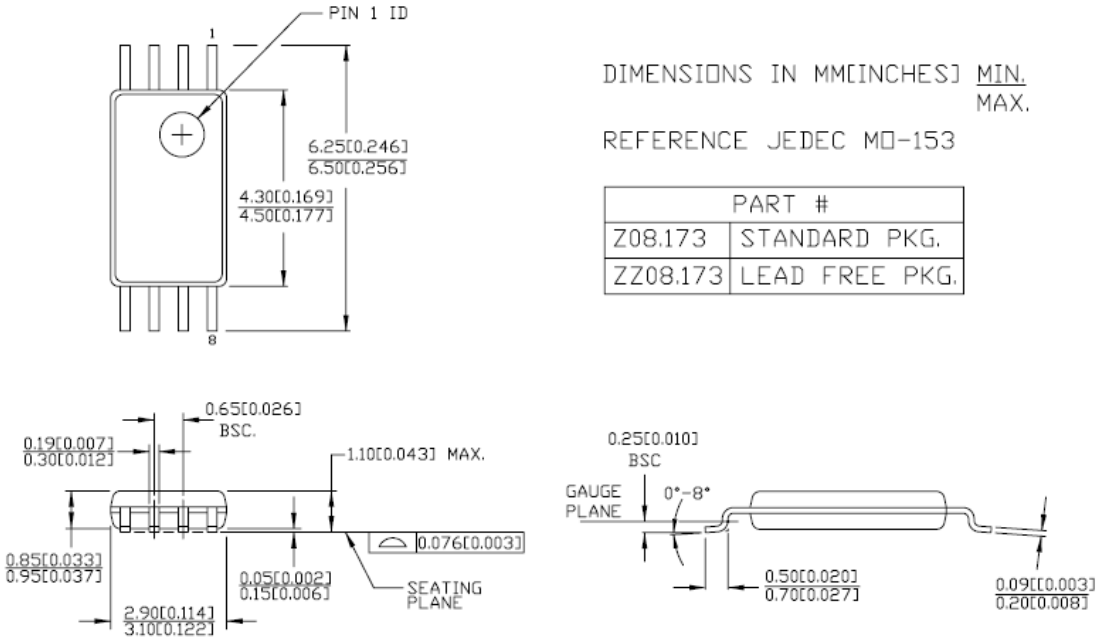
Part Number	Package Description	Product Flow
CY2XL12ZXI	8-pin TSSOP (Unprogrammed device)	Industrial, –40 °C to 85 °C
CY2XL12ZXIT	8-pin TSSOP (Unprogrammed device)	Industrial, –40 °C to 85 °C
CY2XL12ZXI03	8-pin TSSOP (Factory Programmed device)	Industrial, –40 °C to 85 °C
CY2XL12ZXI03T	8-pin TSSOP – Tape and Reel (Factory Programmed device)	Industrial, –40 °C to 85 °C
CY2XL12ZXI06	8-pin TSSOP (Factory Programmed device)	Industrial, –40 °C to 85 °C
CY2XL12ZXI06T	8-pin TSSOP – Tape and Reel (Factory Programmed device)	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 14. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



51-85093 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LVDS	Low-Voltage Differential Signal
OE	Output Enable
PLL	Phase-Locked Loop
RMS	Root Mean Square
TSSOP	Thin Shrunk Small Outline Package
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Units of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2XL12, Low RMS Phase Jitter Programmable LVDS Clock Generator Document Number: 001-63176				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2991849	KVM	07/28/2010	New data sheet.
*A	3117362	BASH	12/21/2010	Updated Features: Added “LVDS PCIe 2.0 Low Jitter XO”. Added Phase Jitter. Added Units of Measure.
*B	3432906	BASH	11/09/2011	Updated Features: Added 150 MHz frequency related information. Updated Frequency Table: Added 150 MHz frequency related information. Updated Ordering Information: Updated part numbers (Added new part numbers CY2XL12ZXI03 and CY2XL12ZXI03T). Updated Package Drawing and Dimensions: spec 51-85093 – Changed revision from *C to *D. Updated to new template.
*C	4120381	CINM	09/11/2013	Updated to new template. Completing Sunset Review.
*D	4700492	TAVA	03/26/2015	Updated Document Title to read as “CY2XL12, Low RMS Phase Jitter Programmable LVDS Clock Generator”. Updated Logic Block Diagram. Updated Pinouts: Updated Figure 1. Updated Package Drawing and Dimensions: spec 51-85093 – Changed revision from *D to *E.
*E	5449404	XHT	09/26/2016	Updated to new template. Completing Sunset Review.
*F	6013629	XHT	01/04/2018	Updated Ordering Information: Updated part numbers. Updated to new template.

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