

# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS

TEXAS INSTR (LIN/INTFC) 25E D

D3371, NOVEMBER 1989

**NOTICE**

SEE ORDER OF DATA FOR ERRATA INFORMATION *7-79-15*

**available features**

- **Excellent Output Drive Capability ...**  
 $V_O = \pm 2.5 \text{ V Min at } R_L = 100 \Omega,$   
 $V_{CC\pm} = \pm 5 \text{ V}$   
 $V_O = \pm 12.5 \text{ V Min at } R_L = 600 \Omega,$   
 $V_{CC\pm} = \pm 15 \text{ V}$
- **Low Supply Current ... 255 μA Typ**
- **Decompensated for High Slew Rate and Gain-Bandwidth Product ...**  
 $A_{VD} = 5 \text{ Min}$   
**Slew Rate = 10 V/μs Typ**  
**Gain-Bandwidth Product = 6.5 MHz Typ**

- **Macromodel Included**
- **Wide Operating Supply Voltage Range ...**  
 $V_{CC\pm} = \pm 3.5 \text{ V to } \pm 20 \text{ V}$
- **High Open-Loop Gain ... 280 V/mV Typ**
- **Low Offset Voltage ... 500 μV Max**
- **Low Offset Voltage Drift with Time ...**  
**0.04 μV/mo Typ**
- **Low Input Bias Current ... 5 pA Typ**

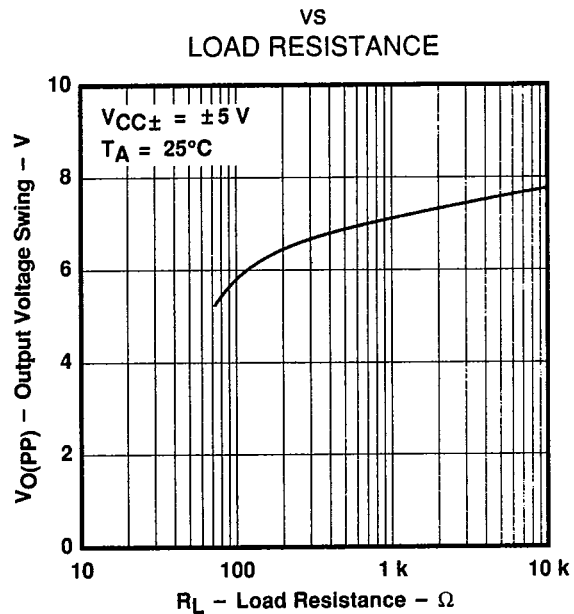
**description**

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

**MAXIMUM PEAK-TO-PEAK  
OUTPUT VOLTAGE SWING**



**AVAILABLE OPTIONS**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGE				
		SMALL- OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	500 μV	—	—	TLE2161BCJG	TLE2161BCL	TLE2161BCP
	1.5 mV	TLE2161ACD	—	TLE2161ACJG	TLE2161ACL	TLE2161ACP
	3 mV	TLE2161CD	—	TLE2161CJG	TLE2161CL	TLE2161CP
-40°C to 85°C	500 μV	—	—	TLE2161BIJG	TLE2161BIL	TLE2161BIP
	1.5 mV	TLE2161AID	—	TLE2161AIJG	TLE2161AIL	TLE2161AIP
	3 mV	TLE2161ID	—	TLE2161IJG	TLE2161IL	TLE2161IP
-55°C to 125°C	500 μV	—	—	TLE2161BMJG	TLE2161BML	TLE2161BMP
	1.5 mV	TLE2161AMD	TLE2161AMFK	TLE2161AMJG	TLE2161AML	TLE2161AMP
	3 mV	TLE2161MD	TLE2161MFK	TLE2161MJG	TLE2161ML	TLE2161MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TLE2161ACDR).

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**EXCALIBUR JFET-INPUT HIGH OUTPUT-DRIVE**  
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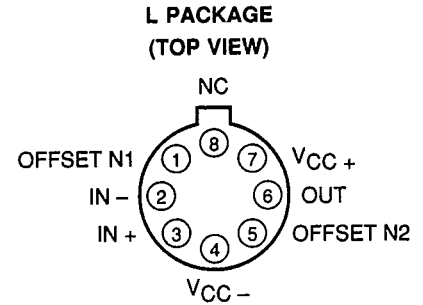
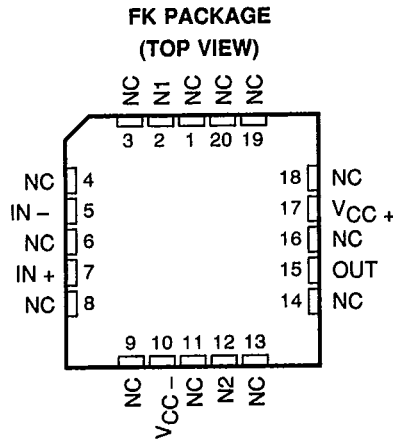
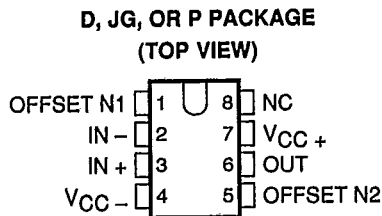
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**description (continued)**

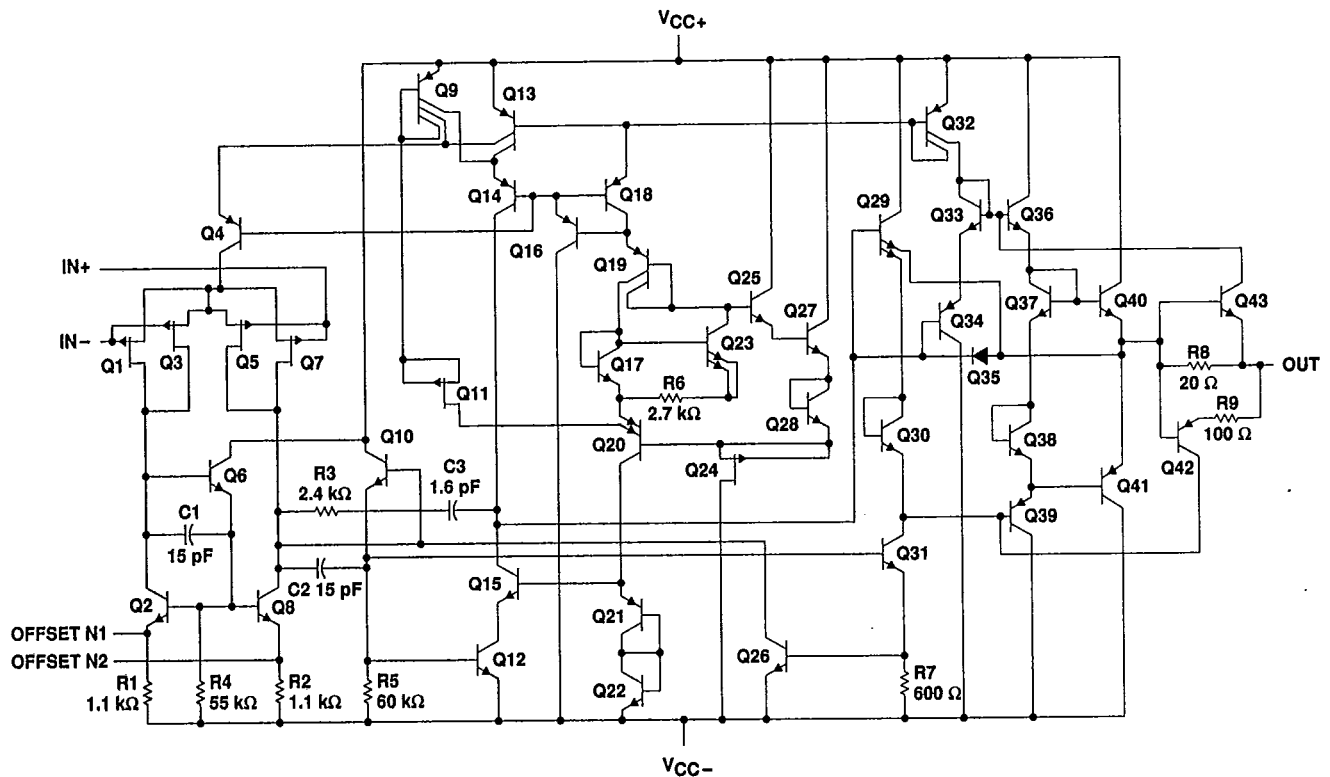
The M-suffix devices are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The I-suffix devices are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The C-suffix devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .



Pin 4 of the L package is in electrical contact with the case.

NC - No internal connection

**equivalent schematic**



All component values are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC+}$ (see Note 1)	22 V
Supply voltage, $V_{CC-}$	-22 V
Differential input voltage (see Note 2)	$\pm 44$ V
Input voltage range, $V_I$ (any input)	$V_{CC\pm}$
Input current, $I_I$ (each input)	$\pm 1$ mA
Output current, $I_O$	$\pm 80$ mA
Total current into $V_{CC+}$ terminal	80 mA
Total current out of $V_{CC-}$ terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : M-suffix	-55°C to 125°C
I-suffix	-40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .  
 2. Differential voltages are at the noninverting input with respect to the inverting input.  
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX		I-SUFFIX		C-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		$\pm 3.5$	$\pm 20$	$\pm 3.5$	$\pm 20$	$\pm 3.5$	$\pm 20$	V
Common-mode input voltage, $V_{IC}$	$V_{CC\pm} = \pm 5$ V	-1.6	4	-1.6	4	-1.6	4	V
	$V_{CC\pm} = \pm 15$ V	-11	13	-11	13	-11	13	
	$V_{CC\pm} = \pm 20$ V	-15	16.5	-15	16.5	-15	16.5	
Operating free-air temperature, $T_A$		-55	125	-40	85	0	70	°C

**TLE2161M, TLE2161AM, TLE2161BM**  
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electrical characteristics at specified free-air temperature,  $V_{CC} \pm = \pm 5 V$

PARAMETER		TEST CONDITIONS		T <sub>A</sub> <sup>†</sup>	MIN	TYP	MAX	UNIT		
V <sub>IO</sub>	Input offset voltage	TLE2161M	V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	0.8	3.1		mV		
				Full range		6				
				25°C	0.6	2.6				
				Full range		4.6				
				25°C	0.5	1.9				
				Full range		3.1				
αV <sub>IO</sub>	Temperature coefficient of input offset voltage			Full range	6			μV/°C		
	Input offset voltage long-term drift (see Note 4)			25°C	0.04			μV/mo		
				25°C	1			pA		
I <sub>IO</sub>	Input offset current			Full range		15		nA		
I <sub>IB</sub>	Input bias current			25°C	3			pA		
				Full range		30		nA		
V <sub>ICR</sub>	Common-mode input voltage range			25°C	-1.6 to 4	-2 to 6		V		
				Full range	-1.6 to 4			V		
V <sub>OM+</sub>	Maximum positive peak output voltage swing	FK, JG, and L packages	R <sub>L</sub> = 10 kΩ	25°C	3.5	3.7		V		
				Full range		3				
				25°C	2.5	3.6				
				Full range		2				
				25°C	2.5	3.1				
				Full range		2				
V <sub>OM-</sub>	Maximum negative peak output voltage swing	FK, JG, and L packages	R <sub>L</sub> = 10 kΩ	25°C	-3.7	-3.9		V		
				Full range		-3				
				25°C	-2.5	-3.5				
				Full range		-2				
				25°C	-2.5	-2.7				
				Full range		-2				
A <sub>VD</sub>	Large-signal differential voltage amplification	FK, JG, and L packages	V <sub>O</sub> = ±2.8 V, R <sub>L</sub> = 10 kΩ	25°C	15	80		V/mV		
				Full range		2				
				25°C	1	65				
				Full range		0.5				
				25°C	1	16				
				Full range		0.5				
				D and P packages	V <sub>O</sub> = 0 to 2 V, R <sub>L</sub> = 100 Ω	25°C	0.75		45	
						Full range			0.5	
						25°C	0.75		3	
						Full range			0.5	
D and P packages	V <sub>O</sub> = 0 to -2 V, R <sub>L</sub> = 100 Ω	25°C	0.75	3						
		Full range		0.5						
		25°C	0.75	3						
		Full range		0.5						

<sup>†</sup>Full range is -55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2161M, TLE2161AM, TLE2161BM  
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE  
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electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 5 V$   
(unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$r_i$ Input resistance		25°C		10 <sup>12</sup>		Ω
$c_i$ Input capacitance		25°C		4		pF
$z_o$ Open-loop output impedance	$I_O = 0$	25°C		560		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR \text{ min}}, R_S = 50 \Omega$	25°C	65	82		dB
		Full range	60			
kSVR Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 5 V \text{ to } \pm 20 V,$ $R_S = 50 \Omega$	25°C	75	93		dB
		Full range	65			
$I_{CC}$ Supply current	$V_O = 0,$ No load	25°C		255	310	μA
		Full range			330	
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		39		μA

†Full range is -55°C to 125°C

operating characteristics,  $V_{CC\pm} = \pm 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		10		V/μs
$V_n$ Equivalent input noise voltage (see Figure 2)	$R_S = 100 \Omega, f = 10 \text{ Hz}$		59		nV/√Hz
	$R_S = 100 \Omega, f = 1 \text{ kHz}$		43		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$		1.1		μV
$I_n$ Equivalent input noise current	$f = 1 \text{ kHz}$		1		fA/√Hz
THD Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2 V$ $f = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$		0.025%		
Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		5.8		MHz
	$f = 100 \text{ kHz}, R_L = 600 \Omega, C_L = 100 \text{ pF}$		4.3		
Settling time	$\epsilon = 0.1\%$		5		μs
	$\epsilon = 0.01\%$		10		
$B_{OM}$ Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10 \text{ k}\Omega$		420		kHz
$\phi_m$ Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		70°		
	$A_{VD} = 5, R_L = 600 \Omega, C_L = 100 \text{ pF}$		84°		

**TLE2161M, TLE2161AM, TLE2161BM**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

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electrical characteristics at specified free-air temperature,  $V_{CC} \pm = \pm 15$  V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161M	$V_{IC} = 0, R_S = 50 \Omega$	25°C	0.6		3	mV
			Full range			6	
	TLE2161AM		25°C	0.5		1.5	
			Full range			3.6	
	TLE2161BM		25°C	0.3		0.5	
			Full range			1.7	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage			Full range	6			$\mu V/^\circ C$
	Input offset voltage long-term drift (see Note 4)		25°C	0.04			$\mu V/mo$
$I_{IO}$ Input offset current			25°C	2			pA
$I_{IB}$ Input bias current			Full range			20	nA
			25°C	4			pA
$V_{ICR}$ Common-mode input voltage range			Full range			40	nA
			25°C	-11 to 13	-12 to 16		V
$V_{OM+}$ Maximum positive peak output voltage swing			Full range	-11 to 13			V
		$R_L = 10 k\Omega$	25°C	13.2	13.7		V
$V_{OM-}$ Maximum negative peak output voltage swing		$R_L = 600 \Omega$	Full range	12.5			
		$R_L = 10 k\Omega$	25°C	12.5	13.2		V
$V_{OM-}$ Maximum negative peak output voltage swing		$R_L = 600 \Omega$	Full range	12			
		$R_L = 10 k\Omega$	25°C	-13.2	-13.7		V
$V_{OD}$ Large-signal differential voltage amplification		$V_O = 0$ to 8 V, $R_L = 600 \Omega$	Full range	-12.5			
		$V_O = 0$ to -8 V, $R_L = 600 \Omega$	25°C	-12.5	-13		V
$A_{VD}$ Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10 k\Omega$	Full range	-12			
		$V_O = 0$ to 8 V, $R_L = 600 \Omega$	25°C	30	230		V/mV
		$V_O = 0$ to -8 V, $R_L = 600 \Omega$	Full range	20			
		$V_O = 0$ to 8 V, $R_L = 600 \Omega$	25°C	25	100		
		$V_O = 0$ to -8 V, $R_L = 600 \Omega$	Full range	7			
		$V_O = 0$ to 8 V, $R_L = 600 \Omega$	25°C	3	25		
	$V_O = 0$ to -8 V, $R_L = 600 \Omega$	Full range	1				
$r_i$ Input resistance			25°C		$10^{12}$		$\Omega$
$c_i$ Input capacitance			25°C		4		pF
$z_o$ Open-loop output impedance		$I_O = 0$	25°C		560		$\Omega$
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICR} \text{ min}, R_S = 50 \Omega$	25°C	72	90		dB
			Full range	65			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} \pm / \Delta V_{IO}$ )		$V_{CC} \pm = \pm 5$ V to $\pm 15$ V, $R_S = 50 \Omega$	25°C	75	93		dB
			Full range	65			
$I_{CC}$ Supply current		$V_O = 0, \text{ No load}$	25°C		265	320	$\mu A$
			Full range			340	
$\Delta I_{CC}$ Supply current change over operating temperature range			Full range		46		$\mu A$

$^\dagger$ Full range is -55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ C$  extrapolated to  $T_A = 25^\circ C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2161M, TLE2161AM, TLE2161BM**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

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operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15V$ 

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C	7	10		V/μs
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100 \Omega, f = 10 \text{ Hz}$	25°C	70			nV/√Hz
		$R_S = 100 \Omega, f = 1 \text{ kHz}$		40			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C	1.1			μV
$I_n$	Equivalent input noise current	$f = 1 \text{ kHz}$	25°C	1.1			fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2 \text{ V}$ $f = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$	25°C	0.025%			
	Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C	6.4			MHz
		$f = 100 \text{ kHz}, R_L = 600 \Omega, C_L = 100 \text{ pF}$		5.6			
	Settling time	$\epsilon = 0.1\%$	25°C	5			μs
		$\epsilon = 0.01\%$		10			
$B_{OM}$	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10 \text{ k}\Omega$	25°C	116			kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C	72°			
		$A_{VD} = 5, R_L = 600 \Omega, C_L = 100 \text{ pF}$		78°			

†Full range is -55°C to 125°C

**TLE2161M, TLE2161AM, TLE2161BM**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
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electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 20\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT		
$V_{IO}$ Input offset voltage	TLE2161M	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	0.6	3		mV		
			Full range		6				
			25°C	0.6	1.6				
	TLE2161AM		Full range		3.6				
			25°C	0.3	0.5				
			Full range		1.7				
	$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Input offset voltage long-term drift (see Note 4)	Full range		6			$\mu\text{V}/^\circ\text{C}$
				25°C	0.04				$\mu\text{V}/\text{mo}$
	$I_{IO}$ Input offset current			25°C	3				pA
Full range				20		nA			
$I_{IB}$ Input bias current		25°C	5			pA			
		Full range		40		nA			
$V_{ICR}$ Common-mode input voltage range		25°C	-15 to 16.5	-17 to 21		V			
		Full range	-15 to 16.5			V			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	18.2	18.7		V			
		Full range	17.5						
	$R_L = 600\ \Omega$	25°C	15	18.1					
		Full range	12						
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	-18.2	-18.7		V			
		Full range	-17.5						
	$R_L = 600\ \Omega$	25°C	-15	-18					
		Full range	-12						
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 15\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	30	280		V/mV			
		Full range	20						
	$V_O = 0\ \text{to}\ 10\ \text{V}, R_L = 600\ \Omega$	25°C	25	80					
		Full range	10						
	$V_O = 0\ \text{to}\ -10\ \text{V}, R_L = 600\ \Omega$	25°C	3	20					
		Full range	1						
$r_i$ Input resistance		25°C		$10^{12}$		$\Omega$			
$c_i$ Input capacitance		25°C		4		pF			
$z_o$ Open-loop output impedance	$I_O = 0$	25°C		560		$\Omega$			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\ \text{min}}, R_S = 50\ \Omega$	25°C	75	91		dB			
		Full range	65						
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 5\ \text{V to } \pm 20\ \text{V}, R_S = 50\ \Omega$	25°C	75	93		dB			
		Full range	65						
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		270	330	$\mu\text{A}$			
		Full range		350					
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		50		$\mu\text{A}$			

$^\dagger$ Full range is -55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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**μPOWER OPERATIONAL AMPLIFIERS**

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operating characteristics,  $V_{CC\pm} = \pm 20\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		10		V/ $\mu\text{s}$
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega$ , $f = 10\text{ Hz}$		75		nV/ $\sqrt{\text{Hz}}$
		$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$		1.1		$\mu\text{V}$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$		1.3		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$A_{VD} = 5$ , $V_{O(PP)} = 2\text{ V}$ $f = 10\text{ kHz}$ , $R_L = 10\text{ k}\Omega$		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		6.5		MHz
		$f = 100\text{ kHz}$ , $R_L = 600\ \Omega$ , $C_L = 100\text{ pF}$		5.7		
	Settling time	$\epsilon = 0.1\%$		5		$\mu\text{s}$
		$\epsilon = 0.01\%$		10		
$B_{OM}$	Maximum output-swing bandwidth	$A_{VD} = 5$ , $R_L = 10\text{ k}\Omega$		85		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		72°		
		$A_{VD} = 5$ , $R_L = 600\ \Omega$ , $C_L = 100\text{ pF}$		78°		

**TLE2161I, TLE2161AI, TLE2161BI**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC} \pm = \pm 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161I	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	0.8	3.1	mV	
			Full range	4.4			
	TLE2161AI		25°C	0.6	2.6		
			Full range	3.9			
	TLE2161BI		25°C	0.5	1.9		
			Full range	2.7			
$\alpha V_{IO}$ Temperature coefficient of input offset voltage			Full range	6		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current			25°C	1		pA	
			Full range		2	nA	
$I_{IB}$ Input bias current			25°C	3		pA	
			Full range		4	nA	
$V_{ICR}$ Common-mode input voltage range			25°C	-1.6 to 4	-2 to 6	V	
			Full range	-1.6 to 4		V	
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	3.5	3.7	V	
		Full range	3.1				
	$R_L = 100\ \Omega$	25°C	2.5	3.1			
		Full range	2				
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	-3.7	-3.9	V	
		Full range	-3.1				
	$R_L = 100\ \Omega$	25°C	-2.5	-2.7			
		Full range	-2				
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 2.8\ \text{V}, R_L = 10\ \text{k}\Omega$		25°C	15	80	V/mV	
		Full range	2				
	$V_O = 0\ \text{to}\ 2\ \text{V}, R_L = 100\ \Omega$	25°C	0.75	45			
		Full range	0.5				
	$V_O = 0\ \text{to}\ -2\ \text{V}, R_L = 100\ \Omega$	25°C	0.75	3			
		Full range	0.5				
$r_i$ Input resistance			25°C		$10^{12}$	$\Omega$	
$c_i$ Input capacitance			25°C		4	pF	
$Z_O$ Open-loop output impedance	$I_O = 0$		25°C		560	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\ \text{min}}, R_S = 50\ \Omega$		25°C	65	82	dB	
		Full range	65				
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} \pm / \Delta V_{IO}$ )	$V_{CC} \pm = \pm 5\ \text{V to } \pm 20\ \text{V}, R_S = 50\ \Omega$		25°C	75	93	dB	
		Full range	65				
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$		25°C	255	310	$\mu\text{A}$	
		Full range	325				
$\Delta I_{CC}$ Supply current change over operating temperature range				Full range	29	$\mu\text{A}$	

$^\dagger$  Full range is -40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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## TLE2161I, TLE2161AI, TLE2161BI EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS

operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 5V$

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C	7	10		V/μs
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega, f = 10\text{ Hz}$	25°C		59	100	nV/√Hz
		$R_S = 100\ \Omega, f = 1\text{ kHz}$			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		μV
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2\text{ V}$ $f = 10\text{ kHz}, R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		5.8		MHz
		$f = 100\text{ kHz}, R_L = 100\ \Omega, C_L = 100\text{ pF}$			4.3		
	Settling time	$\epsilon = 0.1\%$	25°C		5		μs
		$\epsilon = 0.01\%$			10		
$B_{OM}$	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10\text{ k}\Omega$	25°C		420		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		70°		
		$A_{VD} = 5, R_L = 100\ \Omega, C_L = 100\text{ pF}$			84°		

<sup>†</sup>Full range is -40°C to 85°C

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**TLE2161I, TLE2161AI, TLE2161BI**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161I	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	0.6	3		mV
			Full range		4.3		
			25°C	0.5	1.5		
	Full range			2.9			
	25°C		0.3	0.5			
	Full range			1.3			
$\alpha V_{IO}$ Temperature coefficient of input offset voltage			Full range	6		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current			25°C	2		pA	
$I_{IB}$ Input bias current			Full range		3	nA	
			25°C	4		pA	
$V_{ICR}$ Common-mode input voltage range			Full range		5	nA	
			25°C	-11 to 13	-12 to 16		V
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	13.2	13.7		V
		Full range		13			
	$R_L = 600\ \Omega$		25°C	12.5	13.2		
		Full range		12			
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	-13.2	-13.7		V
		Full range		-13			
	$R_L = 600\ \Omega$		25°C	-12.5	-13		
		Full range		-12			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$		25°C	30	230		V/mV
		Full range		20			
	$V_O = 0\ \text{to}\ 8\ \text{V}, R_L = 600\ \Omega$		25°C	25	100		
		Full range		10			
	$V_O = 0\ \text{to}\ -8\ \text{V}, R_L = 600\ \Omega$		25°C	3	25		
		Full range		1			
$r_i$ Input resistance			25°C	$10^{12}$		$\Omega$	
$C_i$ Input capacitance			25°C	4		pF	
$Z_o$ Open-loop output impedance	$I_O = 0$		25°C	560		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}, R_S = 50\ \Omega$		25°C	72	90		dB
		Full range		65			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 5\ \text{V}\ \text{to}\ \pm 15\ \text{V}, R_S = 50\ \Omega$		25°C	75	93		dB
		Full range		65			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$		25°C	265	320		$\mu\text{A}$
		Full range		335			
$\Delta I_{CC}$ Supply current change over operating temperature range			Full range	34		$\mu\text{A}$	

$^\dagger$ Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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**TLE2161I, TLE2161AI, TLE2161BI**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15V$

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C	7	10		$V/\mu s$
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega, f = 10\text{ Hz}$	25°C		70	100	$nV/\sqrt{Hz}$
		$R_S = 100\ \Omega, f = 1\text{ kHz}$			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		$\mu V$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.1		$fA/\sqrt{Hz}$
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2\text{ V}$ $f = 10\text{ kHz}, R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		6.4		MHz
		$f = 100\text{ kHz}, R_L = 600\ \Omega, C_L = 100\text{ pF}$			5.6		
	Settling time	$\epsilon = 0.1\%$	25°C		5		$\mu s$
		$\epsilon = 0.01\%$			10		
$B_{OM}$	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10\text{ k}\Omega$	25°C		116		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		72°		
		$A_{VD} = 5, R_L = 600\ \Omega, C_L = 100\text{ pF}$			78°		

$^\dagger$ Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$

**TLE2161I, TLE2161AI, TLE2161BI**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC} \pm \pm 20$  V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161I	$V_{IC} = 0, R_S = 50 \Omega$	25°C	0.6	3		mV
			Full range		4.3		
	TLE2161AI		25°C	0.6	1.6		
			Full range		2.9		
	TLE2161BI		25°C	0.3	0.5		
			Full range		1.3		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage			Full range	6		$\mu V/^\circ C$	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		$\mu V/mo$	
$I_{IO}$ Input offset current			25°C	3		pA	
			Full range		3	nA	
$I_{IB}$ Input bias current			25°C	5		pA	
			Full range		5	nA	
$V_{ICR}$ Common-mode input voltage range			25°C	-15 to 16.5	-17 to 21		V
			Full range	-15 to 16.5			V
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 k\Omega$		25°C	18.2	18.7		V
		Full range		18			
	$R_L = 600 \Omega$	25°C	15	18.1			
		Full range		12			
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10 k\Omega$		25°C	-18.2	-18.7		V
		Full range		-18			
	$R_L = 600 \Omega$	25°C	-15	-18			
		Full range		-12			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 15$ V, $R_L = 10 k\Omega$		25°C	30	280		V/mV
		Full range		20			
	$V_O = 0$ to 10 V, $R_L = 600 \Omega$	25°C	25	80			
		Full range		10			
	$V_O = 0$ to -10 V, $R_L = 600 \Omega$	25°C	3	20			
		Full range		1			
$r_i$ Input resistance			25°C	$10^{12}$		$\Omega$	
$c_i$ Input capacitance			25°C	4		pF	
$z_o$ Open-loop output impedance	$I_O = 0$		25°C	560		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR} \text{ min}, R_S = 50 \Omega$		25°C	75	91		dB
		Full range		65			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} \pm / \Delta V_{IO}$ )	$V_{CC} \pm = \pm 5$ V to $\pm 20$ V, $R_S = 50 \Omega$		25°C	75	93		dB
		Full range		65			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$		25°C	270	330		$\mu A$
		Full range		345			
$\Delta I_{CC}$ Supply current change over operating temperature range				Full range	36		$\mu A$

$^\dagger$ Full range is -40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ C$  extrapolated to  $T_A = 25^\circ C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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**TLE2161I, TLE2161AI, TLE2161BI**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 20\text{ V}$

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C	7	10		$\text{V}/\mu\text{s}$
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega, f = 10\text{ Hz}$	25°C		75	100	$\text{nV}/\sqrt{\text{Hz}}$
		$R_S = 100\ \Omega, f = 1\text{ kHz}$			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		$\mu\text{V}$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.3		$\text{fA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2\text{ V}$ $f = 10\text{ kHz}, R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		6.5		MHz
		$f = 100\text{ kHz}, R_L = 600\ \Omega, C_L = 100\text{ pF}$			5.7		
	Settling time	$\epsilon = 0.1\%$	25°C		5		$\mu\text{s}$
		$\epsilon = 0.01\%$			10		
BOM	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10\text{ k}\Omega$	25°C		85		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		72°		
		$A_{VD} = 5, R_L = 600\ \Omega, C_L = 100\text{ pF}$			78°		

$^\dagger$ Full range is -40°C to 85°C

**TLE2161C, TLE2161AC, TLE2161BC**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC} \pm = \pm 5 V$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161C	$V_{IC} = 0, R_S = 50 \Omega$	25°C	0.8	3.1		mV
			Full range		4		
	TLE2161AC		25°C	0.6	2.6		
			Full range		3.5		
	TLE2161BC		25°C	0.5	1.9		
			Full range		2.4		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage			Full range	6		$\mu V/^\circ C$	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		$\mu V/mo$	
$I_{IO}$ Input offset current			25°C	1		pA	
$I_{IB}$ Input bias current			Full range		0.8	nA	
			25°C	3		pA	
$V_{ICR}$ Common-mode input voltage range			Full range		2	nA	
			25°C	-1.6 to 4	-2 to 6		V
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	3.5	3.7		V	
		Full range	3.3				
	$R_L = 100 \Omega$	25°C	2.5	3.1			
		Full range	2				
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10 k\Omega$	25°C	-3.7	-3.9		V	
		Full range	-3.3				
	$R_L = 100 \Omega$	25°C	-2.5	-2.7			
		Full range	-2				
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 2.8 V, R_L = 10 k\Omega$	25°C	15	80		V/mV	
		Full range	2				
	$V_O = 0 \text{ to } 2 V, R_L = 100 \Omega$	25°C	0.75	45			
		Full range	0.5				
	$V_O = 0 \text{ to } -2 V, R_L = 100 \Omega$	25°C	0.75	3			
		Full range	0.5				
$r_i$ Input resistance			25°C	$10^{12}$		$\Omega$	
$c_i$ Input capacitance			25°C	4		pF	
$Z_o$ Open-loop output impedance	$I_O = 0$		25°C	560		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR \text{ min}}, R_S = 50 \Omega$	25°C	65	82		dB	
		Full range	65				
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} \pm / \Delta V_{IO}$ )	$V_{CC} \pm = \pm 5 V \text{ to } \pm 20 V, R_S = 50 \Omega$	25°C	75	93		dB	
		Full range	75				
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C	255	310		$\mu A$	
		Full range		320			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		29		$\mu A$	

$^\dagger$ Full range is 0°C to 70°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ C$  extrapolated to  $T_A = 25^\circ C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# TLE2161C, TLE2161AC, TLE2161BC

## EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS

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operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 5V$ 

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C	7	10		V/μs
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100 \Omega, f = 10 \text{ Hz}$	25°C		59	100	nV/√Hz
		$R_S = 100 \Omega, f = 1 \text{ kHz}$			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C		1.1		μV
$I_n$	Equivalent input noise current	$f = 1 \text{ kHz}$	25°C		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2 \text{ V}$ $f = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C		5.8		MHz
		$f = 100 \text{ kHz}, R_L = 100 \Omega, C_L = 100 \text{ pF}$			4.3		
	Settling time	$\epsilon = 0.1\%$	25°C		5		μs
		$\epsilon = 0.01\%$			10		
BOM	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10 \text{ k}\Omega$	25°C		420		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C		70°		
		$A_{VD} = 5, R_L = 100 \Omega, C_L = 100 \text{ pF}$			84°		

†Full range is 0°C to 70°C

**TLE2161C, TLE2161AC, TLE2161BC**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT		
$V_{IO}$ Input offset voltage	TLE2161C	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	0.6		3	mV		
			Full range			3.9			
			25°C	0.5	1.5				
	TLE2161AC		Full range			2.5			
			25°C	0.3	0.5				
			Full range			1			
	$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Input offset voltage long-term drift (see Note 4)	Full range		6			$\mu\text{V}/^\circ\text{C}$
				25°C	0.04				$\mu\text{V}/\text{mo}$
	$I_{IO}$ Input offset current			25°C		2			pA
Full range					1	nA			
$I_{IB}$ Input bias current		25°C		4		pA			
		Full range			3	nA			
$V_{ICR}$ Common-mode input voltage range		25°C	-11 to 13	-12 to 16		V			
		Full range	-11 to 13			V			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	13.2	13.7		V			
		Full range	13						
	$R_L = 600\ \Omega$	25°C	12.5	13.2					
		Full range	12						
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	-13.2	-13.7		V			
		Full range	-13						
	$R_L = 600\ \Omega$	25°C	-12.5	-13					
		Full range	-12						
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	30	230		V/mV			
		Full range	20						
	$V_O = 0\ \text{to}\ 8\ \text{V}, R_L = 600\ \Omega$	25°C	25	100					
		Full range	10						
	$V_O = 0\ \text{to}\ -8\ \text{V}, R_L = 600\ \Omega$	25°C	3	25					
		Full range	1						
$r_i$ Input resistance		25°C		$10^{12}$		$\Omega$			
$c_i$ Input capacitance		25°C		4		pF			
$z_o$ Open-loop output impedance	$I_O = 0$	25°C		560		$\Omega$			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\ \text{min}}, R_S = 50\ \Omega$	25°C	72	90		dB			
		Full range	70						
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 5\ \text{V}\ \text{to}\ \pm 15\ \text{V}, R_S = 50\ \Omega$	25°C	75	93		dB			
		Full range	75						
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		265	320	$\mu\text{A}$			
		Full range			330				
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		34		$\mu\text{A}$			

$^\dagger$ Full range is 0°C to 70°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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**TLE2161C, TLE2161AC, TLE2161BC**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15V$

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$	25°C	7	10		V/μs
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100 \Omega, f = 10 \text{ Hz}$ $R_S = 100 \Omega, f = 1 \text{ kHz}$	25°C		70	100	nV/√Hz
					40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C		1.1		μV
$I_n$	Equivalent input noise current	$f = 1 \text{ kHz}$	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2 \text{ V}$ $f = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$ $f = 100 \text{ kHz}, R_L = 600 \Omega, C_L = 100 \text{ pF}$	25°C		6.4		MHz
					5.6		
	Settling time	$\epsilon = 0.1\%$ $\epsilon = 0.01\%$	25°C		5		μs
					10		
BOM	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10 \text{ k}\Omega$	25°C		116		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$ $A_{VD} = 5, R_L = 600 \Omega, C_L = 100 \text{ pF}$	25°C		72°		
					78°		

†Full range is 0°C to 70°C

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**TLE2161C, TLE2161AC, TLE2161BC**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 20\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	TLE2161C	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		0.6	3	mV
			Full range			3.9	
	TLE2161AC		25°C		0.6	1.6	
			Full range			2.5	
	TLE2161BC		25°C		0.3	0.5	
			Full range			1	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage			Full range		6		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)			25°C		0.04		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current			25°C		3		pA
$I_{IB}$ Input bias current			Full range			1	nA
			25°C		5		pA
$V_{ICR}$ Common-mode input voltage range			Full range			3	nA
			25°C	-15 to 16.5	-17 to 21		V
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	18.2	18.7		V
		Full range		18			
	$R_L = 600\ \Omega$	25°C	15	18.1			
		Full range		12			
$V_{OM-}$ Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$		25°C	-18.2	-18.7		V
		Full range		-18			
	$R_L = 600\ \Omega$	25°C	-15	-18			
		Full range		-12			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 15\ \text{V}, R_L = 10\ \text{k}\Omega$		25°C	30	280		V/mV
		Full range		20			
	$V_O = 0\ \text{to}\ 10\ \text{V}, R_L = 600\ \Omega$	25°C	25	80			
		Full range		10			
	$V_O = 0\ \text{to}\ -10\ \text{V}, R_L = 600\ \Omega$	25°C	3	20			
		Full range		1			
$r_i$ Input resistance			25°C		$10^{12}$		$\Omega$
$c_i$ Input capacitance			25°C		4		pF
$z_o$ Open-loop output impedance	$I_O = 0$		25°C		560		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}, R_S = 50\ \Omega$		25°C	75	91		dB
		Full range		70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 5\ \text{V}\ \text{to}\ \pm 20\ \text{V}, R_S = 50\ \Omega$		25°C	75	93		dB
		Full range		70			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$		25°C	270	330		$\mu\text{A}$
		Full range			340		
$\Delta I_{CC}$ Supply current change over operating temperature range			Full range		18		$\mu\text{A}$

$^\dagger$ Full range is 0°C to 70°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2161C, TLE2161AC, TLE2161BC**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

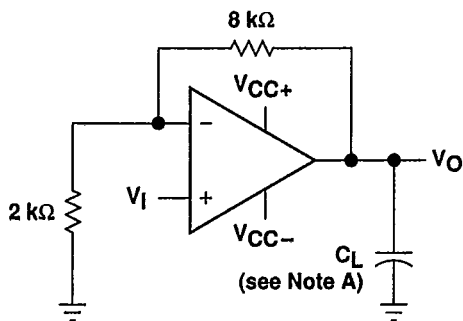
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operating characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 20\text{ V}$ 

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C	7	10		V/ $\mu\text{s}$
			Full range	5			
$V_n$	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega, f = 10\text{ Hz}$	25°C		75	100	nV/ $\sqrt{\text{Hz}}$
		$R_S = 100\ \Omega, f = 1\text{ kHz}$			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		$\mu\text{V}$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.3		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2\text{ V}$ $f = 10\text{ kHz}, R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		6.5		MHz
		$f = 100\text{ kHz}, R_L = 600\ \Omega, C_L = 100\text{ pF}$			5.7		
	Settling time	$\epsilon = 0.1\%$	25°C		5		$\mu\text{s}$
		$\epsilon = 0.01\%$			10		
BOM	Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10\text{ k}\Omega$	25°C		85		kHz
$\phi_m$	Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$	25°C		72°		
		$A_{VD} = 5, R_L = 600\ \Omega, C_L = 100\text{ pF}$			78°		

†Full range is 0°C to 70°C

PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT

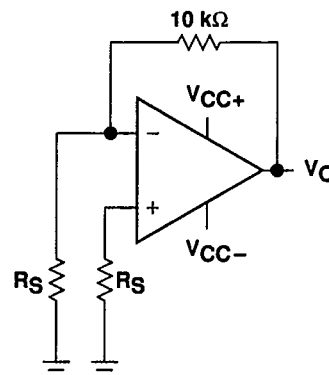
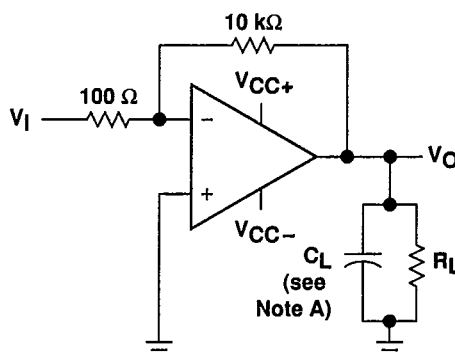


FIGURE 2. NOISE VOLTAGE TEST CIRCUIT



NOTE A:  $C_L$  includes fixture capacitance.

FIGURE 3. GAIN-BANDWIDTH PRODUCT and PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

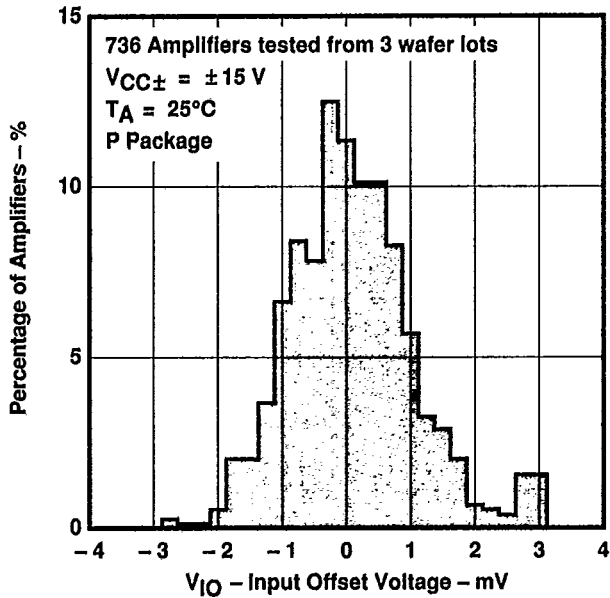
TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
$V_{IO}$	Input offset voltage	Distribution	4
$I_{IB}$	Input bias current	vs Common-mode voltage	5
		vs Temperature	6
$I_{IO}$	Input offset current	vs Temperature	6
$V_{ICR}$	Common-mode input voltage range limits	vs Temperature	7
$V_{OM}$	Maximum peak output voltage swing	vs Output current	8, 9
		vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
$A_{VD}$	Differential voltage amplification	vs Frequency	16
		vs Temperature	17
$I_{OS}$	Short-circuit output current	vs Time	18
		vs Temperature	19
$z_o$	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
$I_{CC}$	Supply current	vs Supply voltage	22
		vs Temperature	23
	Pulse response	Small-signal	24, 25
		Large-signal	26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
$V_n$	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage	32
		vs Temperature	33
$\phi_m$	Phase margin	vs Supply voltage	34
		vs Temperature	35
$\phi$	Phase shift	vs Frequency	16

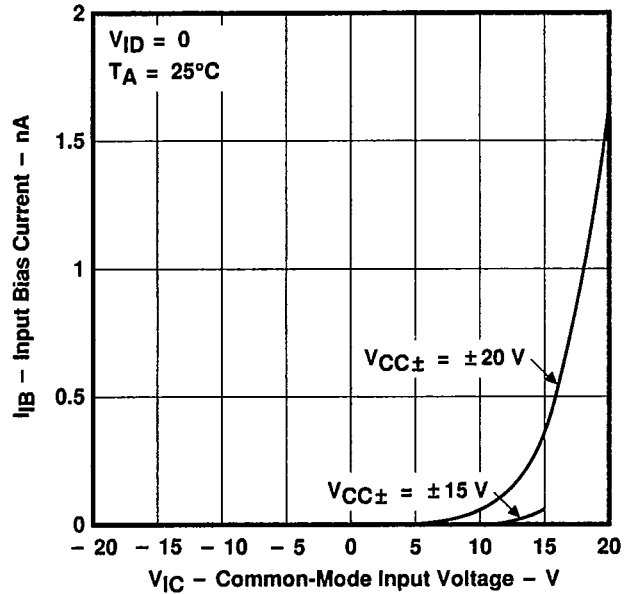
**TYPICAL CHARACTERISTICS†**

**TLE2161**  
**DISTRIBUTION OF**  
**INPUT OFFSET VOLTAGE**



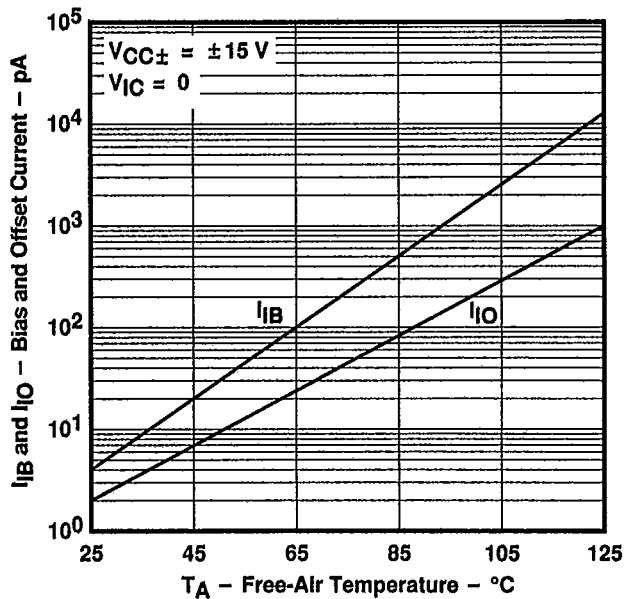
**FIGURE 4**

**INPUT BIAS CURRENT**  
**VS**  
**COMMON-MODE INPUT VOLTAGE**



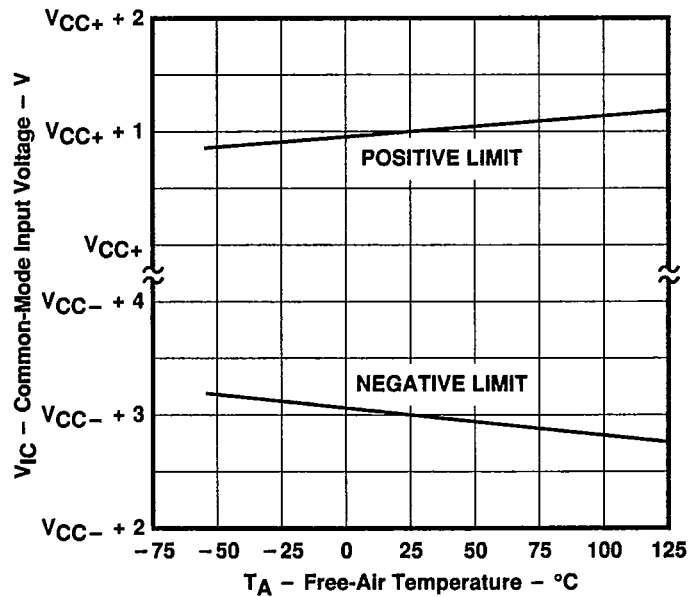
**FIGURE 5**

**INPUT BIAS CURRENT**  
**and INPUT OFFSET CURRENT**  
**VS**  
**FREE-AIR TEMPERATURE**



**FIGURE 6**

**COMMON-MODE**  
**INPUT VOLTAGE RANGE LIMITS**  
**VS**  
**FREE-AIR TEMPERATURE**



**FIGURE 7**

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK  
OUTPUT VOLTAGE  
VS  
OUTPUT CURRENT

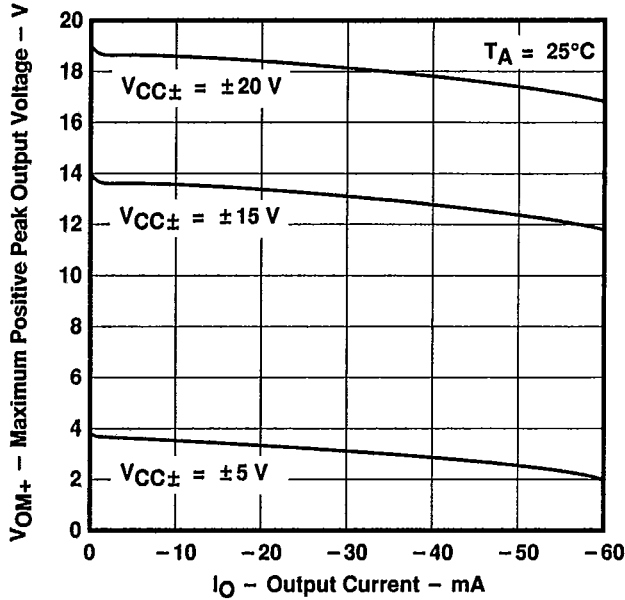


FIGURE 8

MAXIMUM NEGATIVE PEAK  
OUTPUT VOLTAGE  
VS  
OUTPUT CURRENT

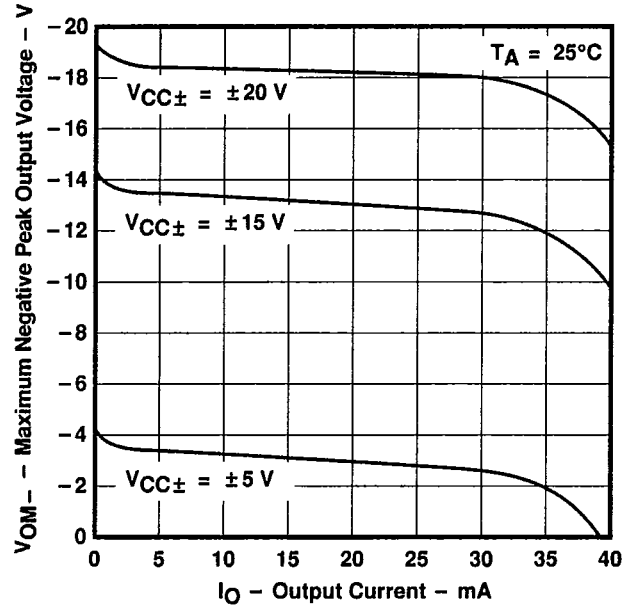


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE  
VS  
SUPPLY VOLTAGE

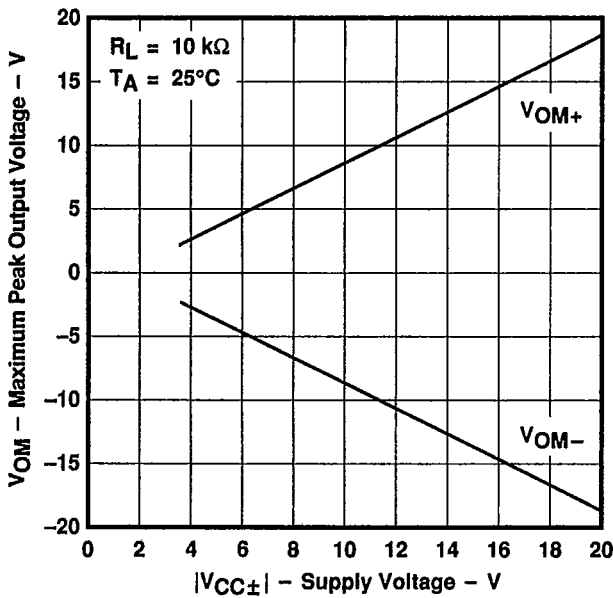


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE  
VS  
SUPPLY VOLTAGE

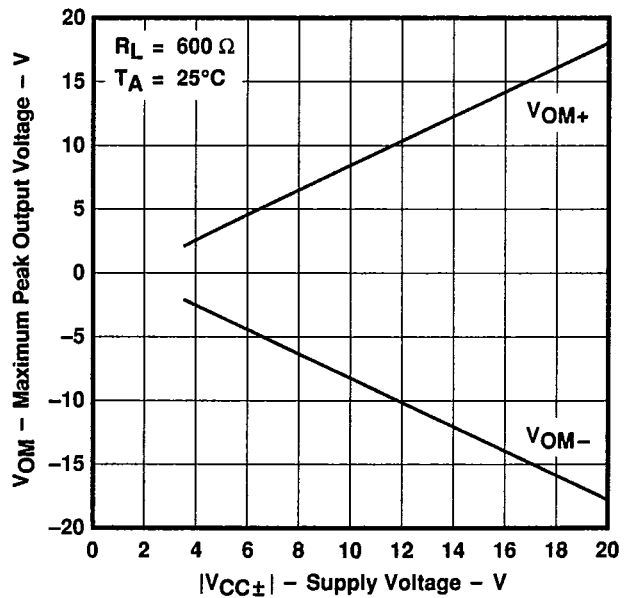


FIGURE 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE  
 VS  
 SUPPLY VOLTAGE

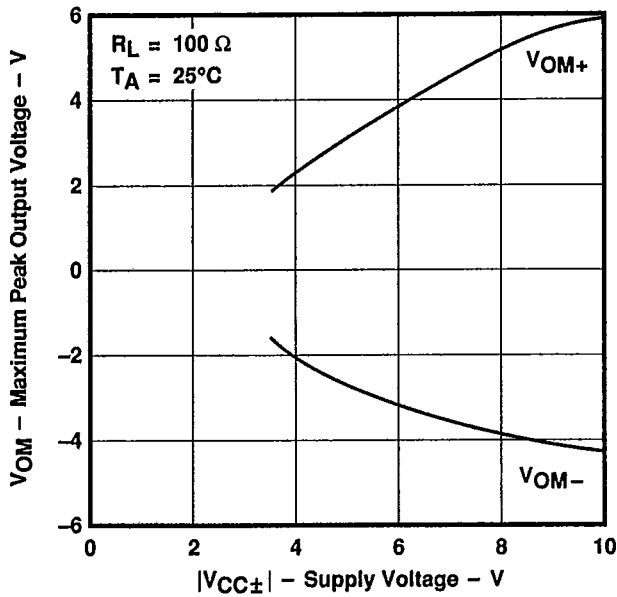


FIGURE 12

MAXIMUM PEAK-TO-PEAK  
 OUTPUT VOLTAGE  
 VS  
 FREQUENCY

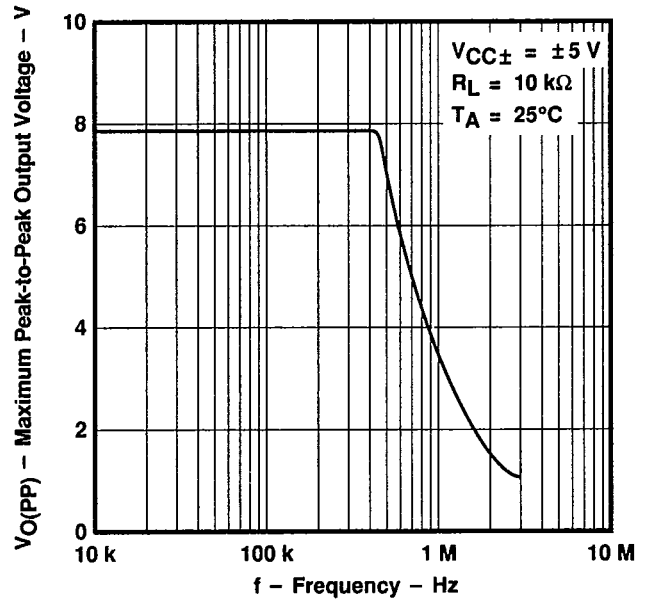


FIGURE 13

MAXIMUM PEAK-TO-PEAK  
 OUTPUT VOLTAGE  
 VS  
 FREQUENCY

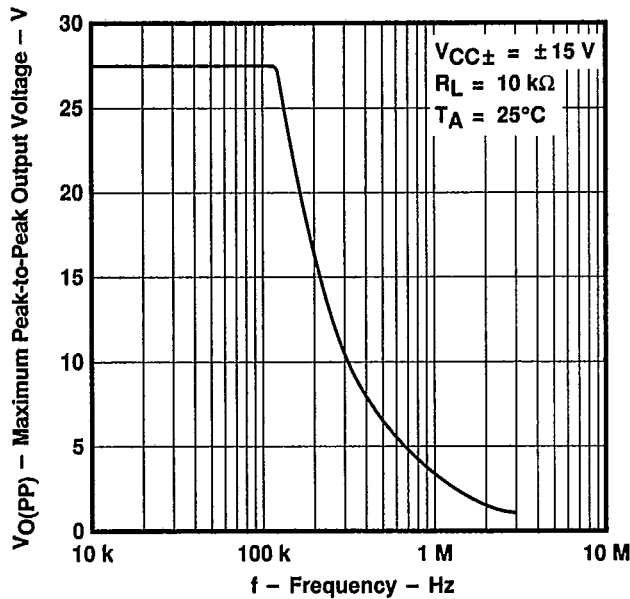


FIGURE 14

MAXIMUM PEAK-TO-PEAK  
 OUTPUT VOLTAGE  
 VS  
 FREQUENCY

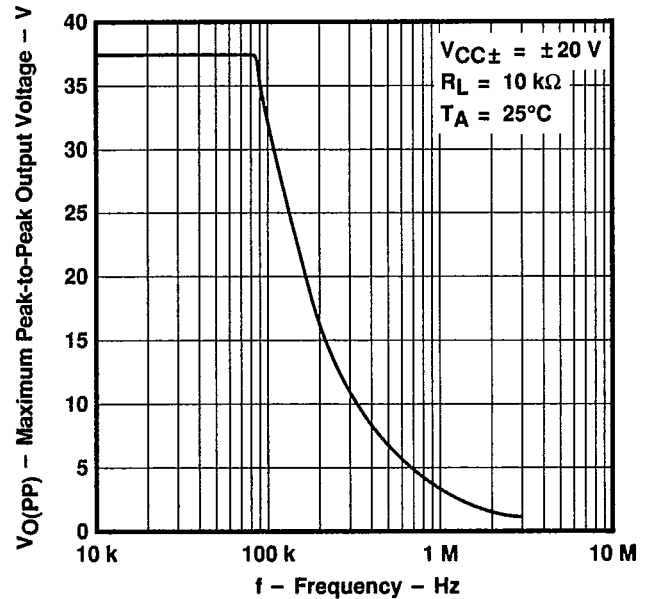


FIGURE 15

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TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT

VS  
FREQUENCY

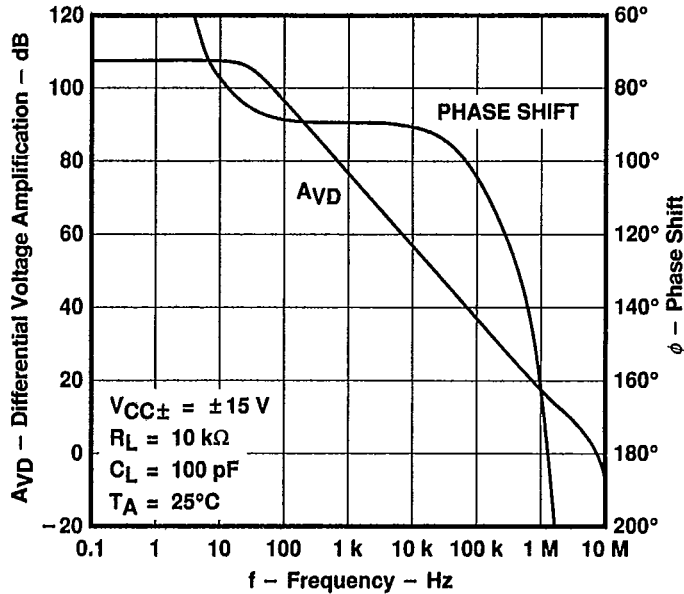


FIGURE 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION

VS  
FREE-AIR TEMPERATURE

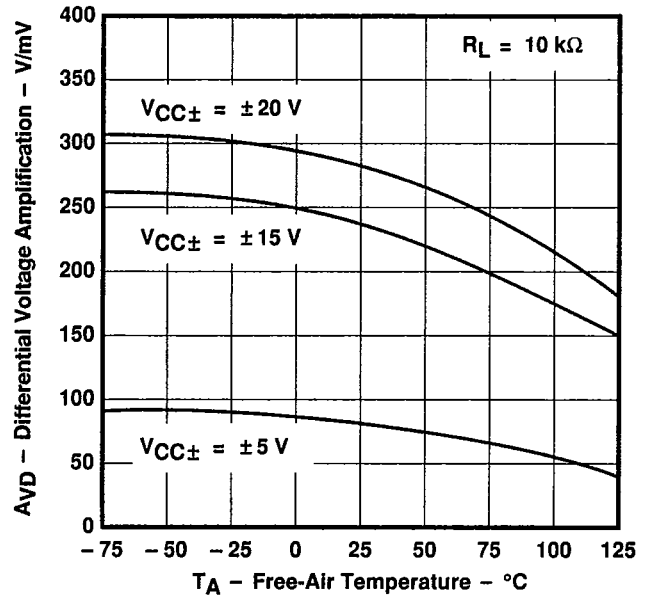


FIGURE 17

SHORT-CIRCUIT OUTPUT CURRENT

VS  
ELAPSED TIME

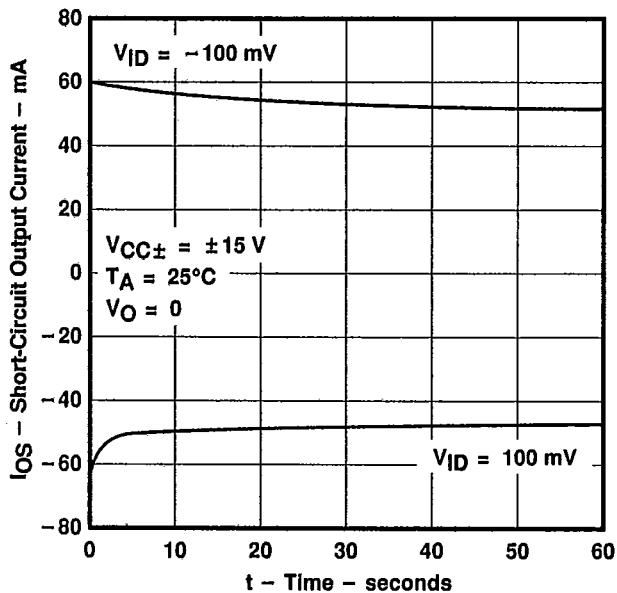


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT

VS  
FREE-AIR TEMPERATURE

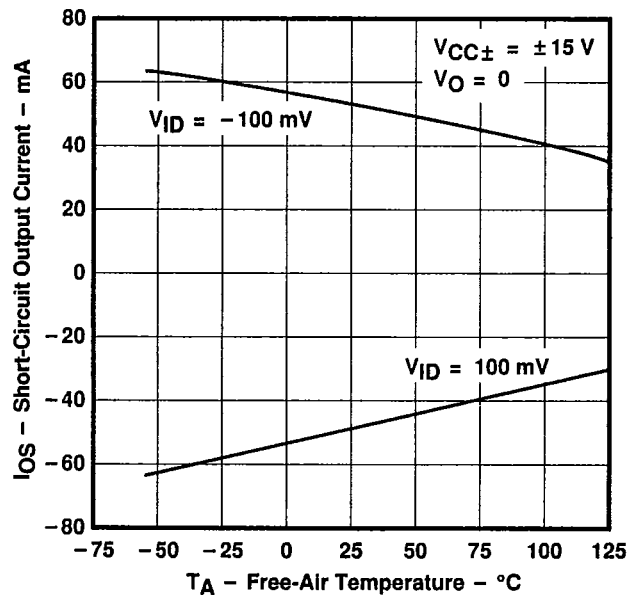


FIGURE 19

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE  
 VS  
 FREQUENCY

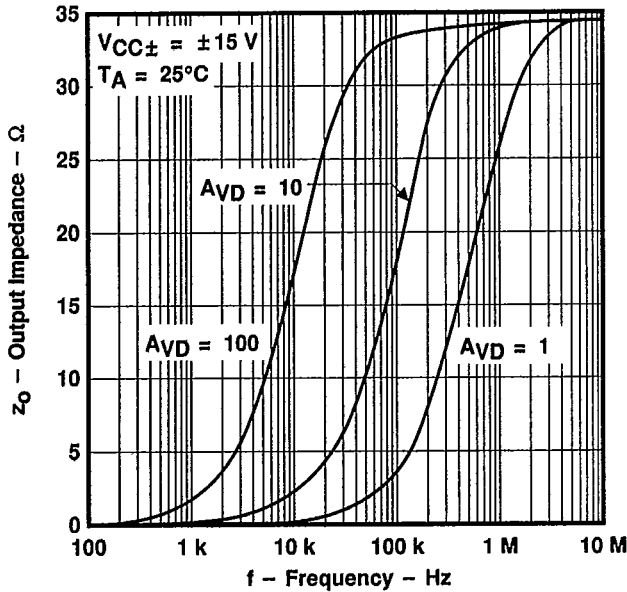


FIGURE 20

COMMON-MODE REJECTION RATIO  
 VS  
 FREQUENCY

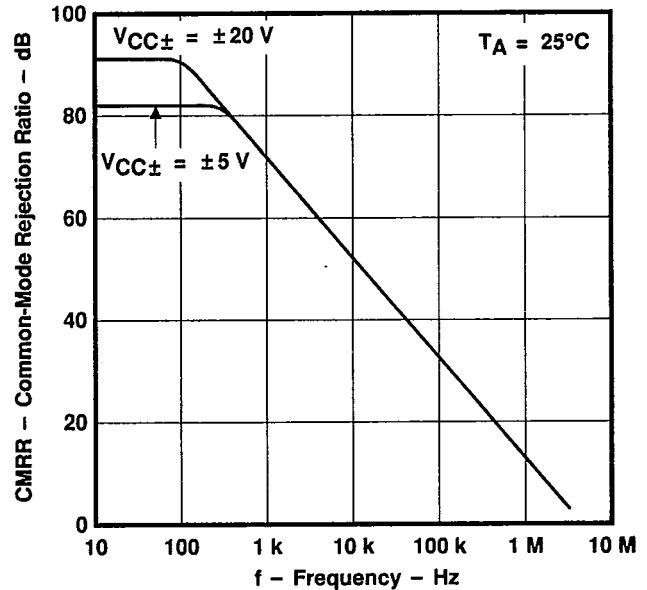


FIGURE 21

SUPPLY CURRENT  
 VS  
 SUPPLY VOLTAGE

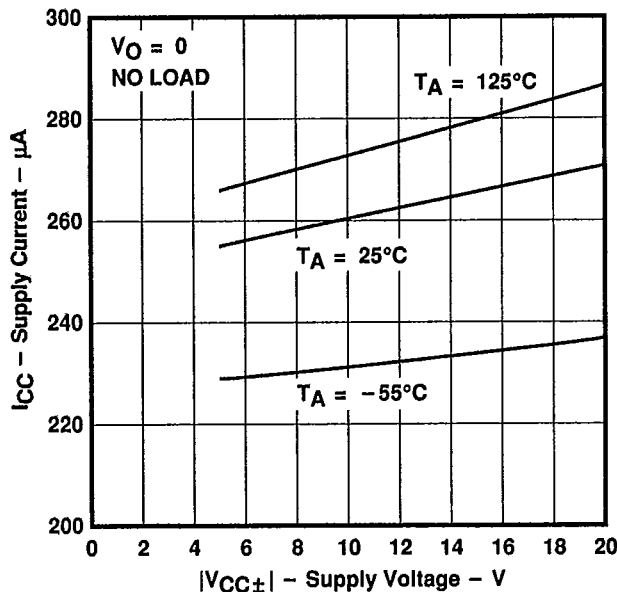


FIGURE 22

SUPPLY CURRENT  
 VS  
 FREE-AIR TEMPERATURE

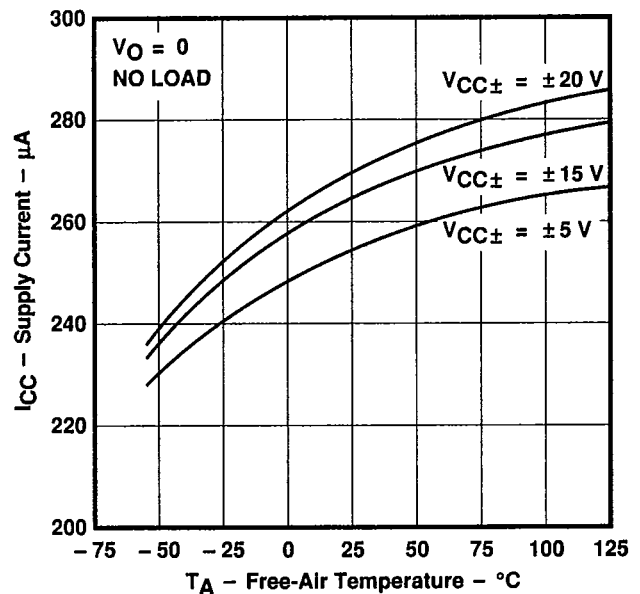


FIGURE 23

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SMALL-SIGNAL  
PULSE RESPONSE

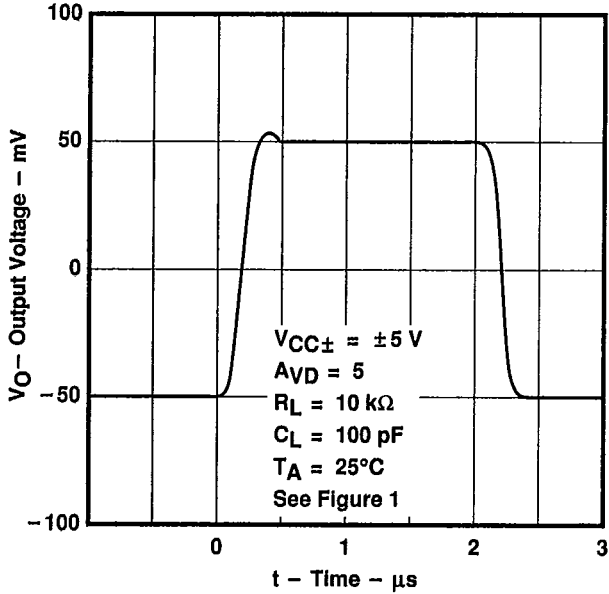


FIGURE 24

SMALL-SIGNAL  
PULSE RESPONSE

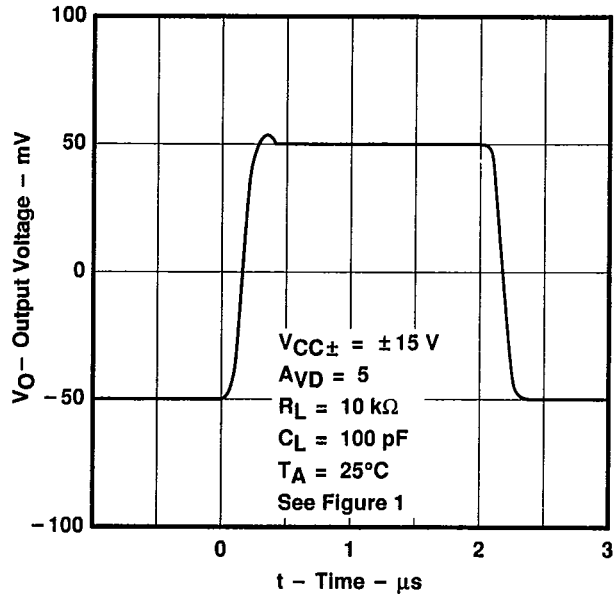


FIGURE 25

LARGE-SIGNAL  
PULSE RESPONSE

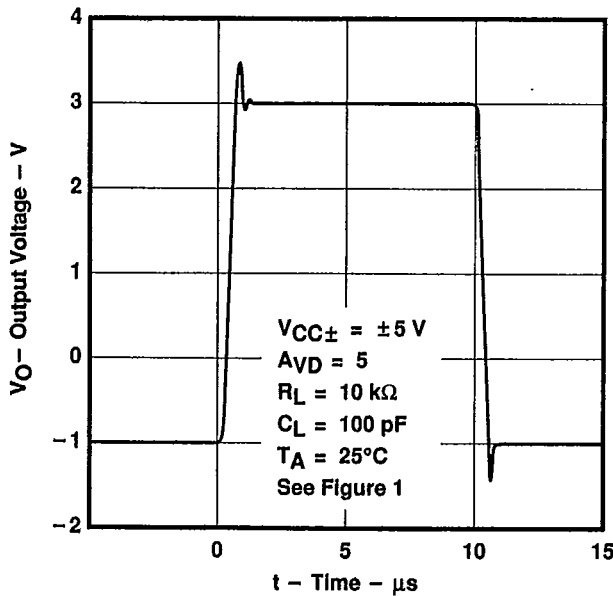


FIGURE 26

LARGE-SIGNAL  
PULSE RESPONSE

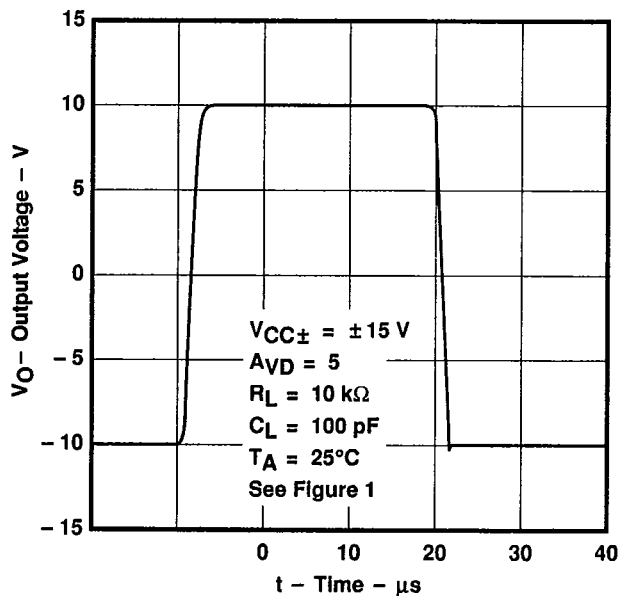
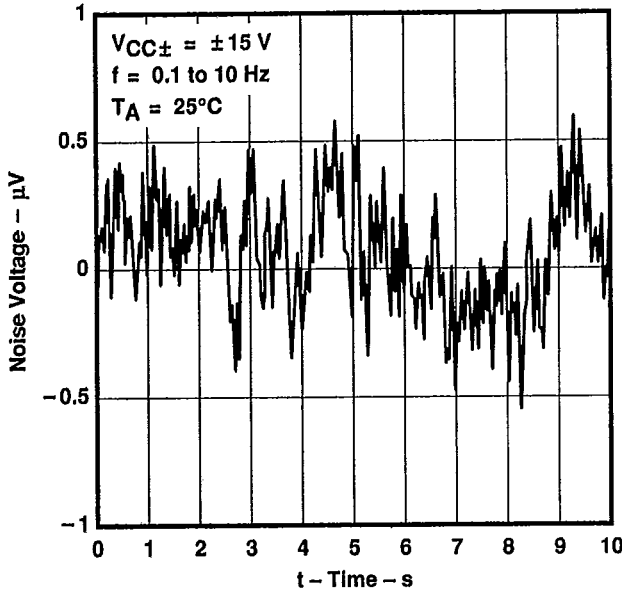


FIGURE 27

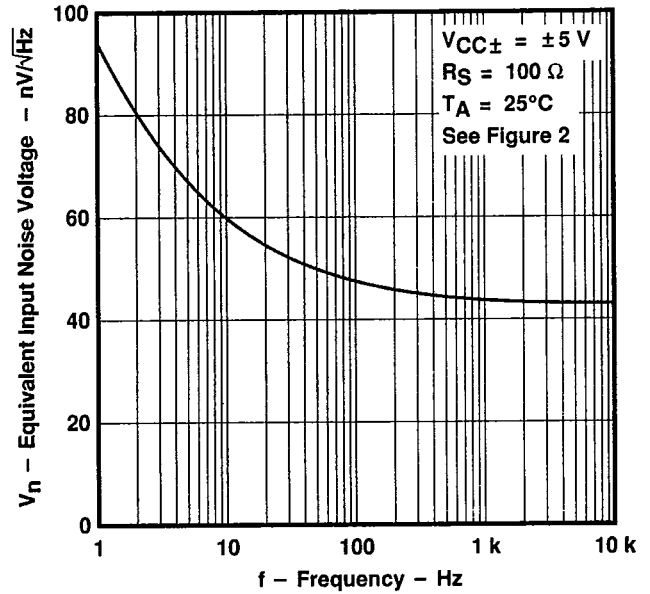
**TYPICAL CHARACTERISTICS**

**NOISE VOLTAGE**  
**(REFERRED TO INPUT)**  
**OVER A 10-SECOND INTERVAL**



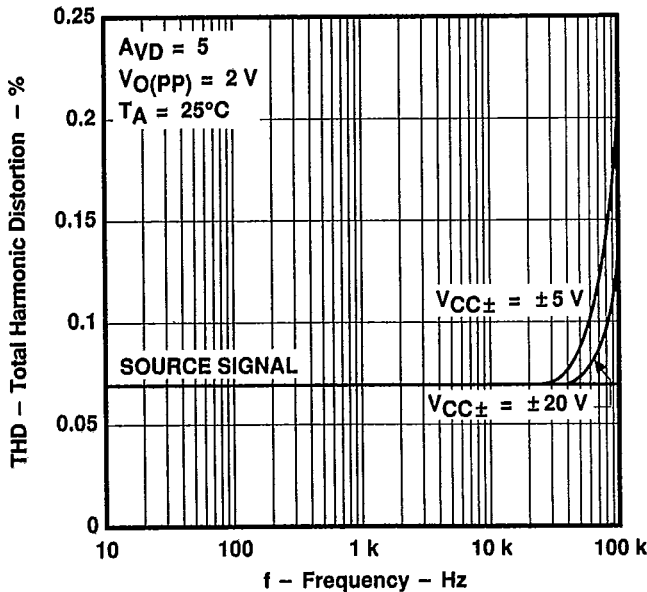
**FIGURE 28**

**EQUIVALENT INPUT NOISE VOLTAGE**  
**VS**  
**FREQUENCY**



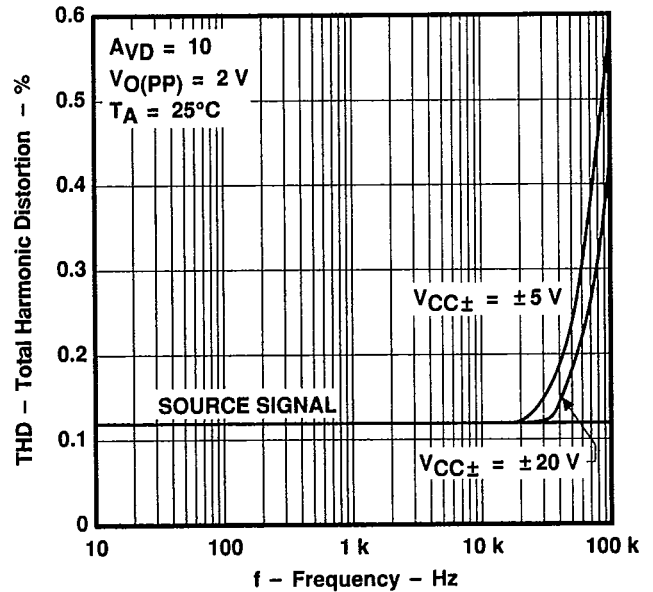
**FIGURE 29**

**TOTAL HARMONIC DISTORTION**  
**VS**  
**FREQUENCY**



**FIGURE 30**

**TOTAL HARMONIC DISTORTION**  
**VS**  
**FREQUENCY**



**FIGURE 31**

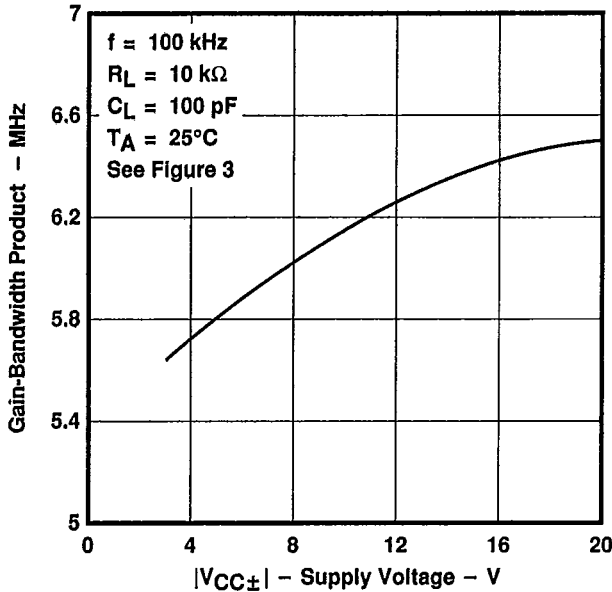
**TLE2161, TLE2161A, TLE2161B**  
**EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE**  
**μPOWER OPERATIONAL AMPLIFIERS**

TEXAS INSTR (LIN/INTFC) 25E D

T-79-15

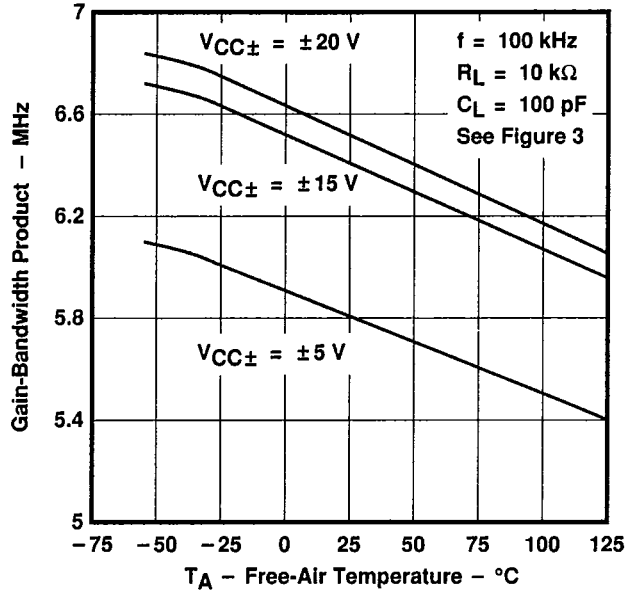
**TYPICAL CHARACTERISTICS†**

**GAIN-BANDWIDTH PRODUCT**  
**VS**  
**SUPPLY VOLTAGE**



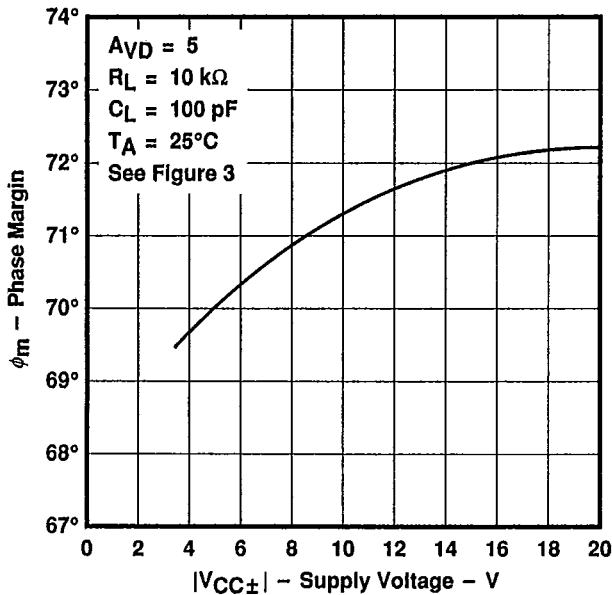
**FIGURE 32**

**GAIN-BANDWIDTH PRODUCT**  
**VS**  
**FREE-AIR TEMPERATURE**



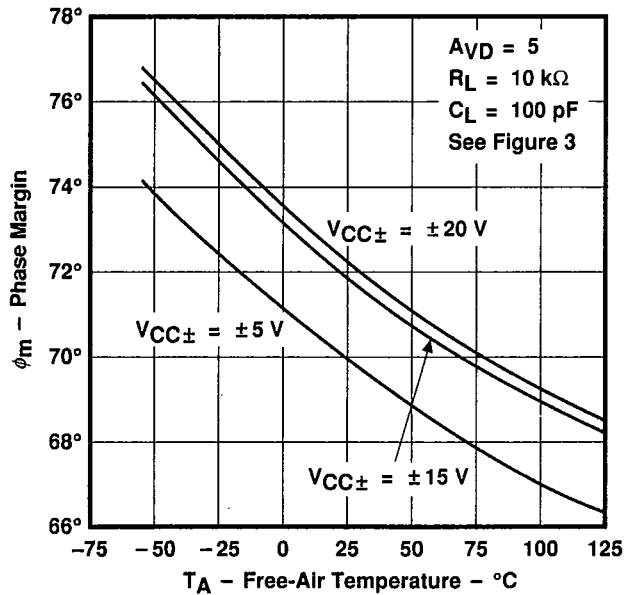
**FIGURE 33**

**PHASE MARGIN**  
**VS**  
**SUPPLY VOLTAGE**



**FIGURE 34**

**PHASE MARGIN**  
**VS**  
**FREE-AIR TEMPERATURE**



**FIGURE 35**

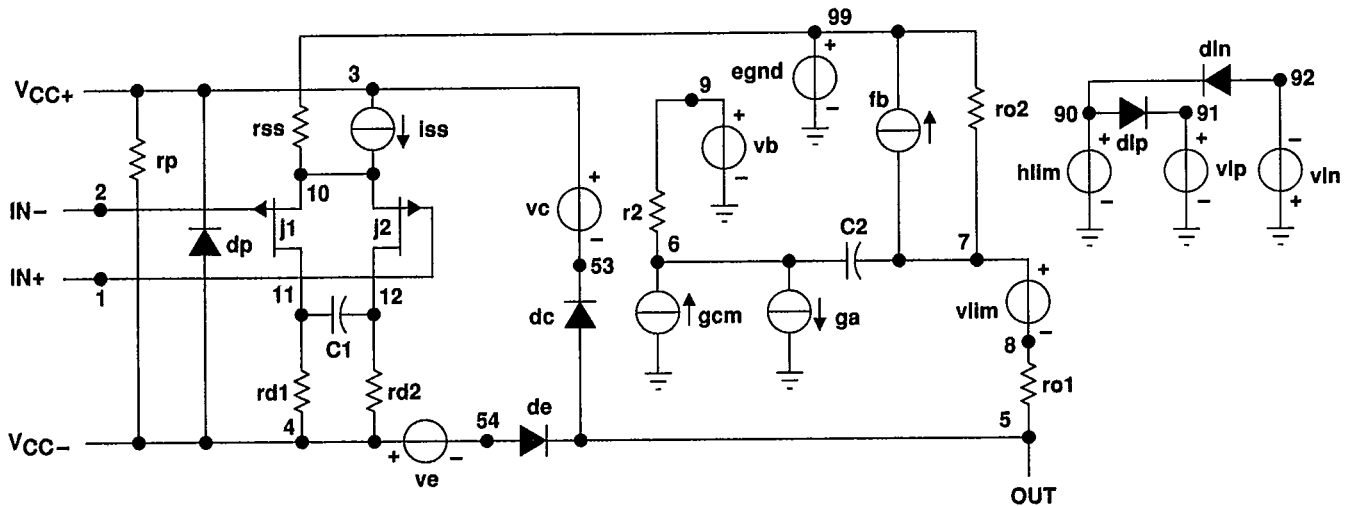
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL APPLICATION DATA**

**macromodel information**

Macromodel information provided was derived using *PSpice® Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figures 36 and 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit



**FIGURE 36. BOYLE MACROMODEL**

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

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*Parts* is a trademark of MicroSim Corporation.

Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specifications and operating characteristics of the semiconductor product to which the model relates.



TYPICAL APPLICATION DATA

macromodel information (continued)

```
.subckt TLE2161 1 2 3 4 5
c1 11 12 125.4E-14
c2 6 7 5.000E-12
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 4.085E6 -4E6 4E6 4E6 -4E6
ga 6 0 11 12 201.1E-6
gcm 0 6 10 99 3.576E-9
iss 3 10 dc 45.00E-6
hlim 90 0 vlim 1K
j1 11 2 10 jx
j2 12 1 10 jx
r2 6 9 100.0E3
rd1 4 11 4.973E3
rd2 4 12 4.973E3
ro1 8 5 280
ro2 7 99 280
rp 3 4 113.2E3
rss 10 99 4.444E6
vb 9 0 dc 0
vc 3 53 dc 2
ve 54 4 dc 2
vlim 7 8 dc 0
vlp 91 0 dc 50
vln 0 92 dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=1.000E-12 Beta=480E-6 Vto=-1)
.ends
```

FIGURE 37. MACROMODEL SUBCIRCUIT

TYPICAL APPLICATION DATA

input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

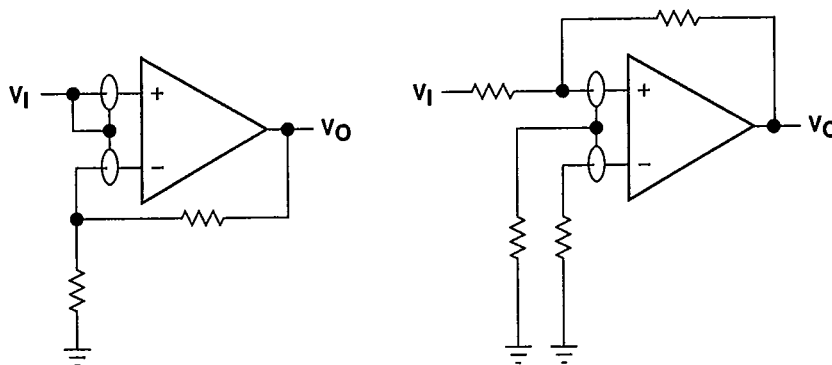


FIGURE 38. USE OF GUARD RINGS

input offset voltage nulling

The TLE2161 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 39 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

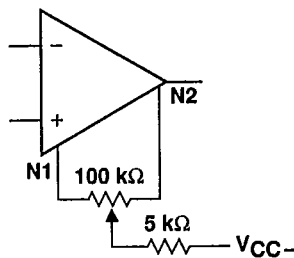


FIGURE 39. INPUT OFFSET VOLTAGE NULLING